

Recent Advances and New Trends in Flip Chip Technology

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Recent advances in flip chip technology such as wafer bumping, package substrate, flip chip assembly, and underfill will be presented in this study. Emphasis is placed on the latest developments of these areas in the past few years. Their future trends will also be recommended. [DOI: 10.1115/1.4034037]

1 Introduction

In this paper, a flip chip is defined [1–4] as a chip attached to the pads of a substrate or another chip with various interconnect materials (e.g., Sn–Pb, Cu, Au, Ag, Ni, In, and isotropic or anisotropic conductive adhesives) and methods (e.g., mass reflow and thermocompression bonding (TCB)), as long as the chip surface (active area or I/O-side) is facing the substrate or another chip as shown in Fig. 1.

The flip chip technology was introduced by IBM in the early 1960s for their solid logic technology, which became the logical foundation of the IBM System/360 computer line [5]. Figure 2(a) shows the first IBM flip chip with three terminal transistors, which are Ni/Au plated Cu balls embedded in a Sn–Pb solder bump on the three I/O pads of transistor. A Cr–Cu–Au adhesion/seed layer is deposited between the Al–Si contact pads on the Si chip and the solder bump. Figure 2(b) shows the first IBM flip chip assembly (three chips) on a ceramic substrate.

As the I/Os increase, the Cu ball is replaced by solder bump. The so-called C4 (controlled-collapse chip connection) technology [6] utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder.

Today, the applications of flip chip technology have been extended to [7–12] chip-to-chip, face-to-face, and face-to-back. Figure 3 shows Amkor's Double-POSSUM™ package [12]. It can be seen that the package is actually defined by two levels of nesting die. The three daughter dies are flip-chip attached to the larger mother die which is then attached to the largest grandma die. The grandma die is then flip-chip attached to the package substrate. The bumps between the daughter dies and the mother die are microbumps (Cu-pillar with solder cap). C4 bumps are used between the mother die and grandma die, and between the grandma die and package substrate.

Flip chip technologies have been used extensively for the processors of mainframe computers, servers, personal computers, notebooks, smartphones, tablets, games, etc., the application-specific integrated circuits (ASICs) of networking, telecommunications, etc., and the memories of data storage devices, etc. Most of the flip chip assemblies are mass reflowed.

Recently, because of the requirements of higher functionalities of the chips and shrinking the chips' area, the number of pin-outs of the processors, ASICs, and memories increases and their pitch (or the spacing between the pin-out pads) decreases. Also, because of the trends of smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and thinner

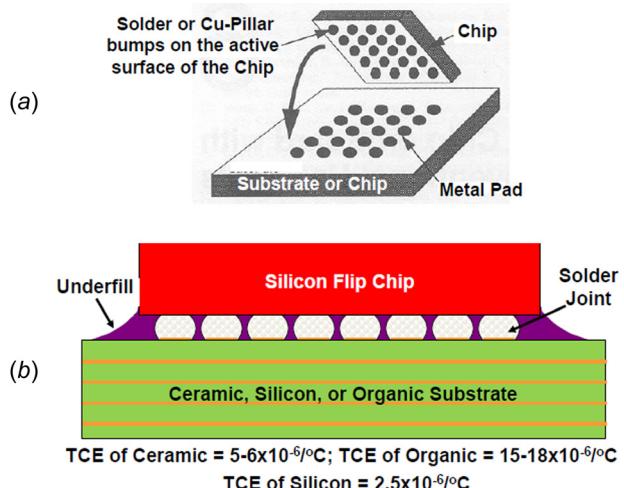


Fig. 1 (a) Definition of flip chip assembly and (b) flip chip assembly on various substrates

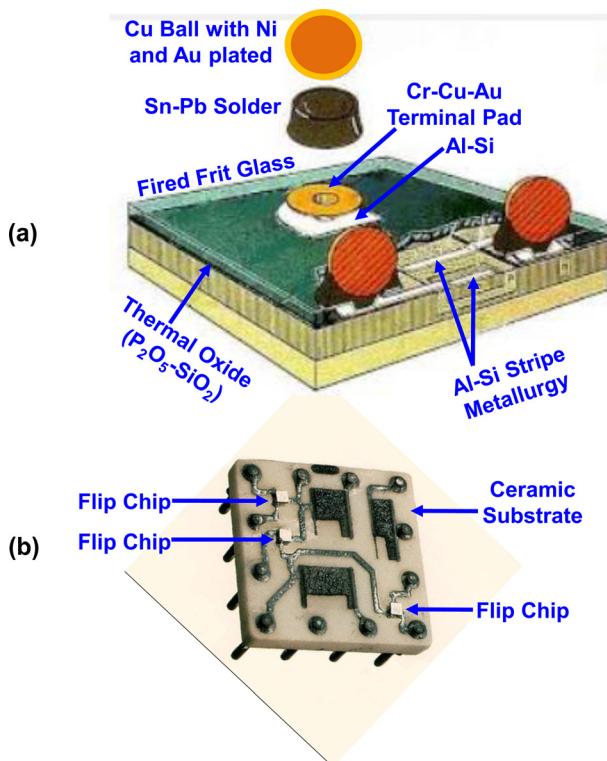


Fig. 2 (a) IBM's first flip chip component with three terminal transistors and (b) IBM's first flip chip assembly (three chips) on a ceramic substrate

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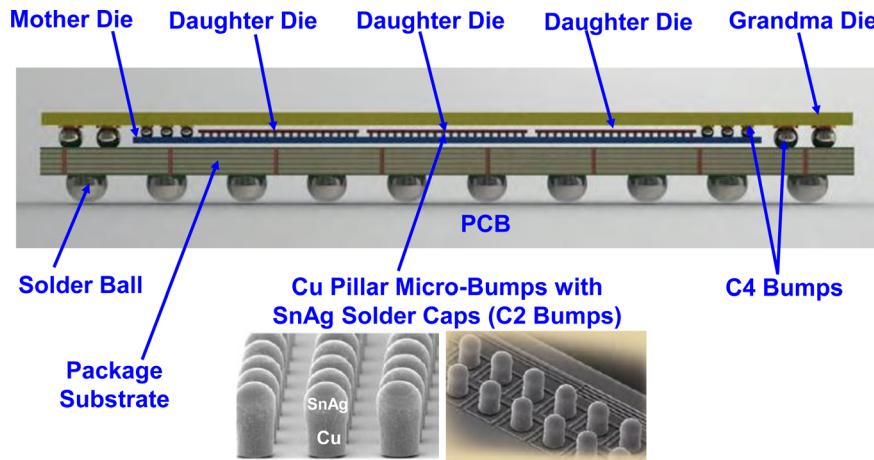


Fig. 3 Three-dimensional integrated circuit (IC) packaging (Amkor's multiple chip-to-chip interconnects)

package substrates lead to the necessity of the TCB method for flip-chip assemblies. In this study, besides mass reflow, various TCB techniques are mentioned.

Recent advances in high-density and low-cost package substrates have promoted more flip chip applications. In this study, the organic build-up substrate, through-silicon via (TSV)-interposer, TSV-less interposer, organic build-up substrate with thin-film layers, coreless substrate, bump-on-lead (BOL), and embedded-trace-substrate (ETS) will be discussed.

In order to enhance the solder joint reliability of flip chip assemblies, underfill is a must, especially for organic package substrate. In this study, the pre-assembly underfill such as the no-flow underfill (NUF), nonconductive paste (NCP), and nonconductive film (NCF) will be discussed. Also, the post-assembly underfill such as the capillary underfill (CUF) and molded underfill (MUF) will be examined. Since wafer bumping is the mother of flip chip technology, it will be briefly mentioned first.

2 Wafer Bumping

There are many ways to perform the wafer bumping (at least 12 are shown in Ref. [2]), and the most common method is by

electrochemical deposition (ECD) or electroplating [13]. Stencil printing method [14–20] is also used for wafer bumping but it will not be presented herein.

2.1 C4 Bumps. Usually the pad size is equal to $100 \mu\text{m}$ and the target bump height is equal to $100 \mu\text{m}$. After redefining the passivation opening (usually it is not required), either Ti or TiW ($0.1\text{--}0.2 \mu\text{m}$) are sputtered over the entire surface of the wafer first, followed by $0.3\text{--}0.8 \mu\text{m}$ of Cu. Ti–Cu and TiW–Cu are called under bump metallurgy (UBM). In order to obtain $100 \mu\text{m}$ bump height, a $40 \mu\text{m}$ layer of resist is then overlaid on the Ti–Cu or TiW–Cu and a solder bump mask is used to define (ultraviolet exposure) the bump pattern as shown in steps #1–4 in Fig. 4. The opening in the resist is $7\text{--}10 \mu\text{m}$ wider than the pad opening in the passivation layer. A $5 \mu\text{m}$ layer of Cu is then plated over the UBM, followed by electroplating the solder. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the target ($100 \mu\text{m}$), the solder is plated over the resist coating by about $15 \mu\text{m}$ to form a mushroom shape. The resist is then stripped off and the Ti–Cu or TiW–Cu is removed with a

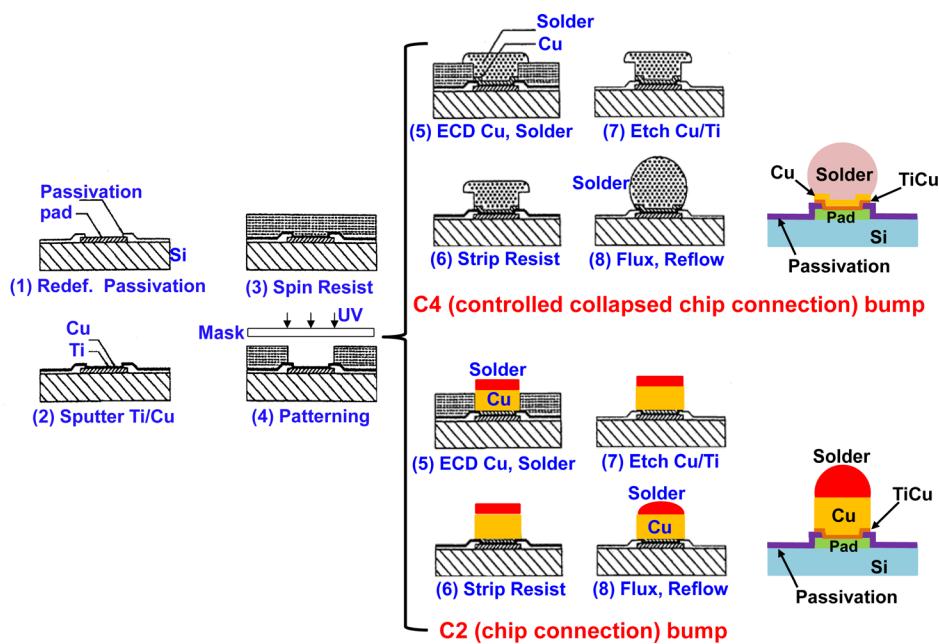


Fig. 4 Wafer bumping by ECD or electroplating method for C4 and C2 bumps

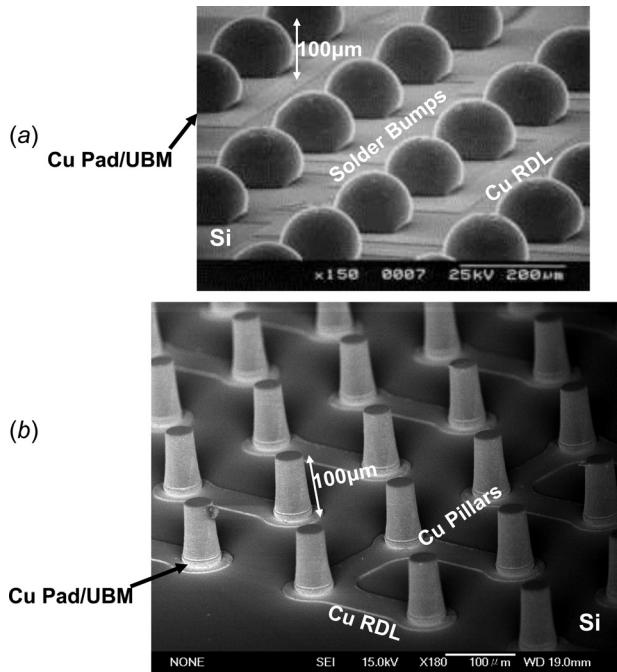


Fig. 5 Scanning electron microscopy images of (a) C4 solder bumps and (b) C2 Cu-pillar without solder cap

hydrogen peroxide or plasma etching. The wafer is then reflowed with flux, which creates smooth truncated spherical solder C4 bumps, Figs. 3 and 5(a), due to surface tension as shown in steps #5–8 on the upper right-hand side of Fig. 4 [13].

2.2 Fan-In Wafer-Level Packaging—Wafer-Level Chip Scale Package (WLCSP). Figure 6 shows the wafer bumping of a WLCSP [21]. Basically, it is the same process as the previous one. Except, instead of making the solder bump on the original pads of the chip on a wafer, add a redistribution layer (RDL) and transfer (fan-in) the original pads to the interior of the chip and make bigger pads, and thus, larger solder bumps with pitch ranges

from 0.5, 0.4, 0.35, and 0.3 mm. These bumped chips ($\leq 5 \text{ mm} \times 5 \text{ mm}$) can be directly attached onto printed circuit board (PCB) without underfill [21–23].

2.3 Fan-Out Wafer-Level Packaging (FOWLP). Figure 7 schematically shows the cross sections of a typical FOWLP. The manufacturing process flow is very simple [24,25]. First, the device wafer is tested for known-good dies (KGDs) and then singulated into individual dies. This is followed by picking up the KGDs and placing them face-down or face-up on a temporary carrier that can be round (wafer) or rectangular (panel) with a double-sided thermal release tape. Then, the reconfigured carrier is over-molded using the compression molding method with epoxy mold compound (EMC) before removing the carrier and the double-sided tape and turning the whole molding (with KGDs) around. Next comes building the RDLs for signals, power, and grounds from the pads. Finally, solder balls (with pitch ranges from 1.27, 1, 0.8, 0.65, and 0.5 mm) are mounted and the whole molding (with KGDs, RDLs, and solder balls) is diced into individual packages. Figure 7(b) shows the image of cross-sectional RDL while Fig. 7(c) shows the image of longitudinal RDL. FOWLP has the potential for substantial growth, however, it is out of the scope of the present study.

2.4 C2 (Cu-Pillar With Solder Cap) Bumps. Because of higher pin-count and tighter pitch (smaller spacing between pads), there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [26] (e.g., Fig. 5(b)) and Cu-pillar with solder cap [27,28] (e.g., Fig. 3) can be a solution. The fabrication process is basically the same as that of the C4 bump except electroplating the Cu instead of solder as shown in step #5 on the lower right-hand side of Fig. 4. It is followed by electroplating the solder cap and then reflowing the solder with flux (Fig. 3 shows the Cu-pillar with solder cap and Fig. 5(b) shows the very tall Cu-pillar without solder cap). Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the Cu pillar with the solder cap bump and therefore, it is sometimes called a C2 (chip connection) bump. Besides being able to handle finer pitch, C2 bumps also provide better thermal and electrical performances than C4 bumps. This is because the thermal conductivity (W/m K) and electrical

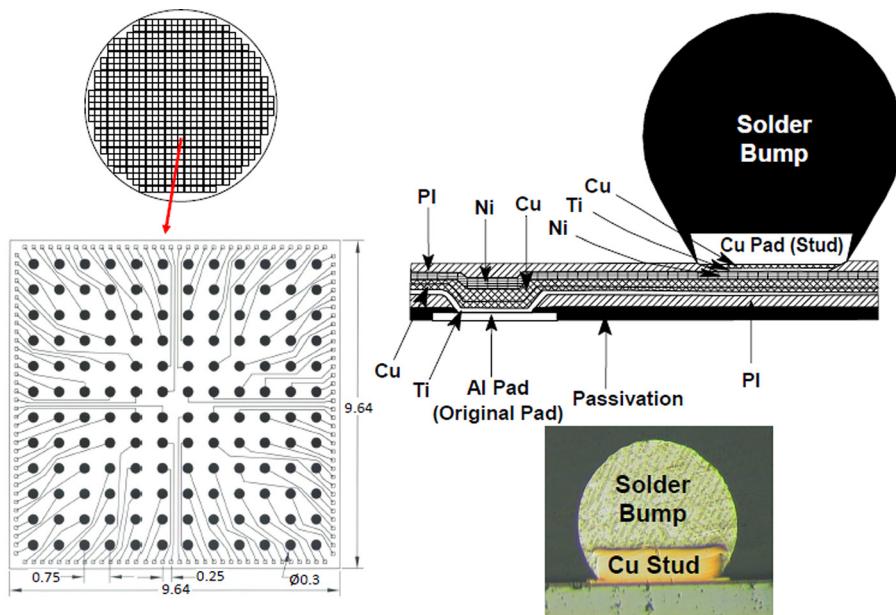


Fig. 6 Fan-in WLCSP

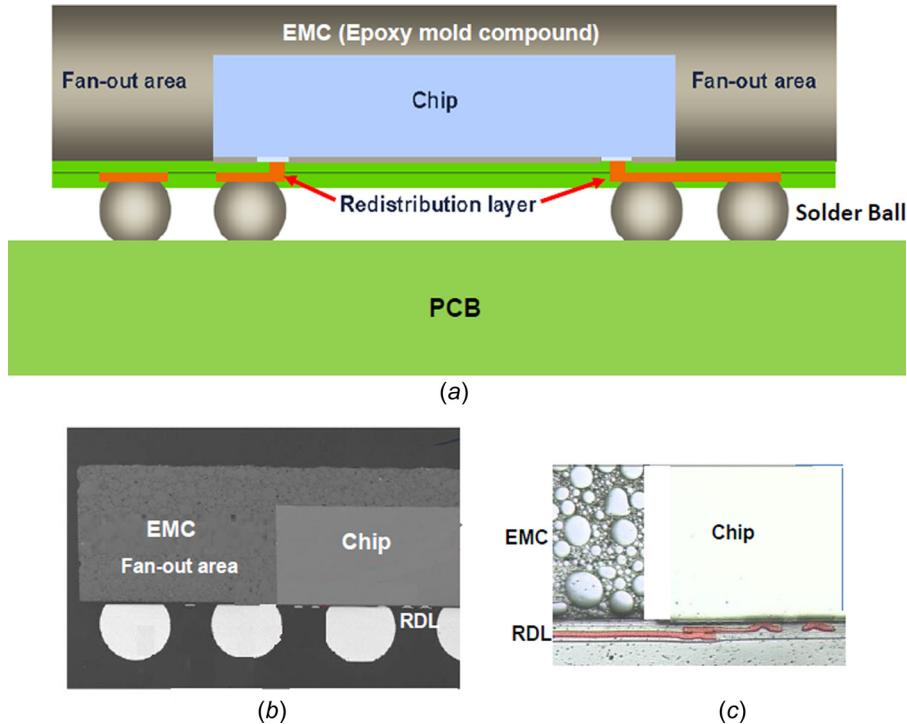


Fig. 7 FOWLP (a), (b) RDL (cross-sectional view), and (c) RDL (longitudinal view)

resistivity ($\mu\Omega \text{ m}$) of Cu (400 and 0.0172) are superior than those (55–60 and 0.12–0.14) of solder.

3 Flip Chip Package Substrate

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of the conventional low-cost build-up organic package substrates by increasing the number of build-up layers, fabricating thin-film layers on top of the build-up

layer, shrinking the dimensions of the metal line width and spacing, reducing the pad size and pitch, eliminating the core, making the BOL, and laminating the ETS. For silicon substrates, first come with the TSV-interposer and the future trend is for TSV-less interposer. Ceramic substrate [29–34] will not be discussed herein.

3.1 Surface Laminar Circuit (SLC) Technology. Almost 25 years ago, IBM in Japan at Yasu invented the SLC technology, Fig. 8 [35–37], which formed the basis of today's very popular

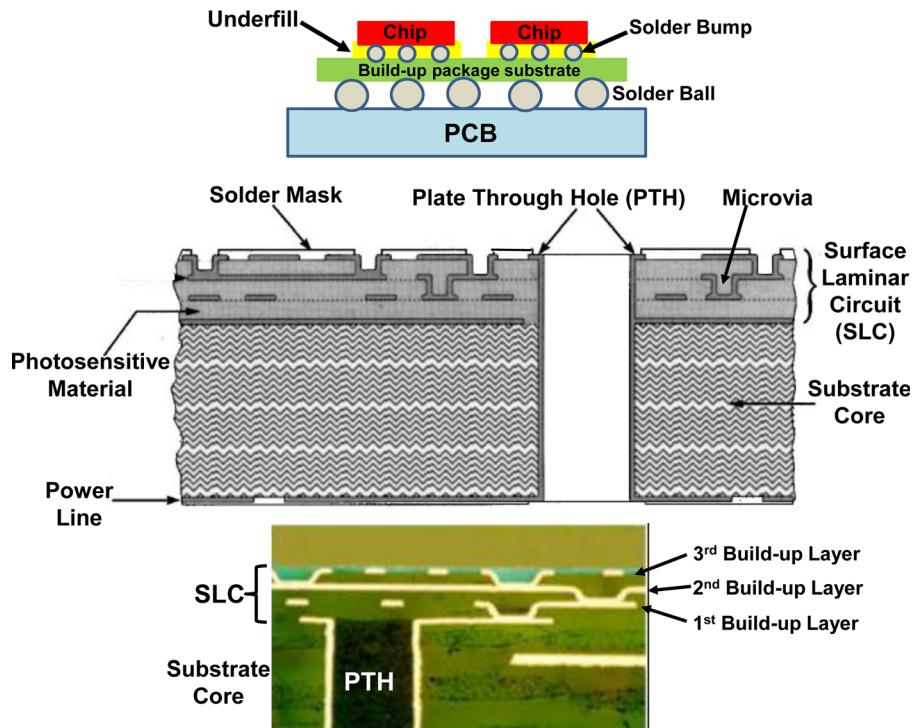


Fig. 8 IBM's SLC for flip chip organic build-up package substrate

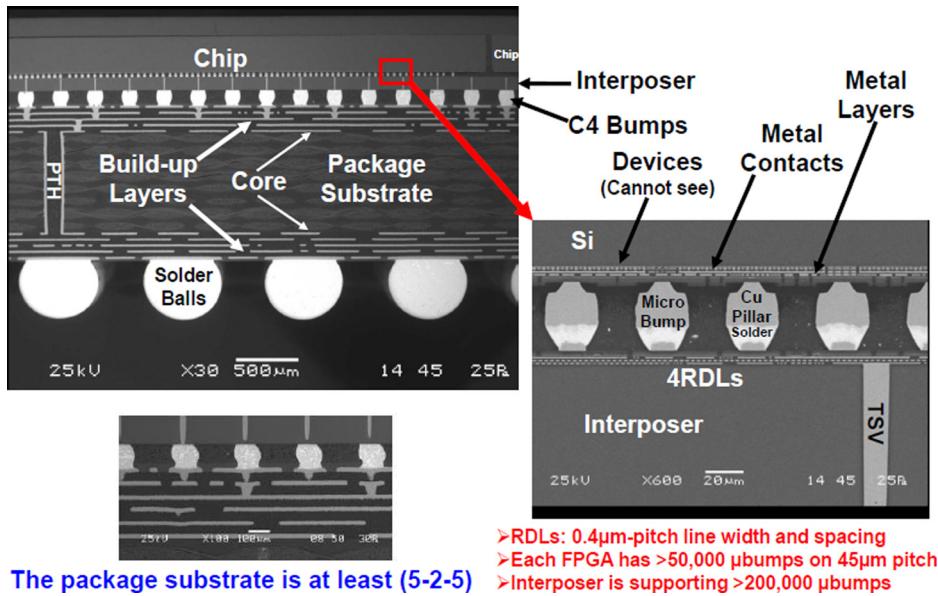


Fig. 9 Xilinx/TSMC's TSV—interposer (CoWoS)

low-cost organic package substrates with build-up layers vertically connected through microvias [38] to support flip chips. There are two parts of the SLC technology: one is the core substrate and the other is the SLC for the signal wiring. The core substrate is made by the ordinary glass epoxy panel. However, the SLC layers are sequentially built up with the dielectric layers made of photo sensitive epoxy and the conductor plane of copper plating (semi-additive technique). In general, a package substrate with twelve layers (e.g., two core-layers and ten build-up layers (5-2-5)) and 10 μm -line width and spacing is more than adequate to support most of the chips.

3.2 TSV-Interposers. In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced field programmable gate array (FPGA), even a twelve build-up layers (6-2-6) package substrate is not enough to support the chips and a TSV interposer is needed [39–51]. For example, Fig. 9 shows the Xilinx/TSMC's FPBG chip on wafer on substrate (CoWoS) [48–50]. It can be seen that the TSV (10 μm -diameter) interposer (100 μm -deep) has four top RDLs: three Cu damascene layers and one aluminum layer. The 10,000+ of lateral interconnections between FPGA chips are connected mainly by the 0.4 μm -pitch (minimum) RDLs of the interposer. The minimum thickness of the RDLs and passivation is $\sim 1 \mu\text{m}$. Each FPGA has more than 50,000 microbumps (200,000+ micro bumps on the interposer) at 45 μm pitch as shown in Fig. 9.

3.3 TSV-Less Interposer—Xilinx/SPIL's Silicon-Less Interconnect Technology (SLIT). So far, TSV-interposer is very expensive [7–9]. In order to lower the cost, enhance the electrical performance, and reduce the package profile, in 2014 Xilinx/SPIL proposed a TSV-less interposer for the sliced FPGA chips called SLIT [52]. The right-hand corner of Fig. 10 shows the new packaging structure. It can be seen that the TSVs and most of the interposer are eliminated and only those four RDLs are kept to perform, mainly, the lateral communication of the FPGA chips.

The process flow of TSV-less interposer is shown in Fig. 11. It starts off by fabricating the RDLs [45,53] on a bare silicon wafer, Fig. 11(a). It is followed by chip-to-wafer (the FPGA chip to the silicon wafer with RDLs) bonding, Fig. 11(b), and underfilling/curing, Fig. 11(c). Then, over mold the whole wafer with EMC, Fig. 11(d). It is followed by backgrinding the over mold to expose the backside of the chips and attaching an optional reinforcement wafer on the backside of the chips, Fig. 11(e). Then, backgrind

the silicon wafer, Fig. 11(f). It is followed by passivation, photoresist, mask, patterning, etching, passivation, sputtering TiCu, photoresist, mask, and patterning, Fig. 11(g). Finally, Cu contact-pad plating, Fig. 11(h), photore sist striping, TiCu etching, and C4 wafer bumping are performed, Fig. 11(i).

Depending on the line-width/spacing of RDLs' conductive wiring, the fabrication method of RDLs can be either by using a polymer for the dielectric layer and Cu plating of the conductive wring (line-width/spacing $\geq 5 \mu\text{m}$), or by using plasma enhanced chemical vapor deposition to make the SiO_2 dielectric layer and Cu damascene + chemical-mechanical polishing (CMP) to make the conductive wring (line-width/spacing $< 5 \mu\text{m}$) [45,53].

In 2016, SPIL/Xilinx published a similar paper [54] with more characterization results such as warpage data and called it non-TSV interposer (NTI).

3.4 TSV-Less Interposer—Amkor's Silicon Interposer-Less Integrated Module (SLIM). In 2015, Amkor announced a very similar technology to SLIT and is called SLIM [55].

3.5 TSV-Less Interposer—ASE's Fan-Out Wafer-Level Chip-on-Substrate (FOCoS). In 2016, ASE [56] proposed to use the FOWLP technology (chip-first and die-down on a temporary wafer carrier and then over molded by the compression method) to make the RDLs for the chips to perform lateral communications as shown in Fig. 12, and is called FOCoS. Wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate via an UBM and the C4 bump as shown in Fig. 12.

3.6 TSV-Less Interposer—Intel's Embedded Multidie Interconnect Bridge (EMIB). In September 2012, Intel proposed an EMIB [57] to replace the TSV-interposer. The lateral communication between the chips will be taken care of by the silicon embedded bridge and the power/ground and some signals will go through the organic package substrate to the PCB as shown in Fig. 13. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB and the other is to make the substrate with EMIB.

For making the EMIB, first build the RDLs (including the contact pads) on a Si-wafer by either polymer + ECD or Cu damascene + CMP methods [53]. Then, thin down the wafer to $\sim 60 \mu\text{m}$.

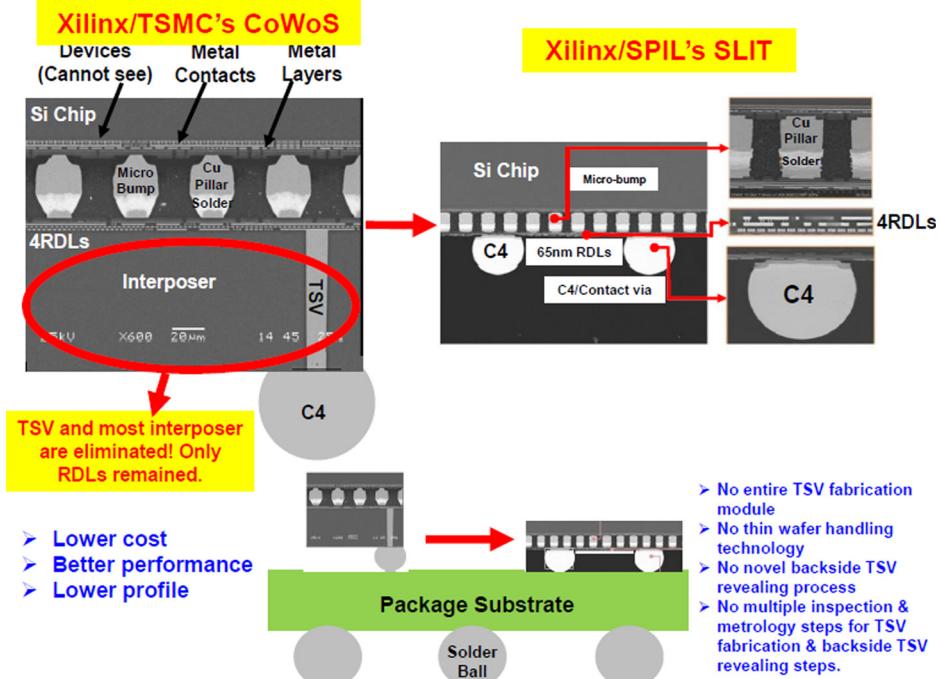


Fig. 10 TSV-less interposer—Xilinx/SPI's SLIT

Finally, attach the non-RDL side of the Si-wafer to a die-attach film and then singulate the Si-wafer. We have the EMIB.

For making the substrate with EMIB, first place the singulated EMIB with die-attached film on top of the Cu foil in the cavity of the substrate, Fig. 14(a). It is followed by laminating a resin film on the whole organic package substrate. Then, drilling (on epoxy resin) and Cu plating to fill the holes (vias) are done to make connections to the contact pads of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown Fig. 14(b). Then, it is followed by laminating another resin film on the whole substrate and drilling (on resin) and Cu plating to fill the holes and make contact pads (Fig. 14(c)). (Smaller pads on finer pitch are for microbumps while larger pads on gross pitch are for ordinary bumps.) The organic package substrate with EMIB is ready for bonding of the chips as shown in Fig. 14(d).

3.7 TSV-Less Interposer—ITRI's Through-Silicon Hole (TSH). On August 16, 2012, ITRI proposed the use of a TSH-interposer to replace the TSV-interposer [58,59]. Figure 15 schematically shows a TSH-interposer supporting a few chips on its top and bottom sides. The key feature of TSH-interposers is not metallization in the holes and the dielectric layer, barrier and seed layers, via filling, CMP for removing overburden copper, and Cu revealing are eliminated. Comparing with the TSV-interposers, TSH-interposers only need to make holes by either laser or deep reactive-ion etching on a piece of silicon wafer. Just like the TSV-interposers, RDLs are needed by the TSH-interposers.

The TSH-interposers can be used to support the chips on its top side as well as bottom side. The holes can let the signals of the chips on the bottom-side transmit to the chip on the top side (or vice versa) through the Cu pillars and solders. The chips on the same side can communicate to each other with the RDLs of the TSH-interposer. Physically, the top and bottom chips are connected through Cu pillars and micro solder joints. In addition, the peripherals of all the chips are soldered to the TSH-interposer for structural integrity to resist shock and thermal conditions. In addition, the peripherals of the bottom side of the TSH-interposer have ordinary solder bumps that are attached to a package substrate.

The test vehicle is shown in Fig. 16(a). It can be seen that it consists of a TSH-interposer, which is supporting a top-chip with

Cu pillars and a bottom-chip with UBM and solder. The interposer module is connected to a package substrate and then attached to a PCB. Figure 16(b) shows the X-ray images of the final assembly. It can be seen that: (a) the Cu pillars are not touching the side-wall of the TSH-interposer and (b) the Cu pillars are almost at the center of the TSH. It has been shown in Ref. [59] that the electrical performance of the TSH-interposer is better than that of the TSV-interposer. Also, the structural integrity of the TSH-interposer assembly has been demonstrated by drop and thermal cycling tests [59].

3.8 TSV-Less Interposer—Shinko's Integrated Thin-Film High Density Organic Package (i-THOP). In 2013, in order to replace the TSV-interposer, Shinko proposed to make thin-film layers on top of the build-up layer of a package substrate. Figure 17 shows Shinko's i-THOP substrate [60,61] for high performance applications. It is a 4+(2-2-3) test vehicle, which means there is a two-layer metal core, three build-up metal layers at the bottom (PCB) side, two build-up metal layers on the top (chip) side, and the first number "4" represents that there are four thin-film Cu wiring layers (RDLs) on the surface of the top build-up layer. The thickness, line width, and spacing of the thin-film Cu RDLs can be as small as 2 μm . The thin-film Cu RDLs are vertically connected through a 10 μm via, as shown in Fig. 17. The surface Cu pad-pitch is 40 μm and the Cu pad diameter is 25 μm with a height of 10–12 μm . The i-THOP substrate passed the warpage and reliability tests and there was no via delamination observed [60].

In 2014, Shinko demonstrated that [61] ultrafine pitch flip chips can be successfully assembled on the i-THOP substrate. Figure 18 schematically shows the two chips' lateral communications by the 2 μm line width/spacing RDLs of the two thin-film layers, which are built on top of the 1-2-2 build-up organic substrate, i.e., 2+(1-2-2). Figure 18 shows the 40 μm pitch microbumps (Cu-pillar + Ni + SnAg) of the test chips and the 40 μm pitch flip chip bonding pads (25 μm -diameter). Typical images of the cross section of the flip chip assembly with optimized conditions are shown in Fig. 19. It can be seen that good solder joints are confirmed at all areas of the assembly [61].

3.9 Coreless Substrate. Coreless substrate was first proposed by Fujitsu [62] in 2006. Figure 20 shows the comparison between

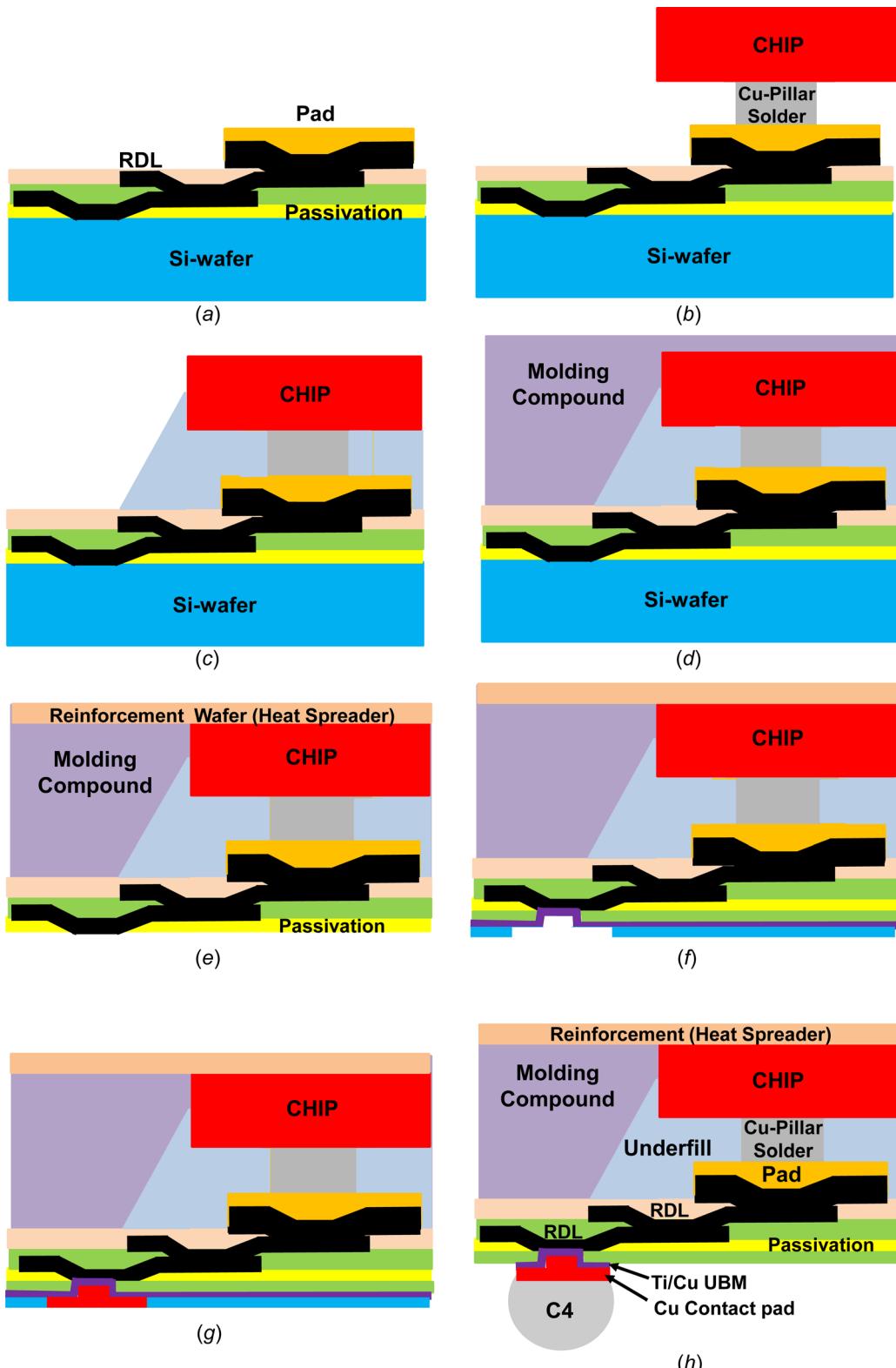


Fig. 11 Process flow for fabricating the SLIT (a) RDLs build-up on a Si-wafer, (b) chip to wafer bonding, (c) underfilling, (d) over molding the whole wafer, (e) reinforced wafer and backgrind the Si-wafer, (f) passivation, photoresist, mask, litho, etch passivation, sputter Ti/Cu, photoresist, mask, litho, (g) Cu plating, and (h) strip photoresist, etch Ti/Cu, C4 bumping

the conventional organic package substrate with build-up layers and the organic coreless package substrate. It can be seen that the biggest difference is that there is not a core in the coreless package substrate and all the layers of the coreless package substrate are the build-up layers [62–84].

The advantages of the coreless package substrate are [62–84]: (a) because of eliminating the core, the cost of the coreless substrate is lower; (b) by eliminating the core, higher wiring ability can be achieved; (c) better electrical performance because of good high-speed transmission characteristic; and (d) definitely smaller

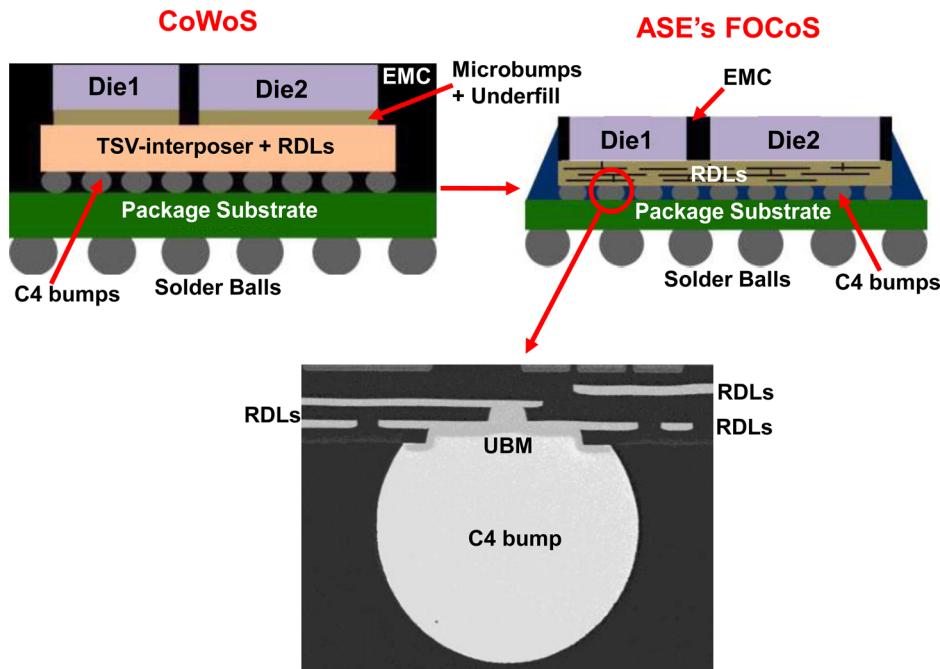


Fig. 12 TSV-less interposer—ASE's FOCoS

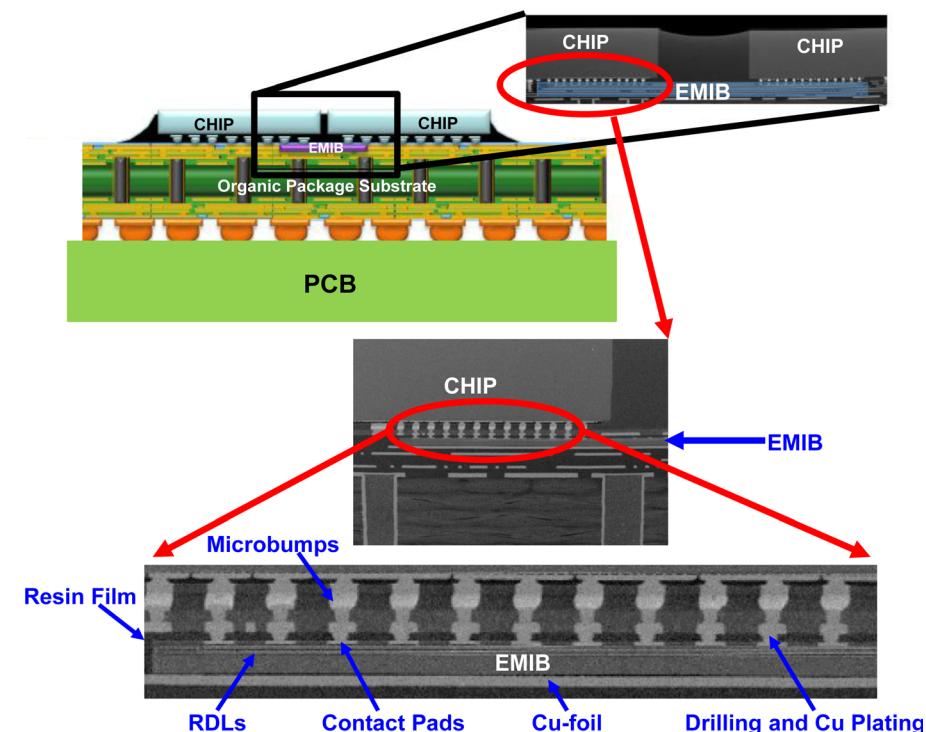


Fig. 13 TSV-less interposer—Intel's EMIB

form factor. On the other hand, the disadvantages are [62–84]: (a) because of eliminating the core, the warpage of the coreless substrate is larger; (b) easier to have laminate chipping; (c) poor solder joint yield because of less substrate rigidity; and (d) new manufacturing infrastructure is necessary. In 2010, Sony manufactured the first coreless package substrate for the cell processor of their PlayStation 3 [74].

Even though coreless substrates have many advantages, they are not popular because of the warpage control issue. One of the key factors affecting the warpage is the coefficient of thermal

expansion mismatch of substrate materials. Thus, a proper control of this factor will help reduce the warpage issue of coreless substrates. Another factor affecting the warpage is the package assembly. Thus, a proper package assembly warpage correction control (with vacuum and pressure) will help improve the warpage problem of coreless substrate.

3.10 BOL. BOL was first proposed by STATSChipPac [85–89] and was used by Qualcomm [90] and others [90–93]. A

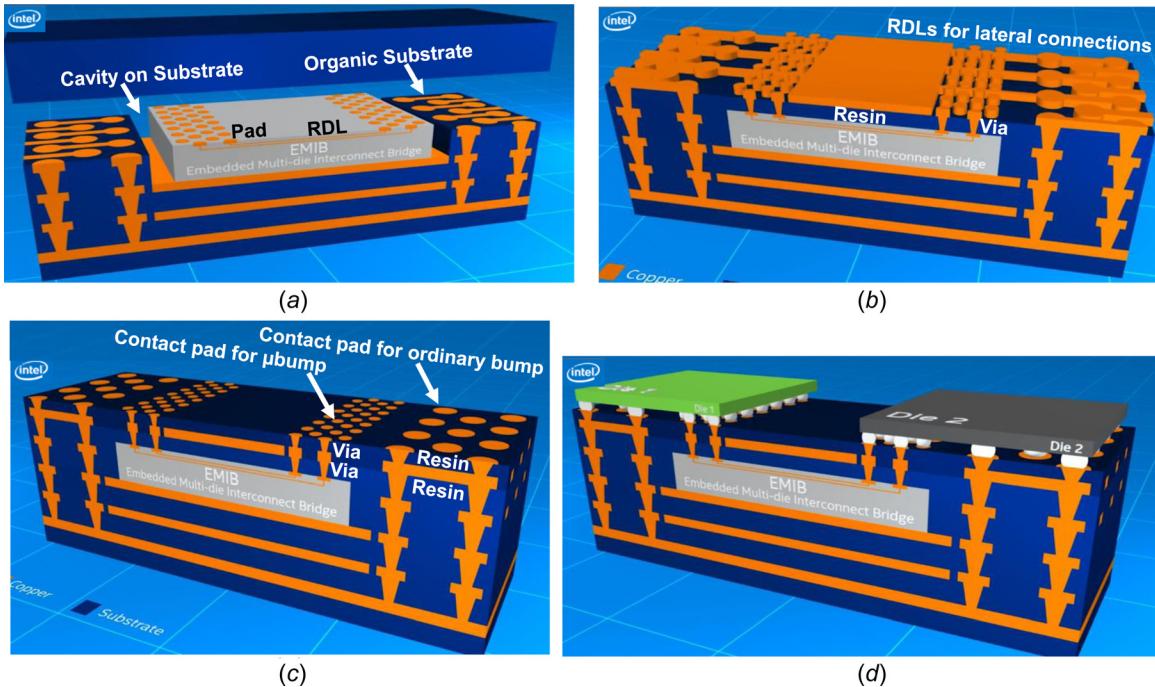


Fig. 14 Process flow for making Intel's EMIB

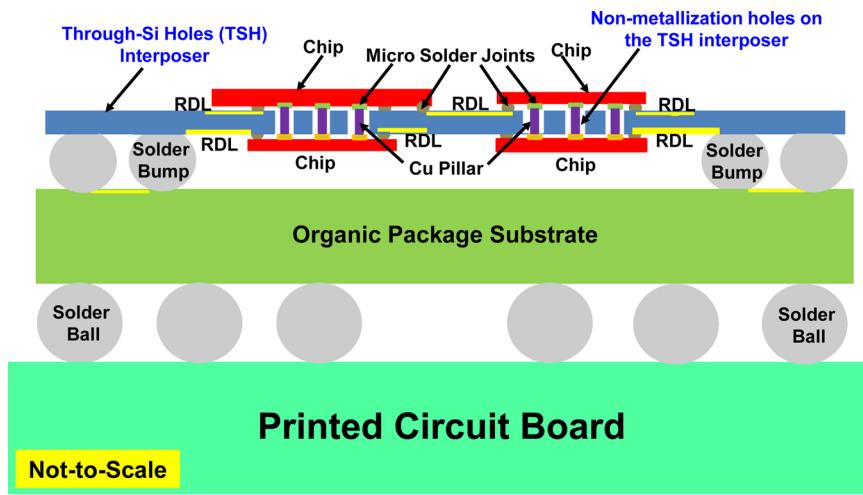


Fig. 15 TSV-less interposer—ITRI's TSH-interposer

conventional bump-on-capture pad (BOC) or simply bump-on-pad (BOP) flip chip organic substrate layout is shown in Fig. 21(a). It can be seen that the flip chip pads are on a 210 μm area array pitch in an solder mask (SR) defined configuration with one signal escape between bump pads resulting in an effective escape pitch of 105 μm . The BOL methodology is shown in Fig. 21(b); here, the landing pad on the substrate is merely the trace (lead) itself, or a slightly widened version of the trace which results in freeing up of enough routing space to allow routing an additional trace between bumps thereby resulting in an effective escape pitch of 70 μm without changing the design rules (trace width and space) of the substrate. The improved BOL structure is shown in Fig. 21(c). It can be seen that the bump pads are without any solder resist confinement, i.e., open SR [90]. The test vehicles, Cu-column on BOL, used in Ref. [90] are shown in Figs. 21(d) and 21(e). It can be seen that one trace between the 180 μm bump

pitch and up to two traces with the 200 μm bump pitch can be comfortably routed.

Typical cross sections of the perpendicular-to-BOL and longitudinal-to-BOL are shown in the upper portion of Fig. 22. A 3D slide finite element model showing the BOL, BOC (or BOP), and solder joint is shown in the middle of Fig. 22. The creep strain contours of the BOL solder joint are shown in the lower portion of Fig. 22 [93] and are too small to create solder joint reliability problem under most conditions.

3.11 ETS. ETS is one of the coreless substrates with fine line width/spacing embedding the top metal trace pattern into prepreg layer [94–98]. The process flow of ETS is shown in Fig. 23(a). It starts from a carrier board with a removable Cu foil. It is followed by using a typical electrolytic copper plating method to form the

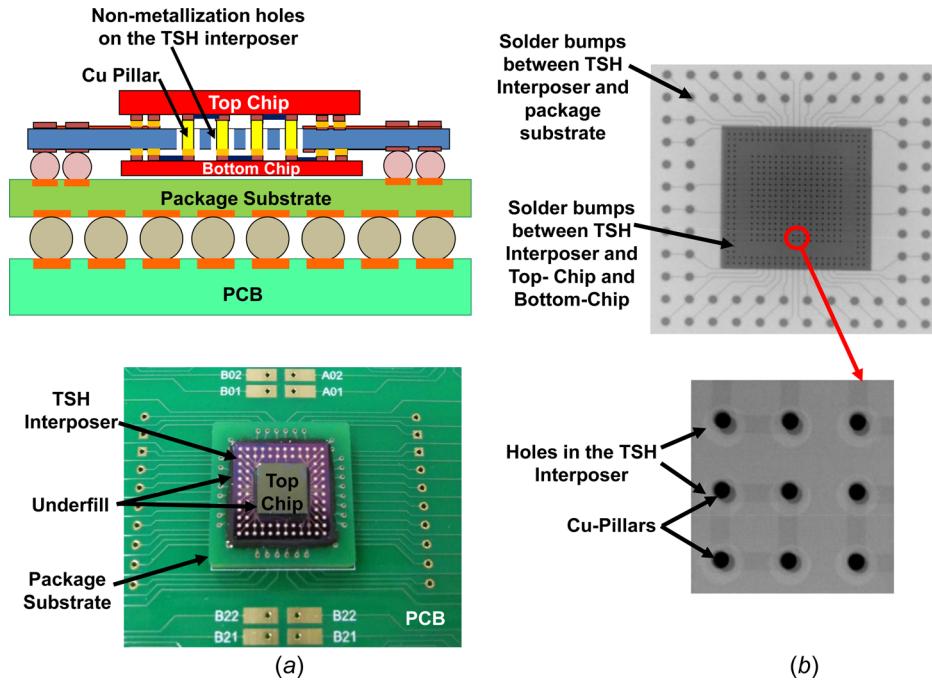


Fig. 16 (a) TSH-interposer test vehicle and (b) X-ray images of the final assembly

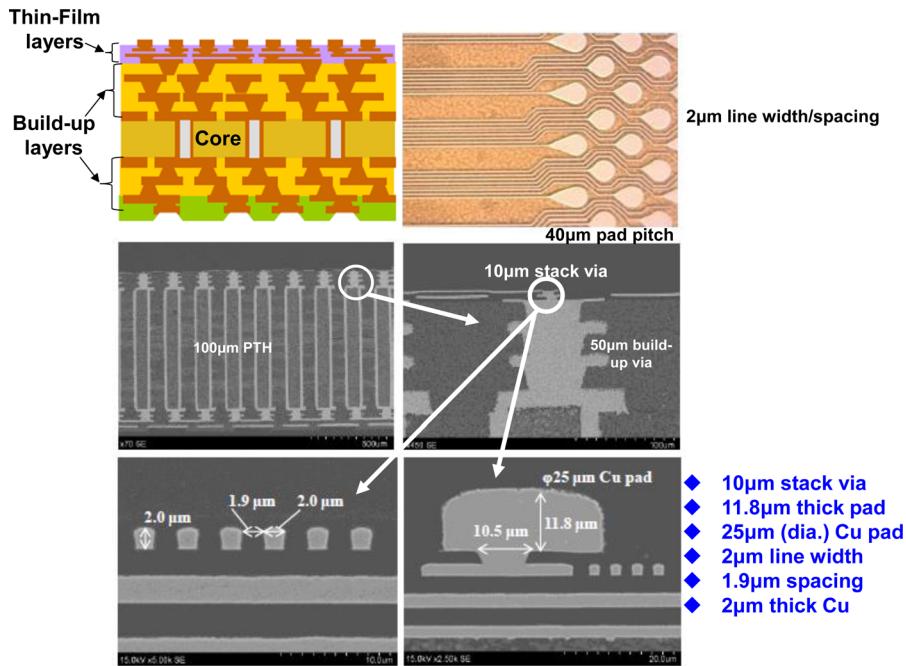


Fig. 17 TSV-less interposer—Shinko's i-THOP; a flip chip package substrate with thin-film layers on top of the build-up layer

first layer of copper pattern. Then, laminate a prepreg on the copper pattern. It is followed by laser via drilling, electroless copper coating, dry film laminating, exposing and developing, second layer copper pattern plating, stripping, and micro etching. Once all the copper pattern layers have been completed, the carrier board will be removed. Since the Cu foil is connected to the first copper pattern, micro etching is necessary before SR coating. After the SR opening process, it is completed by metal finishes treatment, e.g., organic solderability preservatives (OSPs). Figure 23(b) shows a cross section of a Cu-pillar flip chip on ETS assembly by SPIL [97]. Most line width/spacing of ETS in use today is 15 μm /

15 μm . However, 13 μm /13 μm line width/spacing is in production by Simmtech [98].

4 Flip Chip Assembly

Basically, there are two groups of flip chip assemblies: one is with an intermediate layer between the bonding pads/traces, and the other is not, i.e., nothing! Flip-chip assembly with intermediate layers such as solder for mass reflow and Cu-pillar with solder cap by TCB are called indirect bonding, which is the focus of this paper. Cu-to-Cu diffusion bonding, which does not have anything

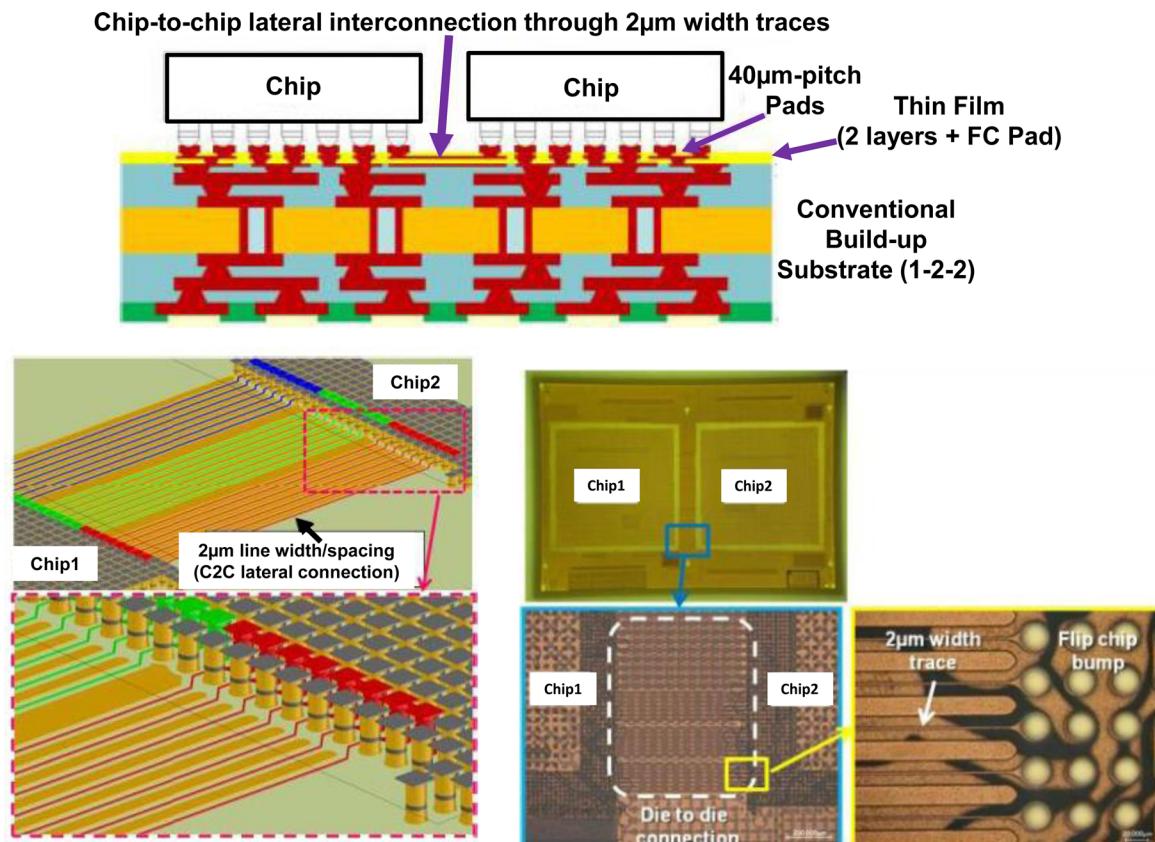


Fig. 18 Shinko's i-THOP test vehicle. Two thin film layers are built on top of the 1-2-2 package substrate.

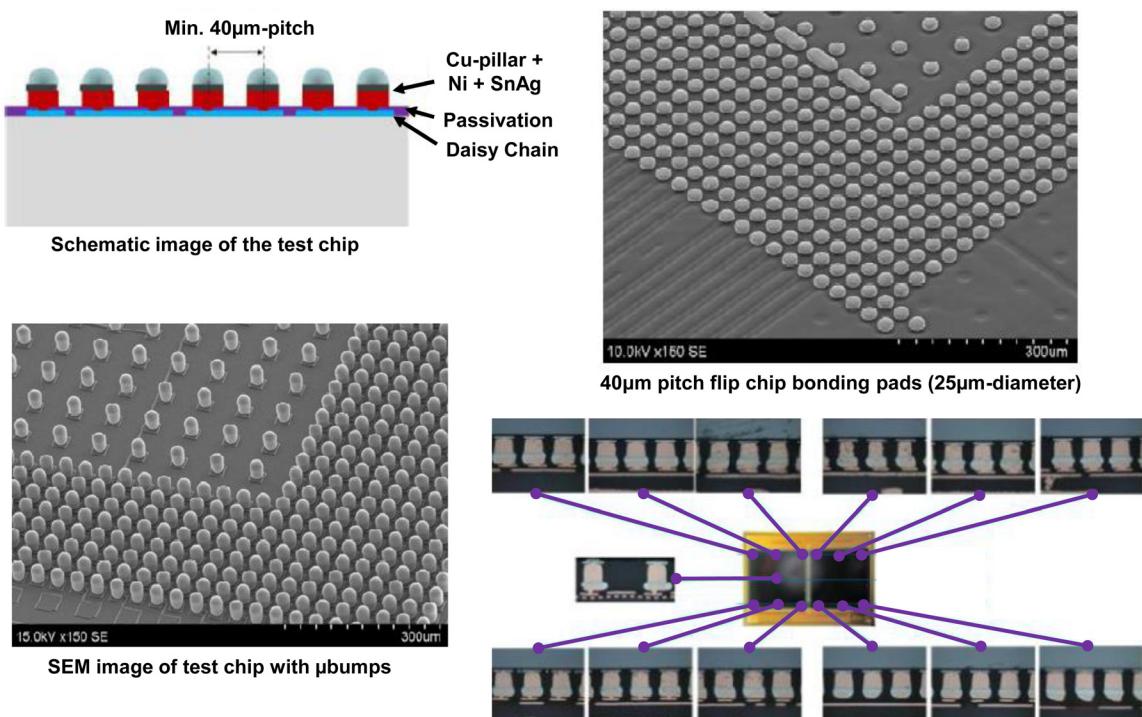


Fig. 19 C2 Microbumps at 40 μm -pitch. 40 μm -pitch flip chip bonding pads (25 μm -diameter) on the i-THOP substrate. Good solder joints from optimized condition.

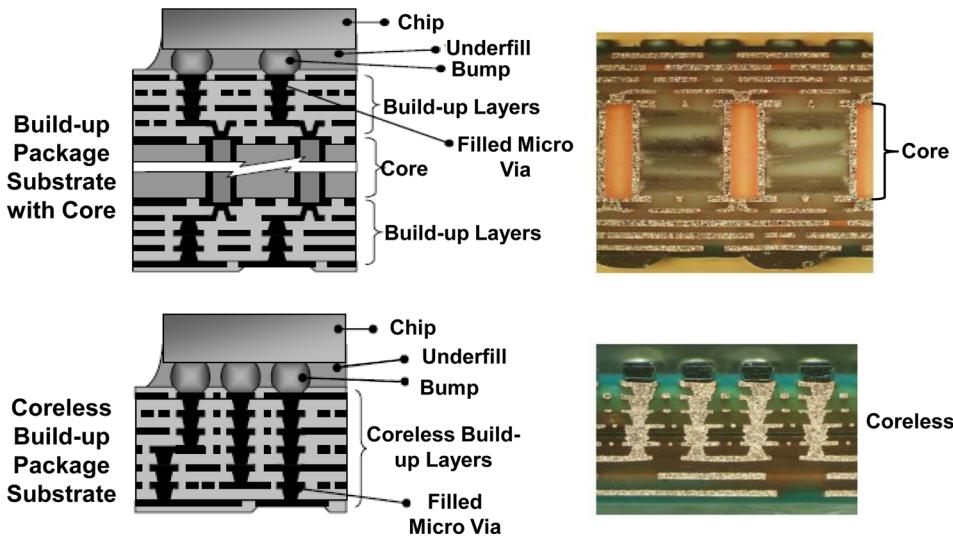


Fig. 20 (Top) flip chip on conventional build-up package substrate. (Bottom) flip chip on coreless substrate.

between the bonding pads/traces on the chip/wafer, is therefore, called direct bonding.

4.1 Cu-to-Cu TCB Direct Bonding. Cu-to-Cu diffusion bonding can go down to ultrafine pitch and pad size (the spacing between pads is 5 μm or less). In order to reduce the tendency to form native oxides that strongly affect the bonding quality and reliability, Cu-to-Cu is a TCB and usually operates at high

temperature ($\sim 400^\circ\text{C}$) and pressure and long process time (60–120 mins) [99–101], which are not good for throughput and the device reliability. On the other hand, Cu-to-Cu bonding at room temperature [102–108] leads to the highest throughput and the least amount of device reliability concerns, as well as very low costs. However, the drawbacks of room temperature bonding are the stringent requirements on: (a) pad/trace/wafer planarization, (b) surface treatment to ensure smooth hydrophilic surfaces for high quality bonding, and (c) the class of clean room (very

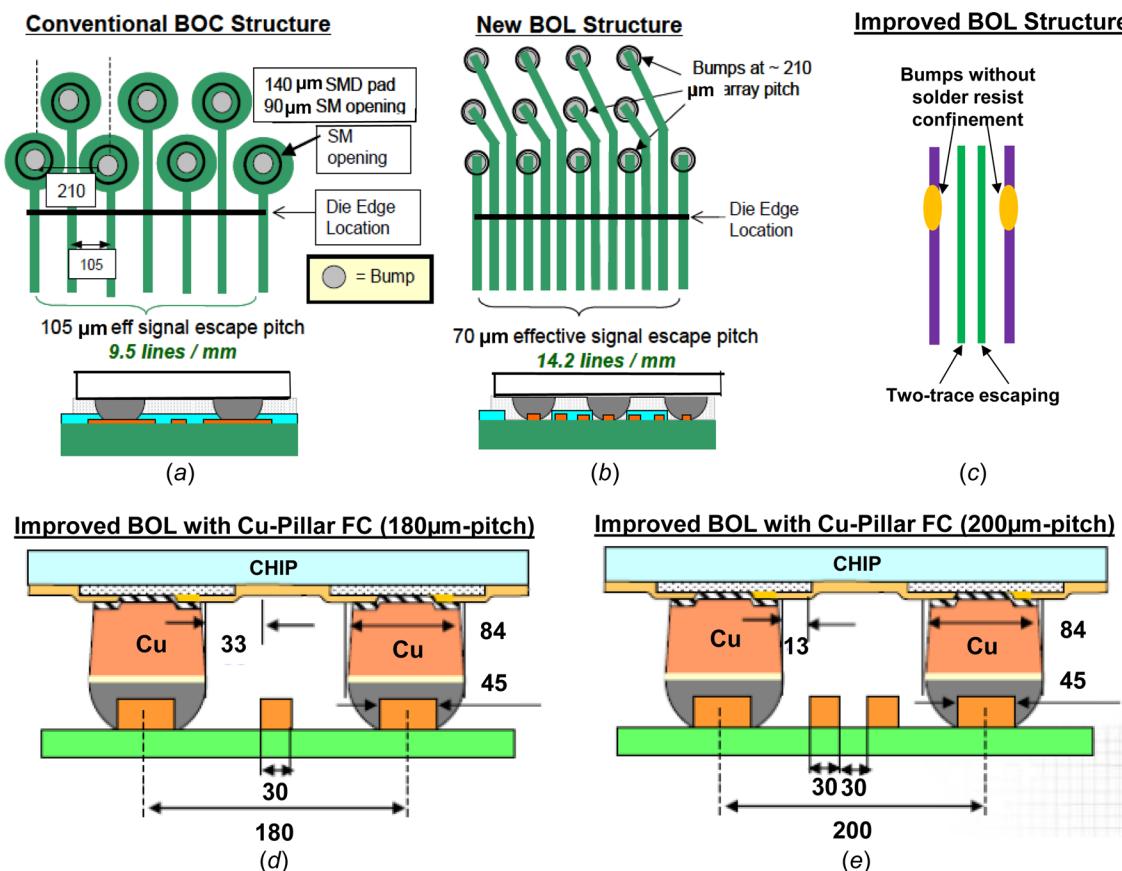


Fig. 21 BOL (a) conventional BOP, (b) new BOL, (c) improved BOL, (d) improved BOL with Cu-pillar FC (180 μm -pitch), and (e) improved BOL with Cu-pillar FC (200 μm -pitch)

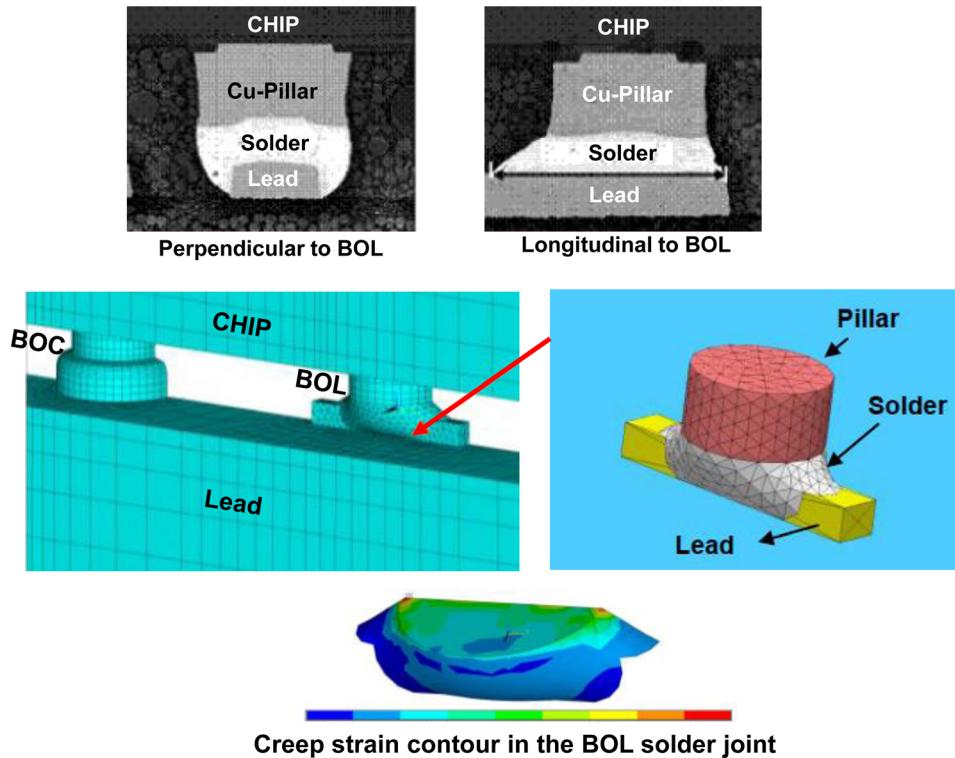


Fig. 22 Images of the perpendicular-to-BOL and longitudinal-to-BOL. Finite element models and creep strain contours in the BOL solder joint.

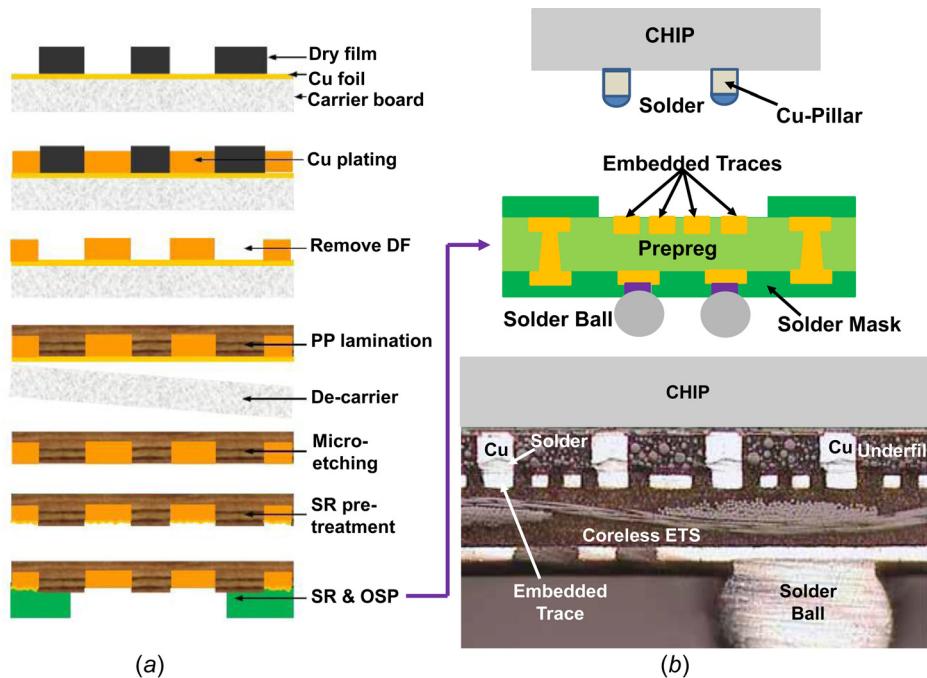


Fig. 23 (a) Process flow for fabricating the ETS and (b) flip chip with C2 bumps on ETS assembly

high required). Cu-to-Cu TCB is mainly for wafer-to-wafer (W2W) assembly process and is not in high-volume manufacturing yet, and thus, it is out of the scope of the present study.

4.2 C4 Solder Mass Reflow. Solder mass reflow has been used for flip-chip assembly for almost 50 years. Most of the solder

C4 bumps are mass reflowed on either silicon, ceramic, or organic substrates. The assembly process is very simple, Fig. 24(a): (i) use a look-up and look-down camera to identify the location of the bumps on the chip and the pads on the substrate; (ii) apply flux on either the C4 bumps, or the substrate, or both; and (iii) pick and place the C4 bumped chips on the substrate, then mass reflow with temperature H . Because of the surface tension of the C4

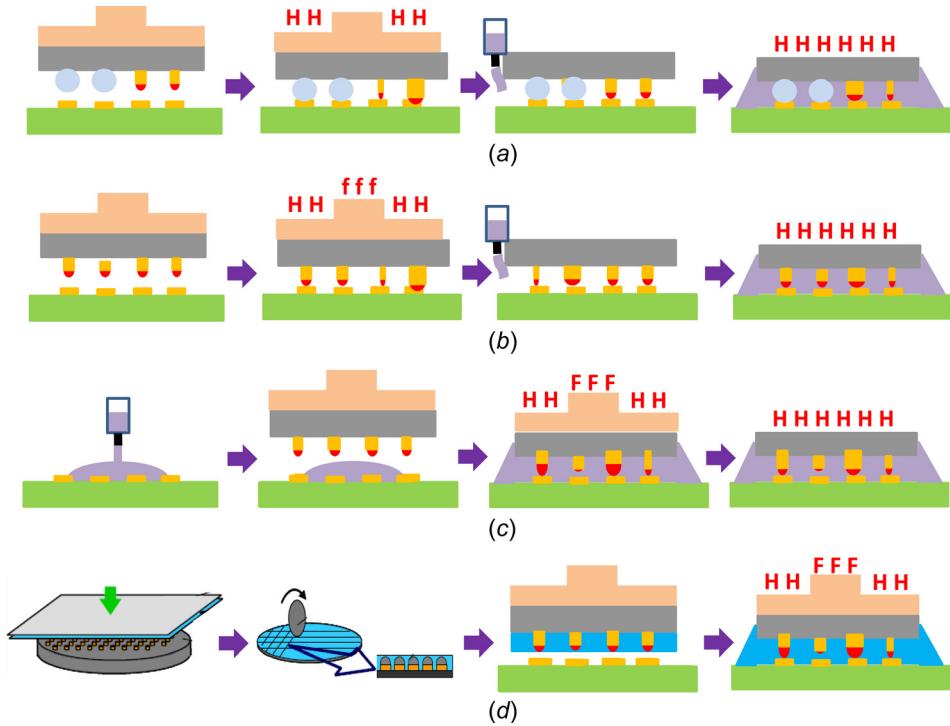


Fig. 24 Flip chip assembly with indirect bonding: (a) mass reflow of chips with C4 or C2 bumps with CUF, (b) TCB with low-force of chips with C2 bumps with CUF, (c) TCB with high-force of chips with C2 bumps with NCP, and (d) TCB with high-force of chips with C2 bumps with NCF

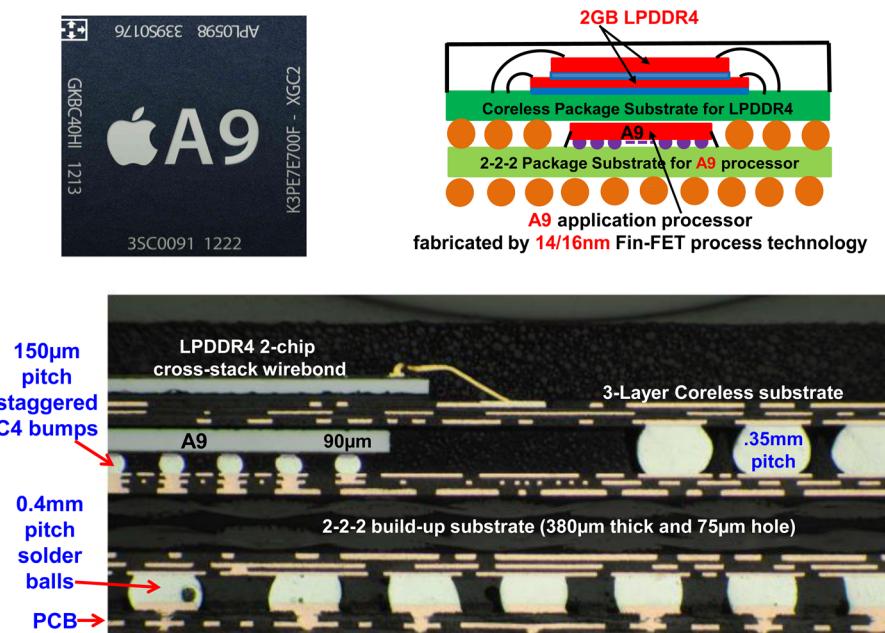


Fig. 25 Package-on-package (PoP) in Apple's smartphone. The C4 solder bumped flip chip is mass reflowed on a 2-2-2 package substrate.

solder bumps during reflow, the process is very robust (self-alignment). Figure 25 shows the cross section of iPhone 6 Plus (September 2015). It can be seen that the A9 application processor is housed in a PoP format and the solder bumped flip chip is mass reflowed on a 2-2-2 organic package substrate. In general, the spacing between the bumps on the solder mass reflow of C4 bumped chips can be as small as 50 µm.

4.3 C2 Solder Mass Reflow. In the past few years, solder mass reflow of C2 (Cu-pillar with solder cap) bumped chips on either silicon, ceramic, or organic package substrates has been tried for high pin-count and fine-pitch flip-chip assemblies. The assembly process, Fig. 24(a), is exactly the same as that of the C4 bumps, but the self-alignment characteristic is nowhere near the same, and thus, it is seldom being used. In general, the spacing

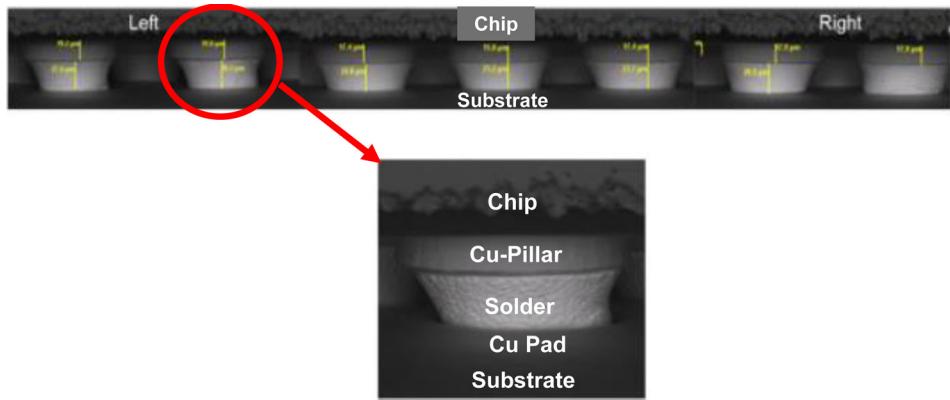


Fig. 26 Cross section of a C2 flip chip assembled on an organic package substrate by a TCB with low-force (CUF)

between the pillars on the solder mass reflow of C2 bumped chips can be as small as $25\text{ }\mu\text{m}$.

4.4 C2 TCB. In the past few years, TCB of chips with an intermediate layer such as C2 (Cu-pillar with solder cap) bumps on silicon, ceramic, or organic package substrates, has been attracting attention for high-density and ultrafine pitch flip chip assemblies. Basically, there are two methods, one is with low-bonding force and the other is with a high-bonding force.

4.4.1 C2 TCB With Low-Bonding Force. For the one with low bonding force, the assembly process is simple, Fig. 24(b): (i) first, use the look-up and look-down camera to locate the position of the C2 bumps on the chip and their corresponding pads on the substrate; (ii) apply flux on the solder cap or on the substrate or both; and (iii) pick-and-place the chip on the substrate and then apply temperature (H) to melt the solder and a low force (f) to hold the chip at a certain distance from the substrate. The above procedure is done one chip at a time and therefore, the throughput is low in comparison with the C2 solder mass reflow process. Figure 26 shows a typical cross section of a flip chip assembly with TCB with low force on C2 bumps [109]. In general, the spacing between the pillars on the C2 chip by TCB with a low-bonding force can be as small as $8\text{ }\mu\text{m}$.

4.4.2 C2 TCB With High-Bonding Force. For TCB with a high-bonding force on the C2 chip, the assembly process must be combined with the NCP or NCF underfill, which will be discussed in Sec. 5.

5 Underfill/Reliability

The reliability of flip chip solder joints is enhanced by the application of underfill [110–124], especially on organic substrate. Most underfills consist of low-expansion fillers such as fused silica (SiO_2) and a liquid prepolymer such as thermosetting resin (adhesive) that can be cured to a solid composite.

In 1987, Hitachi showed that with underfill, the thermal fatigue life of the flip chip solder joints on ceramic substrate increased [125]. In 1992, IBM at Yasu proposed the use of the low-cost organic substrate instead of the high-cost ceramic substrate for flip chip assemblies [35–37]. They showed that with underfill, the large thermal expansion mismatch between the silicon chip ($2.5 \times 10^{-6}/^\circ\text{C}$) and the organic substrate ($15\text{--}18 \times 10^{-6}/^\circ\text{C}$) is reduced substantially and the solder joints are reliable for most applications. This opened up the doors for today's very popular solder bumped flip chip on low-cost organic substrate packages used, e.g., in the processors of personal computers, notebooks, smartphones, tablets, etc.

Basically, there are two different procedures to apply the underfill, namely pre-assembly underfill and post-assembly underfill.

5.1 Post-assembly Underfill. For post-assembly underfill, the application of underfill is after the flip chip assembly, i.e., the flip chip is already on the substrate and the solder joints are already mass reflowed (either with C2 or C4 bumps) or low-force TCB with C2 bumps.

For post-assembly underfill, there are basically two methods, namely CUF [126–129] and MUF [130–134]. CUF is the first method that went into volume production [126–129]. For CUF, the underfill is dispensed by a needle or jet w/o vacuum assisted on one (or two) sides of the flip chip on substrate assembly. Because of capillary action, this underfill completely fills the space between the chips, solder joints, and substrates. The chip and the substrate are then firmly bonded by curing the underfill. CUF is performed one chip assembly at a time, thus, throughput is an issue.

Molded underfill was first proposed by Cookson Electronics [130] in 2000 and later by, e.g., Dexter [131], Intel [128], Amkor [132], STATSChipPAC [133], and LETI/STMicroelectronics [134]. For MUF, the modified EMC is transferred molding the chip and filling the gap between the chip, solder joints, and the substrate of the flip chip assembly. The encapsulant of the chip and the underfill are formed at the same time, which will increase the throughputs. However, the challenges of MUF are: (a) the flow of MUF between the chip and the substrate is usually assisted by vacuum, (b) the size of the silica filler of the EMC must be very small for flowability, (c) the cost of EMC for MUF is much higher than that for package molding, (d) package warpage is an issue due to the thermal expansion mismatch between the EMC, chip, and substrate, (e) the molding temperature is limited by the melting point of the solder joints, and (f) the standoff-height and pitch of the solder joints cannot be too small.

In order to increase the throughput of CUF and avoid the drawbacks of MUF, a method of post-assembly underfill has been proposed by Lau et al. [135], where a stencil is designed for printing the underfill material for flip chips on organic-panel and Si-wafer assemblies as shown in Fig. 27. It can be seen that: (a) a very small rectangular opening of the stencil is designed for each chip and it is located on one edge of the chip; (b) the stencil has a dry film underneath with many rectangular openings (one for each chip) and the size is a little larger than the chip size; and (c) there is a gap between the stencil and the backside of the chips. During printing, Fig. 27(b), the underfill will fill the opening of the stencil and fall into the space between one edge of the chip and the dry film. After printing (usually it only takes a few seconds), remove the assembly (Fig. 27(c)) from the stencil printer and place it on a hot plate ($\sim 120^\circ\text{C}$) for the underfill to flow between the chip, solder joints, and the substrate by capillary action (Fig. 27(d)). Finally, cure the underfill.

The test chip is shown in Fig. 28(a). It can be seen that the chip dimensions are $5\text{ mm} \times 5\text{ mm} \times 150\text{ }\mu\text{m}$ and there are 31×31

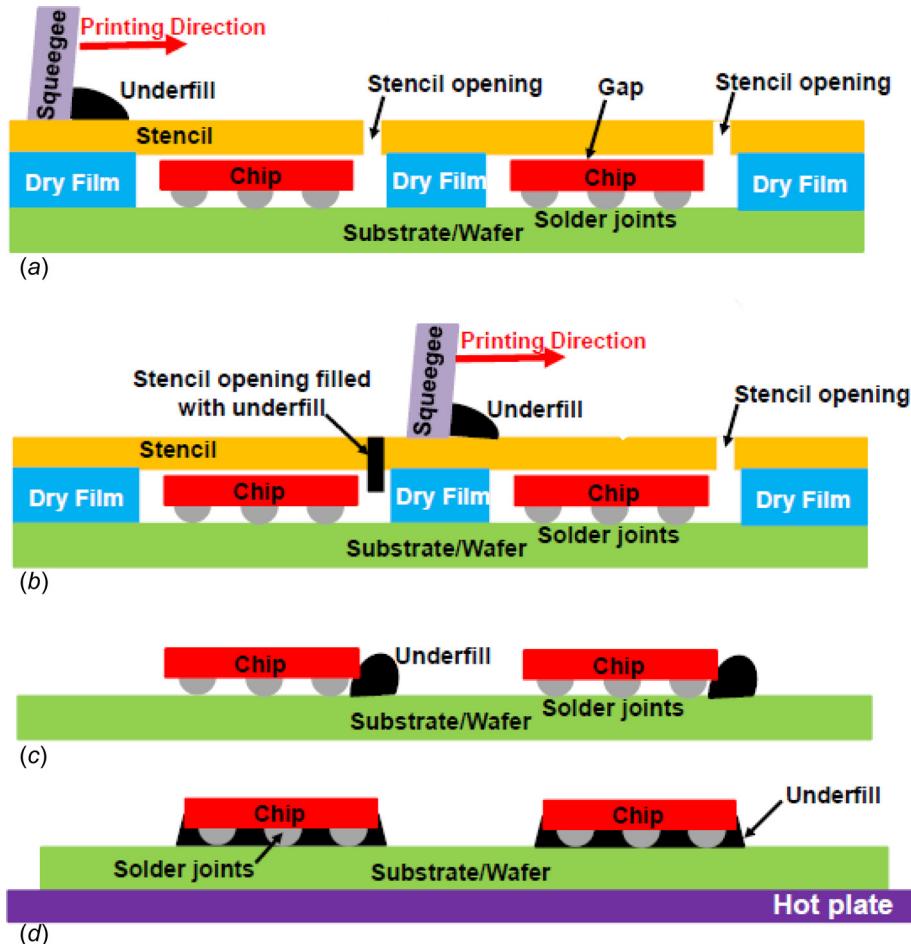


Fig. 27 A new stencil printing of underfill system. (a) Before printing, (b) during printing, (c) after printing, and (d) after capillary action.

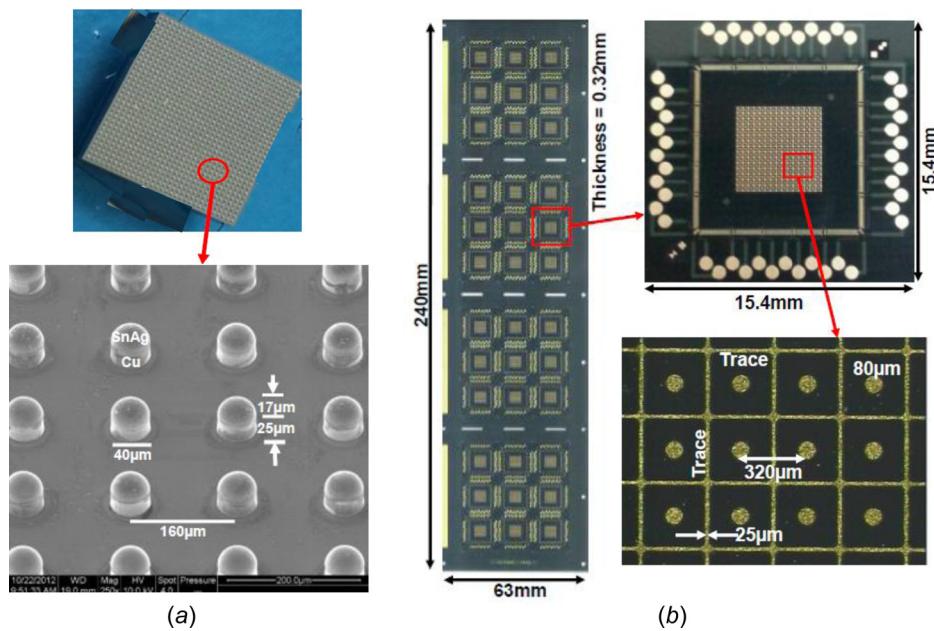


Fig. 28 (a) Test chip with Cu-pillar + SnAg solder cap and (b) organic-panel substrate

(961) Cu-pillar + SnAg solder cap bumps, which are on 160 μm -pitch. The diameter of the Cu-pillar is 40 μm and its height is 25 μm , while the SnAg solder cap is 17 μm . The test organic-panel substrate is shown in Fig. 28(b). The dimensions are

240 mm \times 63 mm \times 0.32 mm. There are 36 units and the dimensions for each unit are 15.4 mm \times 15.4 mm \times 0.32 mm. There are pads and traces on each chip site. The diameter of the OSP Cu pad is 80 μm and is on a 320 μm -pitch. The traces (leads) width is

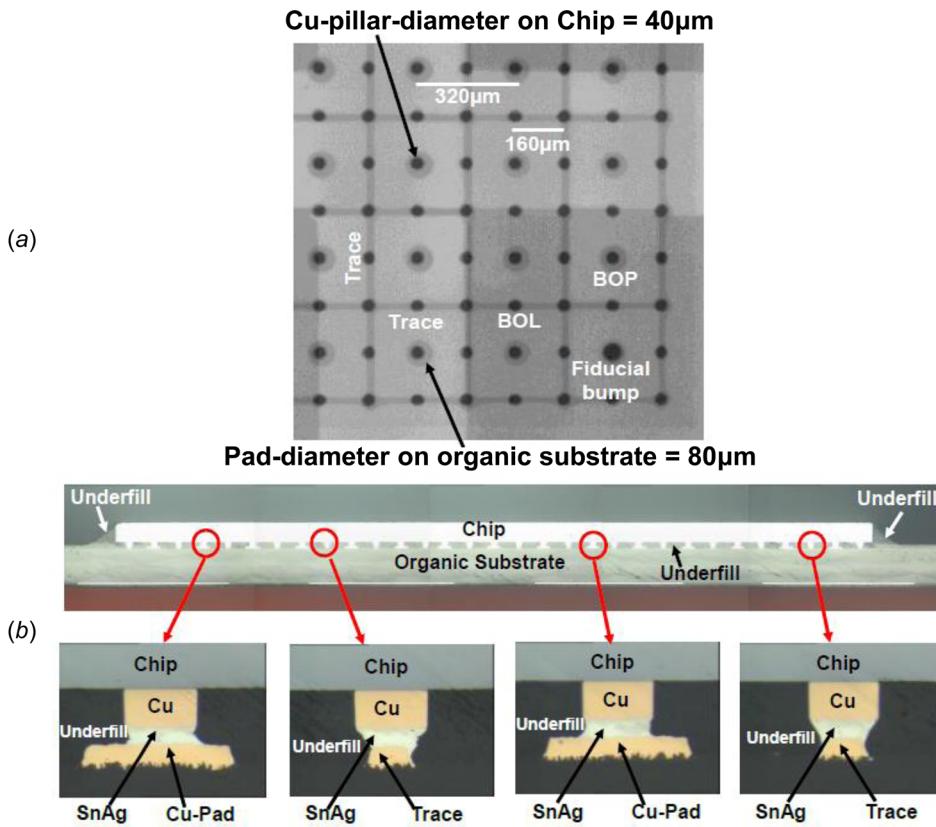


Fig. 29 (a) X-ray image and (b) a typical cross section of stencil printed underfill for flip chip on organic-panel assembly

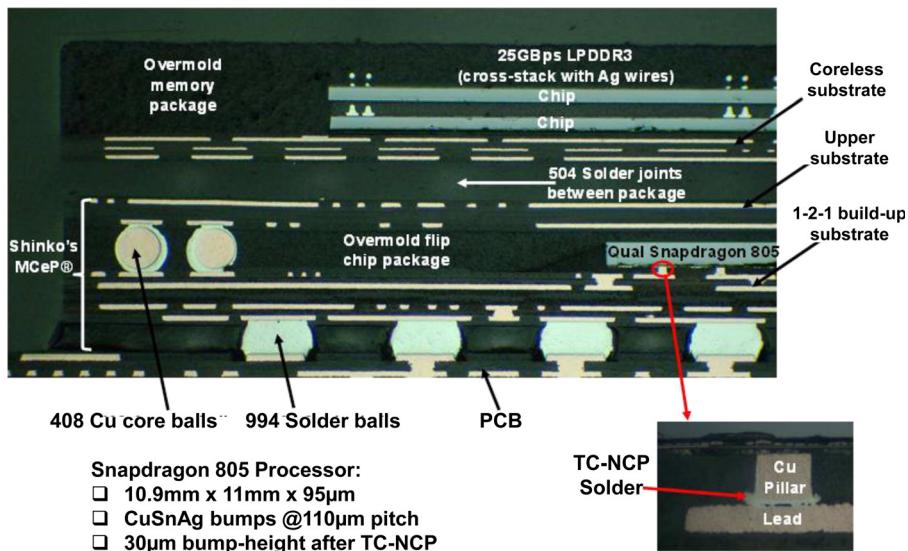


Fig. 30 PoP in Samsung's smartphone. The C2 flip chip is TCB with high-force on a package substrate (TC-NCP).

25 µm and will be BOL. Figure 29 shows a typical cross section of the stencil printed underfill for flip chip on organic-panel assemblies. It can be seen that: (a) the underfill fillets on the edges of the chip are clearly shown; (b) the underfill between the chip, solder joints, and substrate has no void and is properly processed; and (c) the solder joints on Cu-pad (BOP) and lead (BOL) of the organic substrate look very good.

5.2 Pre-Assembly Underfill. For pre-assembly underfill, the application of underfill is either on the substrate or wafer and is

before the flip-chip assembly. Solder reflow of the C4 bumps with underfill on substrates was first proposed by GIT [136] and is called NUF. High-bonding force TCB of the C2 bumps with non-conductive paste (TC-NCP) underfill on the substrate, Fig. 24(c) was first studied by Amkor [137] and has been used to assemble Qualcomm's SNAPDRAGON application processor for Samsung's Galaxy smartphone as shown in Fig. 30. The NUF and NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

By learning from the chip-on-glass technology, high-bonding force TCB of C2 bumps with nonconductive film underfill on

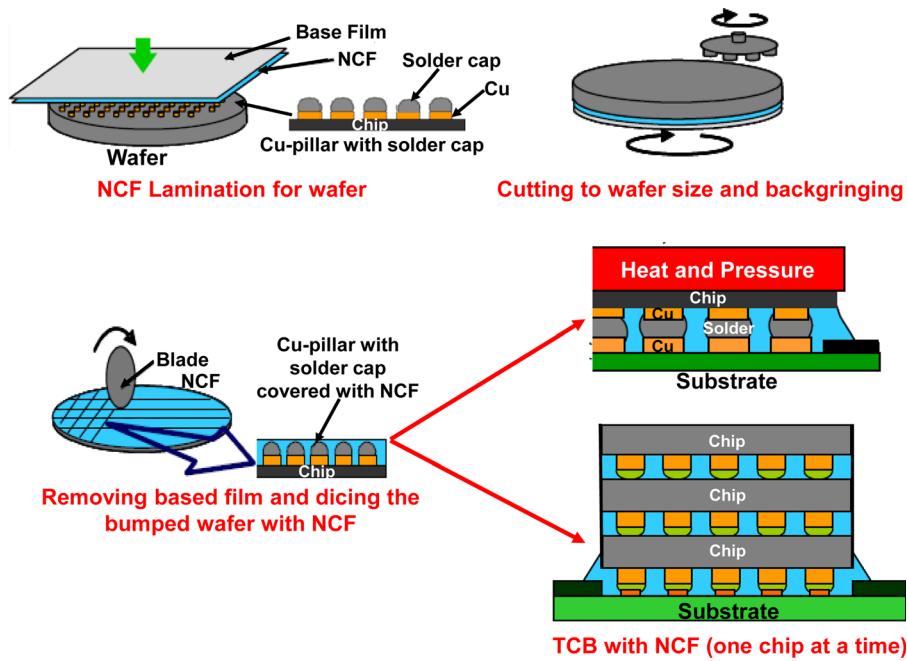


Fig. 31 Lamination of NCF on a C2 bumped wafer, dicing, and TCB of NCF flip chips one by one

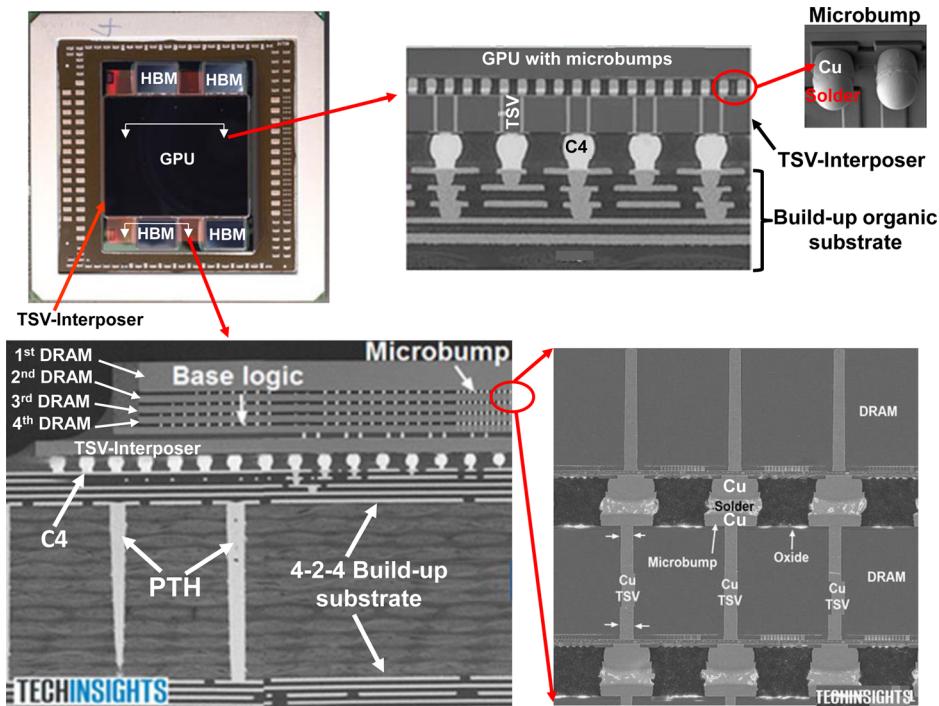


Fig. 32 AMD's graph card made by Hynix's HBM, which is TCB with high-force of the NCF DRAM chips one by one

wafers have been studied by, e.g., Sanyo [138], Hitachi [139,140], Tohoku [141,142], DOW [143], Hynix [144], KAIST/Samsung [145,146], Amkor/Qualcomm [147], and Toray [148–150] for 2.5D/3D IC integration [7–10]. Figure 31 shows the lamination of NCF on the Cu-pillar with a solder cap bumped wafer.

High-bonding force TCB of the C2 chips with NCF (after singulation from the laminated wafer) has been in production for 3D IC integration by Samsung on its TSV-based double data rate type 4 dynamic random access memory (DRAM), and by Hynix on the high bandwidth memory (HBM) of AMD's graphic processor unit

(GPU) code-named Fiji. The TSV-interposer is supporting the GPU and four-set of HBM, which is a stack of four DRAMs on a base logic, as shown in Fig. 32. This 3D memory cube is stacked by high-force TCB of the C2 chips with NCF one chip at a time and each chip takes ~10 s for the underfill film to gel, the solder to melt, the underfill film to cure, and the solder to solidify. Throughput is a problem!

In order to resolve this problem, Toray [149,150] proposed a collective bonding method which is shown in Fig. 33. It can be seen that the C2 chip with NCF is prebond (bond force = 30 N,

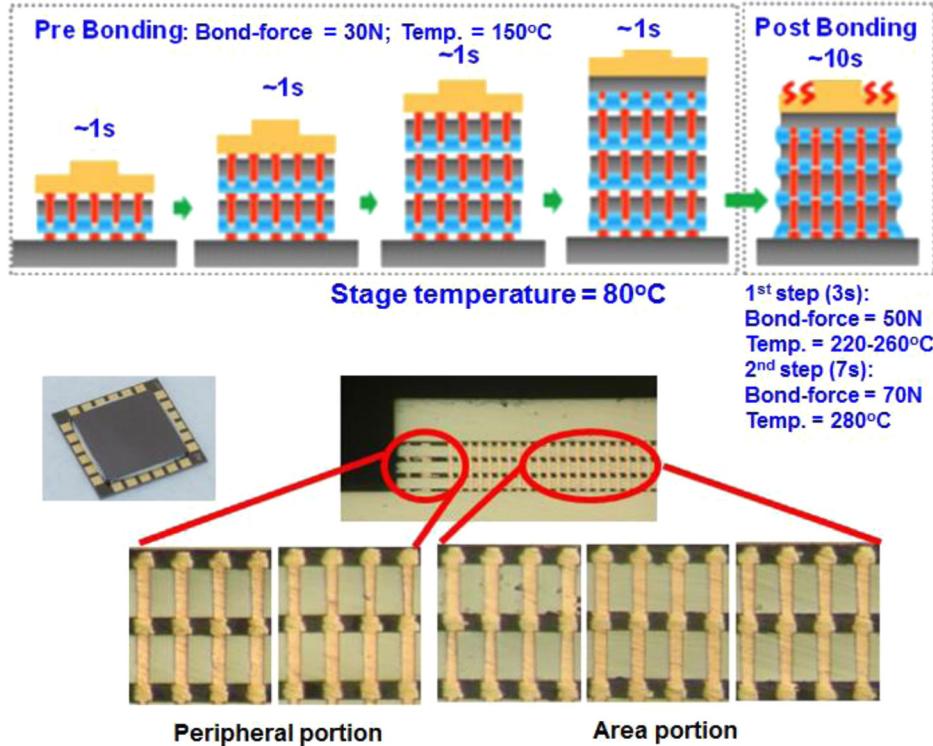


Fig. 33 Toray's collective TCB with high-force with NCF flip chips

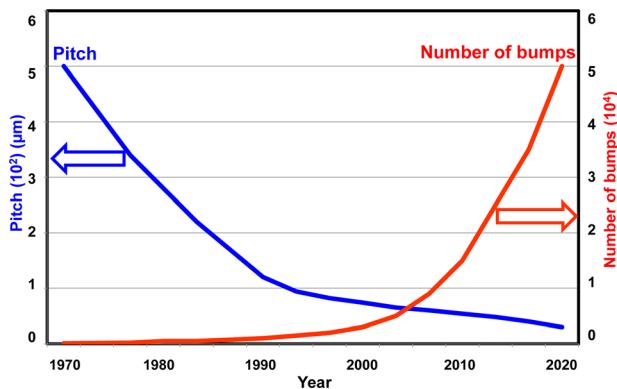


Fig. 34 Trend in flip chip bump and pitch

temperature = 150 °C, and time < 1 s) on a stage with temperature = 80 °C. For postbond (first step (3 s): bond-force = 50 N, temperature = 220–260 °C, second step (7 s): bond-force = 70 N, temperature = 280 °C) on a stage temperature = 80 °C. Thus, instead of using 40 s in stacking up four chips by the conventional method, it only takes less than 14 s by the collective method. Some images of the cross section of the proposed collective bonding method are shown in Fig. 33. Reasonable good joints are achieved with optimized conditions.

In general, the spacing between the pillars on the C2 chip with either NCP or NCF by TCB with high bonding force can be as small as 10 μm .

6 Summary and Recommendations

Wafer bumping, package substrate, assembly, and underfill for flip-chip technology have been investigated in this study. Some important results and recommendations are as follows:

- Flip chip technology (excluding Cu-to-Cu direct bonding) came from a long way. From the three-bump flip chip to

10,000-bump flip chip, and could be 50,000-bump flip chip by the year of 2020. Also, by that time, the flip-chip pitch could be as small as 30 μm as shown in Fig. 34.

- C2 bumps have better thermal and electrical performance and can go down to finer pitch (smaller spacing between pads) than C4 bumps. However, more research and development works should be done on relative performance characteristics, such as electromigration life, thermal fatigue life, signal speed, chip junction temperature, etc.
- The self-alignment characteristic (one of the most unique features of flip chip technology) of the C2 bumps is nowhere near the C4 bumps. Thus, mass reflow is usually applied to C4 bumped chips.
- C2 bumped chips are usually assembled by TCB with high-force, while low-force is sometime used.
- The advantages of TCB are for higher pin-count, finer pitch, thinner chips, higher-density, and thinner package substrates, and controlling warpage and die tilt. One of the drawbacks of TCB is throughput (compared with mass reflow).
- A package substrate with ten build-up layer (5-2-5) and 10 μm line width and spacing is more than adequate to support most of the flip chips. In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced FPGA, even a 12 build-up layer (6-2-6) package substrate is not enough to support the chips and a TSV interposer is needed.
- As of today, TSV-interposer is very expensive. In order to lower the cost, enhance the electrical performance, and reduce the package profile, TSV-less interposers such as the Xilinx/SPIL's SLIT, Amkor's SLIM, SPIL/Xilinx's NTI, ASE's FOCOS, Intel's EMIB, ITRI's TSH, and Shinko's i-THOP have been developed. This will be the trend in flip chip package substrate for high-density and performance applications.
- More research and development works should be done on innovative and low-cost ETS and coreless substrates for portable, mobile, and wearable applications.

- More research and development works should be done to effectively use the BOL technique to increase routing density, and thus, lower the cost and reduce the size of organic package substrate.
- For Cu-to-Cu direct diffusion bonding, the spacing between pads is $5\text{ }\mu\text{m}$ or less.
- For mass reflow of C4 bumped chips with either CUF or MUF, the spacing between bumps is as low as $50\text{ }\mu\text{m}$.
- For mass reflow of C2 bumped chips with either CUF or MUF, the spacing between Cu-pillars is as low as $25\text{ }\mu\text{m}$.
- For TCB with low-force of C2 bumped chips with either CUF or MUF, the spacing between Cu-pillars is as low as $8\text{ }\mu\text{m}$.
- For TCB with high-force of C2 bumped chips with either NCP or NCF underfills, the spacing between Cu-pillars is as low as $10\text{ }\mu\text{m}$.
- For the post-assembly underfill approach, the CUF or MUF is usually applied to flip-chip assemblies with mass reflow and TCB with low-bonding force methods.
- For the pre-assembly underfill approach, the NUF, NCP, or NCF is usually applied before flip-chip assemblies; NUF is with mass reflow and NCP or NCF is with high-force TCB. In general, the NUF and NCP are applied on the substrate and the NCF is laminated onto the C2 bumped wafer and then diced into individual chips.
- Toray's collective TCB with high-force method can be a potential high-throughput process for stacking C2 chips with laminated NCF.
- As pointed out in Ref. [45] that Cu-to-Cu W2W direct bonding is the right way to go for memory chips stacking and the industry should strive to make this happen! However, more research and development efforts should be placed on areas such as: cost reduction, design and process parameter optimization, bonding environment, W2W bonding alignment, wafer distortion, wafer bow (warpage), inspection and testing, contact performance, contact integrity, contact reliability, and yield issues.

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