Read-While-Write, Multiplexed, Burst Mode, Flash Memory

MX69V28F64

1. FEATURES

Characteristics

Burst Length
- Burst Mode - Continuous linear
- Linear burst length - 8/16 word with wrap around

Sector Architecture
- Multi-bank Architecture (8 banks)
- Read while write operation
- Four 16 Kword sectors on top/ bottom of address range
- 127 sectors are 64 KWord sectors

Power Supply Operations
- 1.8V for read, program and erase operations (1.70V to 1.95V)
- Deep power down mode

Performance

High Performance
- 30us - Word programming time
- 7.5us - Effective word programming time utilizing a 32 word Write Buffer at VCC level
- 2.5us - Effective word programming time of utilizing a 32 word Write Buffer at ACC level

Sector Erase Time
- 500ms for 16 Kword sectors
- 1000ms for 64 Kword sectors

Read Access Time
- Burst access time: 7ns (at industrial temperature range)
- Asynchronous random access time: 80ns
- Synchronous random access time: 75ns

Secure Silicon Sector Region
- 128 words for the factory & customer secure silicon sector

Power Dissipation
- Typical values: 8 bits switching, CL = 10 pF at 108 MHz, CIN excluded
- 20mA for Continuous burst read mode
- 30mA for Program/Erase Operations (max.)
- 30uA for Standby mode

Program/Erase Cycles
- 100,000 cycles typical

Data Retention
- 20 years

Hardware Features

- Supports multiplexing data and address for reduced I/O count.
- A15–A0 multiplexed as Q15–Q0 Sector Architecture

Hardware Sector Protection
- All sectors locked when ACC = VIL

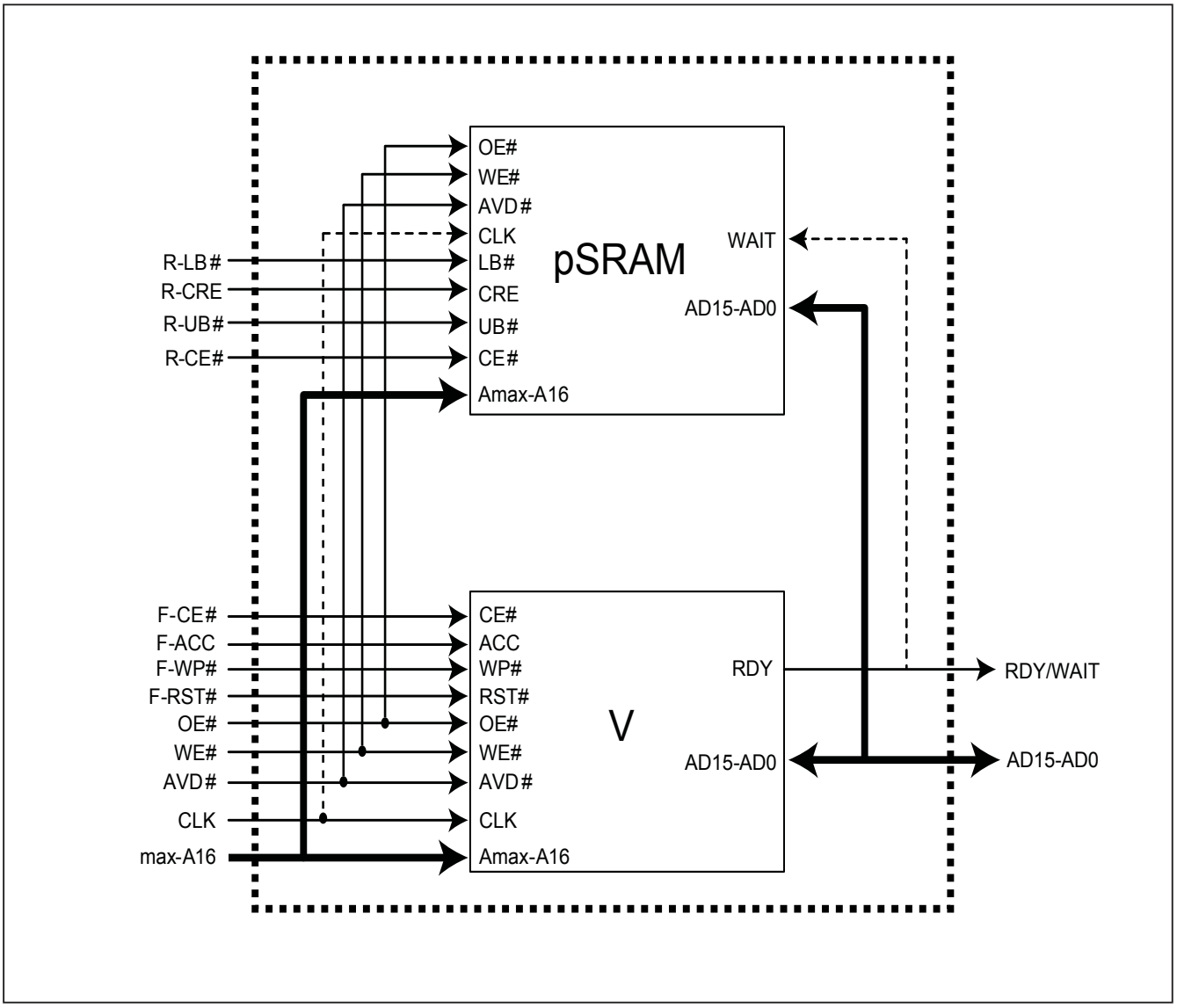
Package
- 56-Ball Thin FBGA (Fine-Pitch Ball Grid Array)
- REACH SVHC Free and RoHS Compliant

Handshaking Feature
- Allows system to determine the read operation of burst data with minimum possible latency by monitoring RDY.

2. Product Selection Guide

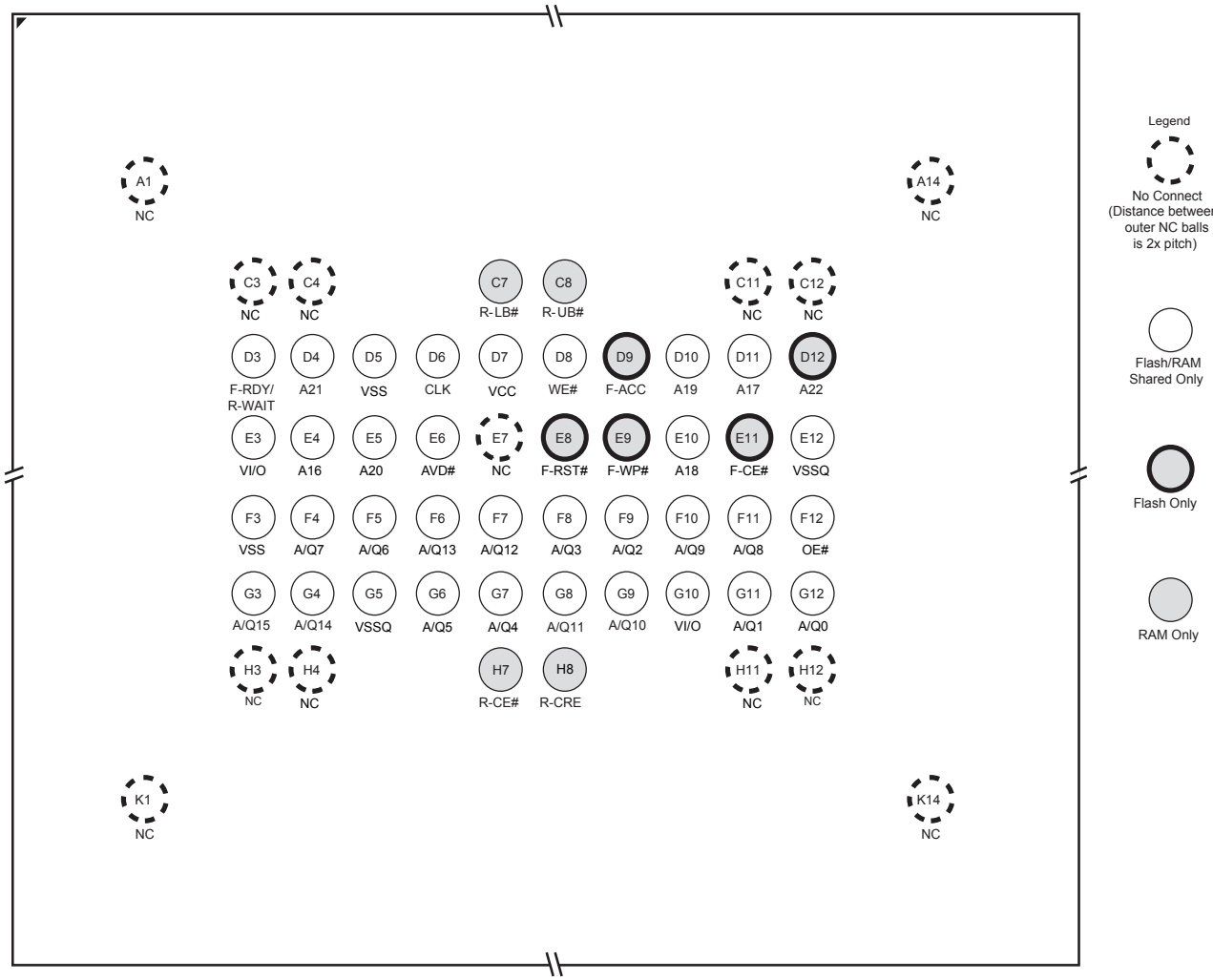
Device	Flash Density	Flash Speed	pSRAM	Package Type	Boot Sector Type
MX69V28F64BBXJW	128Mb	108MHz	108MHz	7.7x6.2x1.2 56-TFBGA	Bottom
MX69V28F64BBXLW	128Mb	108MHz	108MHz	7.7x6.2x1.05 56-TFBGA	Bottom
MX69V28F64MBXLW	128Mb	108MHz	108MHz	7.7x6.2x1.05 56-TFBGA	Bottom

3. BLOCK DIAGRAM



4. PIN CONFIGURATIONS

56-Ball, VFBGA with pSRAM



Notes:

1. Flash & pSRAM shared the address pins, which varies by density of pSRAM.

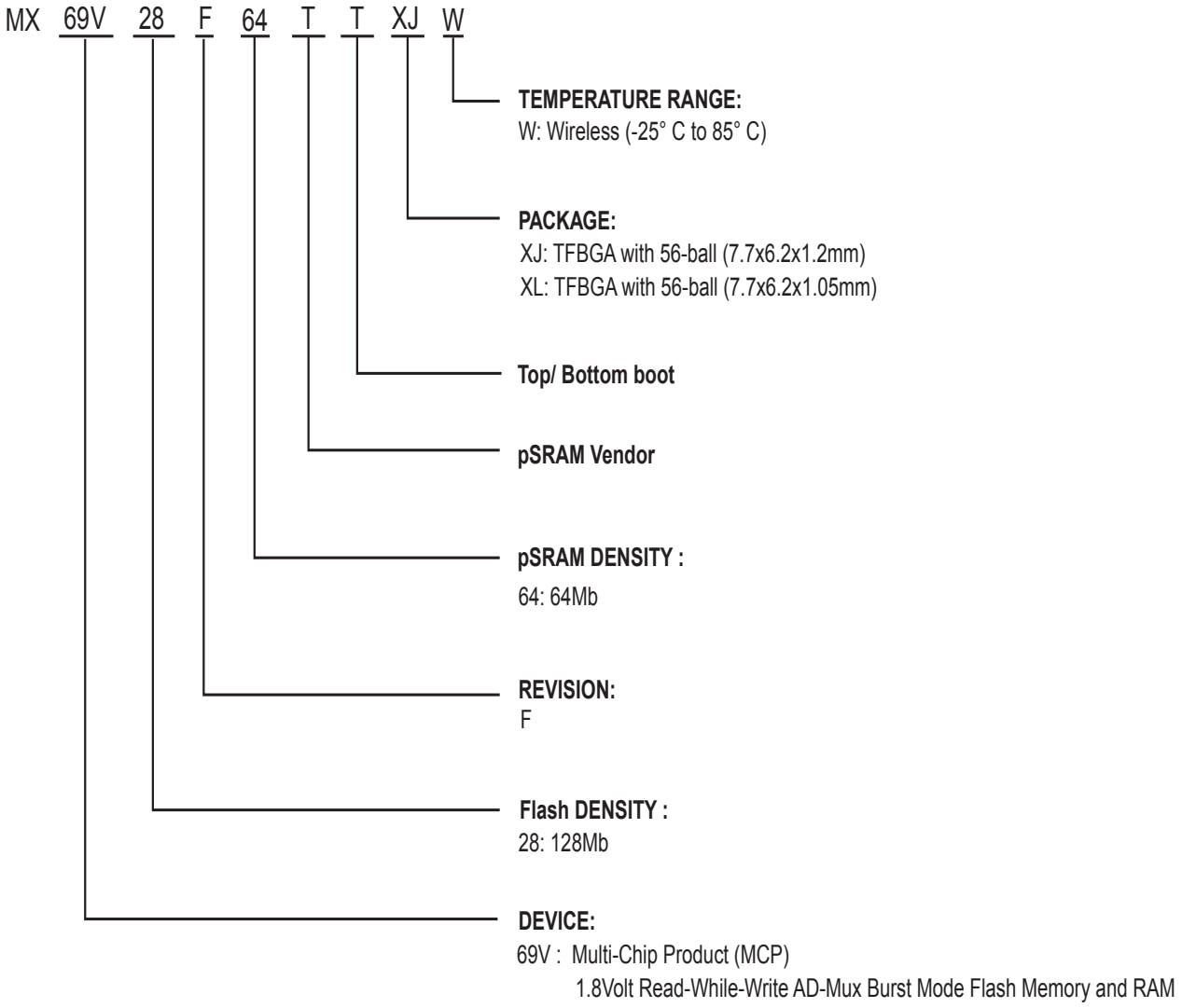
MCP	Shared AQ Pins	Flash-only Addresses	Shared Addresses
MX69V28F64	AQ15-AQ0	A22	A21~A16

5. PIN DESCRIPTION

SYMBOL	DESCRIPTION	Flash	RAM
Amax-A16	Address Inputs for 128Mb	V	V
A/Q15~A/Q0	Multiplexed Data Inputs/Outputs	V	V
OE#	Output Enable	V	V
WE#	Write Enable	V	V
VCC	Device Power Supply (1.70V~1.95V)	V	V
VI/O	Input/Output Power Supply (1.70V~1.95V)	V	V
VSS	Device Ground	V	V
VSSQ	Input/Output Ground	V	V
NC	No Connection	V	V
RDY	Ready status of the Burst Mode	V	V
	Refer to configuration register table		
CLK	Clock	V	V
AVD#	Address Valid Data input.	V	V
F-RBST#	Hardware Reset Pin, Active Low	V	
F-WP#	H/W Write Protect	V	
F-ACC	Programming Acceleration Input	V	
R-CE#	Chip-enable		V
F-CE#	Chip-enable	V	
R-CRE	Control Register Enable		V
R-UB#	Upper Byte Latch		V
R-LB#	Lower Byte Latch		V

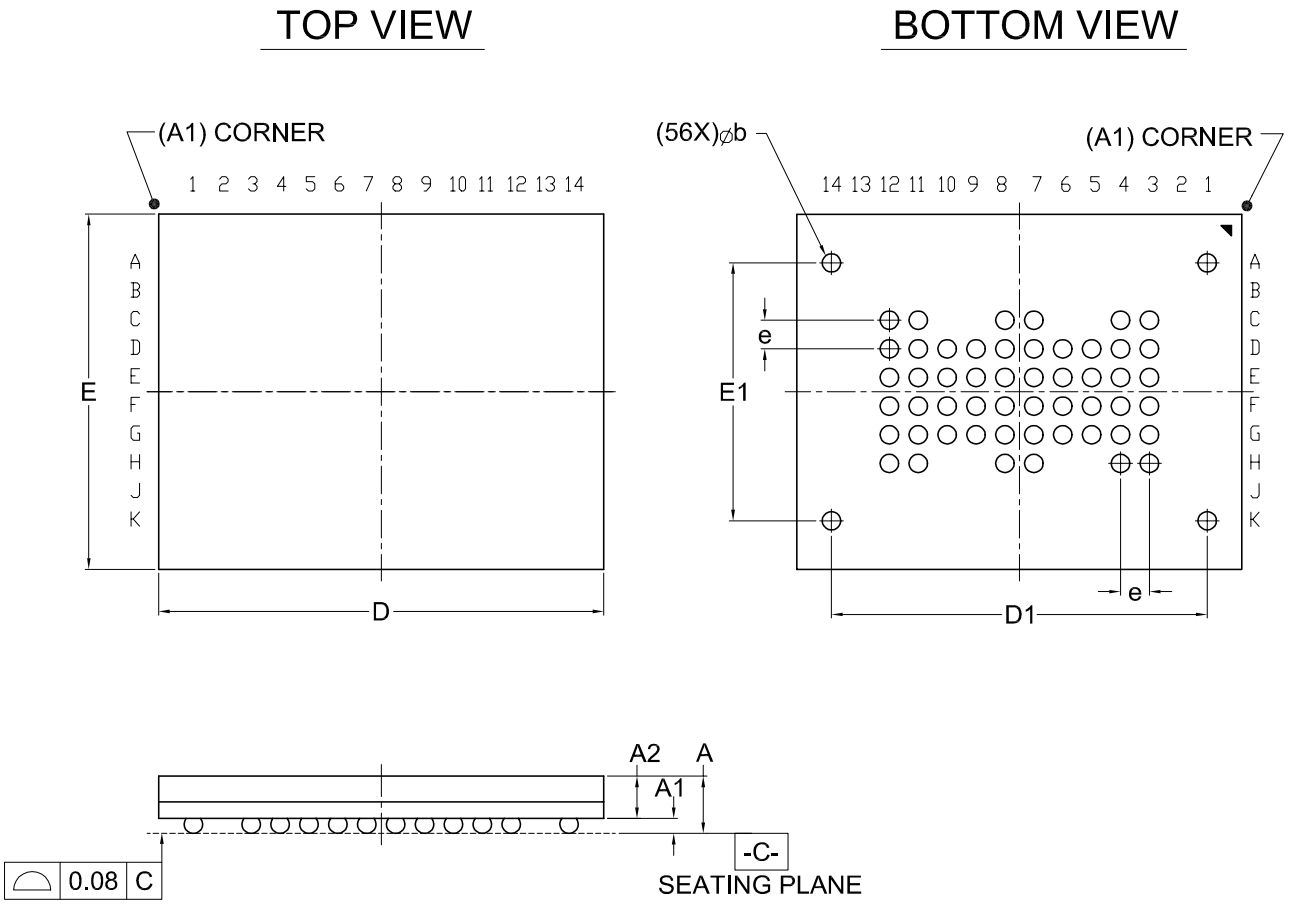
Note: F- : For Flash
R- : For pSRAM

6. PART NAME DESCRIPTION



7. PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 56BALL(7.7X6.2X1.2MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)



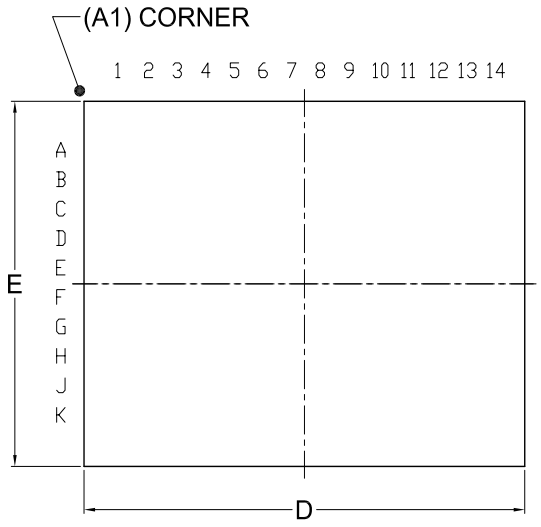
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	---	---
	Nom.	---	0.21	---	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.20	0.26	---	0.35	7.8	---	6.3	---	---
Inch	Min.	---	0.006	0.026	0.010	0.299	---	0.240	---	---
	Nom.	---	0.008	---	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.047	0.010	---	0.014	0.307	---	0.248	---	---

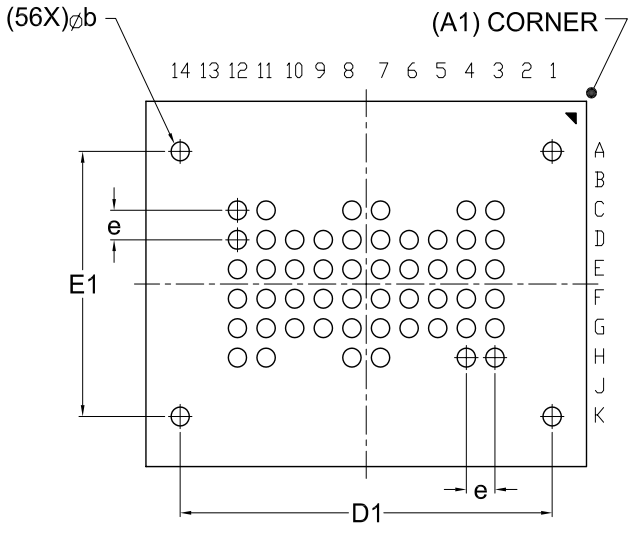
Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4264	1				

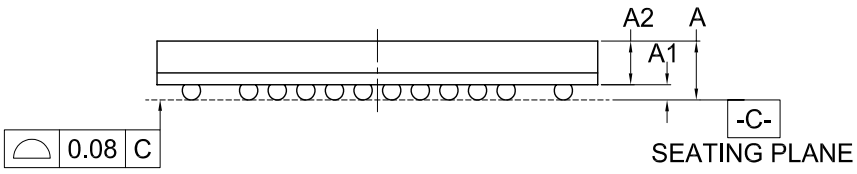
Doc. Title: Package Outline for CSP 56BALL(7.7X6.2X1.05MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)

TOP VIEW



BOTTOM VIEW





Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	---	---
	Nom.	---	0.21	---	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.05	0.26	---	0.35	7.8	---	6.3	---	---
Inch	Min.	---	0.006	0.026	0.010	0.299	---	0.240	---	---
	Nom.	---	0.008	---	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.041	0.010	---	0.014	0.307	---	0.248	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4269	0	MO-225			

8. REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information"	P1,2	JUL/30/2012
	2. Modified word programming time, continuous burst read mode and standby mode	P2	
	3. Added MX69V28F32BBXJW in Product Selection Guide	P3	
1.1	1. Added MX69V28F64BBXLW in Product Selection Guide	P3	NOV/27/2012
	2. Added 56-TFBGA (7.7x6.2x1.05mm) package information	P7,9	
1.2	1. Modified PIN CONFIGURATIONS (from K3 to K1)	P5	APR/25/2013
	2. Added MX69V28F64MBXLW in Product Selection Guide	P3	
1.3	1. Removed MX69V28F32	All	JUL/22/2013

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