# 數位IC設計

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# Syllabus (1/2)

- Time and Place
  - Tuesday:  $9:10 \sim 12:00$

Rm.化工系 華立廳

- Contact Information
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- Office Hour
  - Monday: 8:00~12:00
- Assistants
  - 資訊系10F 數位IC設計實驗室(65A01) 博士生 陳宥融 lt2es.93039@gmail.com

## Syllabus (2/2)

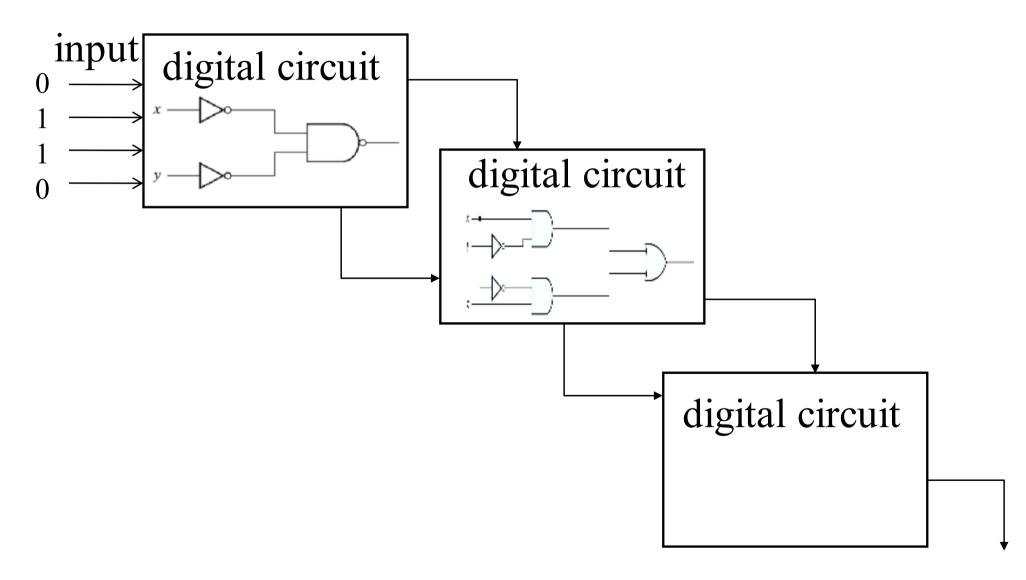
評分方式: 考試(40%~50%)

作業含Demo(60%~50%)

考試為Verilog實作設計,因修課人數較多,考試與 作業皆以pass與fail評分,不會部分給分。 上課1~15週(期末考),3週非同步線上(於第1週看完)。 參考書目:

- 1. 教育部P&L聯盟課程講義-FPGA系統設計實務
- 2. HDL chip design (Douglas J. Smith), Doone Publications
- 3. Principles of digital design (Daniel D. Gajski), Prentice Hall
- 4. Modeling, synthesis, and rapid prototyping with the Verilog HDL (Michael. D. Ciletti), Prentice Hall
- 5. 數位IC設計--Verilog,(陳培殷),滄海書局

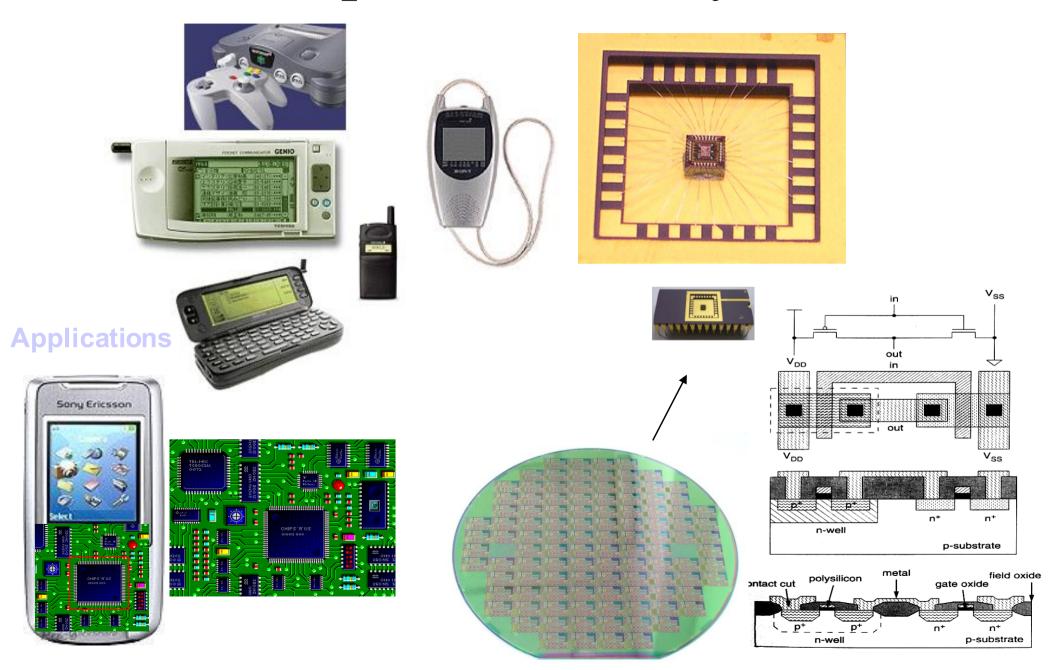
# Digital System



digital circuit === IC (integrated circuit)

semiconductor

# Chip/Circuit Everywhere!



## **Circuits**

- Transistor
- Gate (1 gate ~= 2~14 transistors)

A combination of interacting transistors

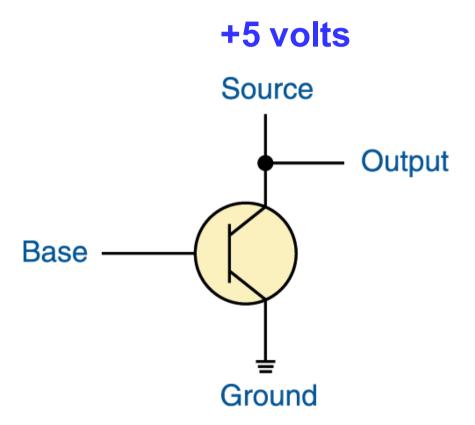
### Circuit

A combination of interacting gates designed to accomplish a specific logical function

- IC (Integrated Circuit)
- System > PCB (printed circuit board)
- SoC (system on a chip) 

  How many gates in a chip?

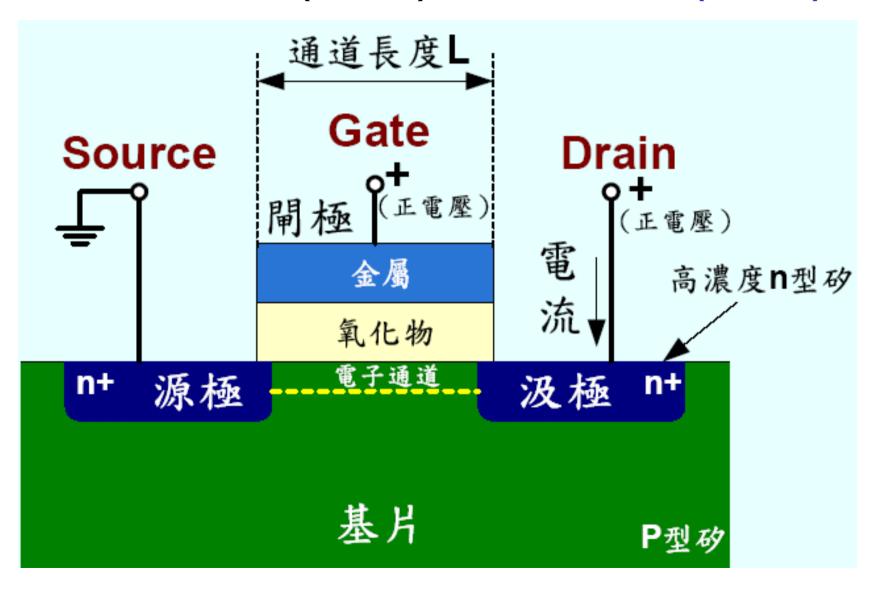
## Transistor(電晶體)



- A transistor has three terminals
  - A source (feed with 5 volts)
  - A base
  - An emitter, typically connected to a ground wire
- If the base signal is high (close to +5 volts), the source signal is grounded and the output signal is low (0). If the base signal is low (close to 0 volts), the source signal stays high and the output signal is high (1)

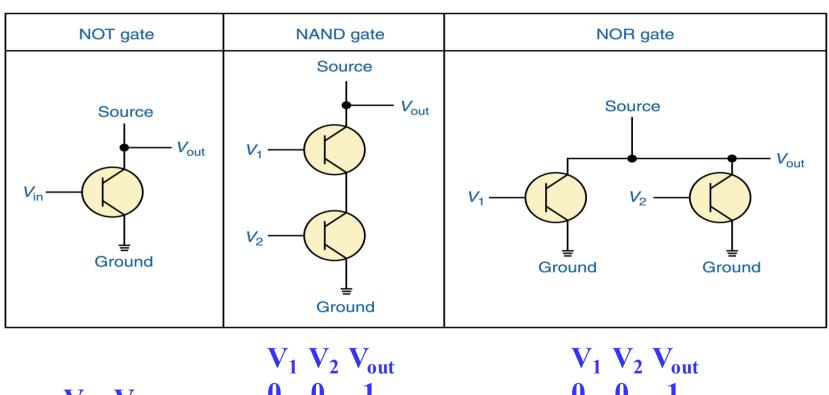
### **N-channel MOS Transistor**

Transistor (電晶體)— Semiconductor(半導體)



## **Constructing Gates (semiconductor)**

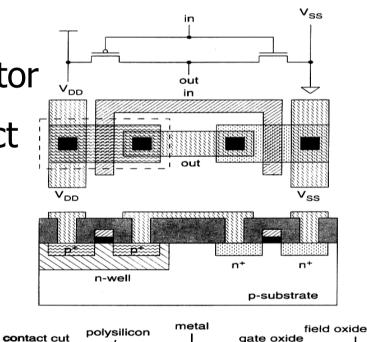
• It turns out that, because the way a transistor works, the easiest gates to create are the NOT, NAND, and NOR gates



# IC Design (with CMOS)

CMOS Inverter in -

One npn transistor and one pnp transistor are used to construct one inverter.



done by chip designer

masking

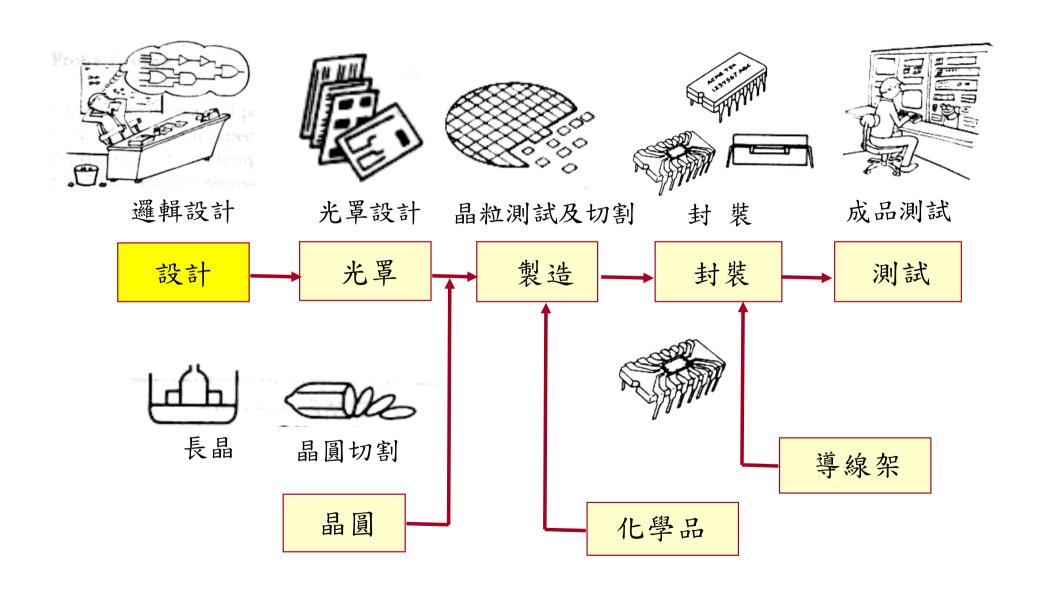
done by TSMC, UMC

Packing, Testing

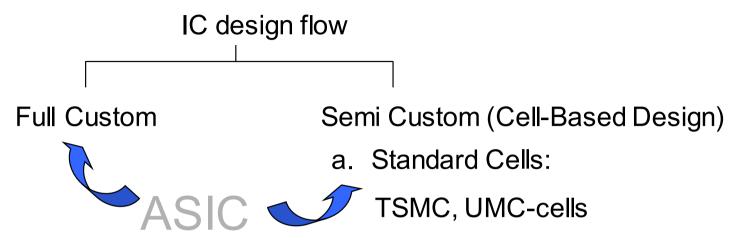
gate oxide

p-substrate

## IC Industry in Taiwan



## IC Design flow



b. FPGA or PLD Programmable logic:

Xilinx, Altera, Actel-cells

### Full (Fully) Custom Design:

- a. For analog circuits and digital circuits requiring custom optimization
- b. Gates, transistors and layout are designed and optimized by the engineer

### Semi Custom Design:

- a. For larger digital circuits
- b. Real gates, transistors and layout are synthesized and optimized by related software tools
- c. Realization with hardware description language (HDL) such as VHDL and Verilog

### **Goal of Course**

- Digital IC Design
- Cell-Based Design
- Verilog
- PC-based simulation

## **Hierarchical Components in PCB**

PCB2

ASIC1 ASIC2 FPGA1

RTL code

SYSTEM

RAM

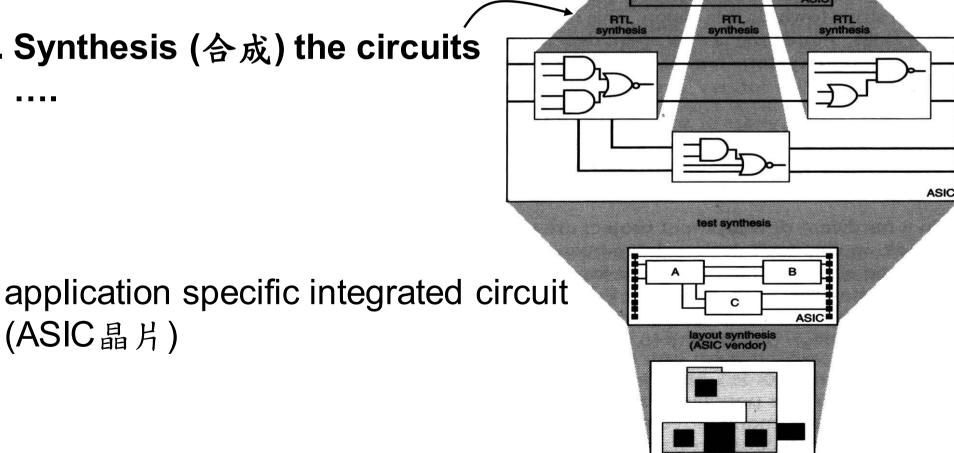
RTL code

PCB1

A RTL code

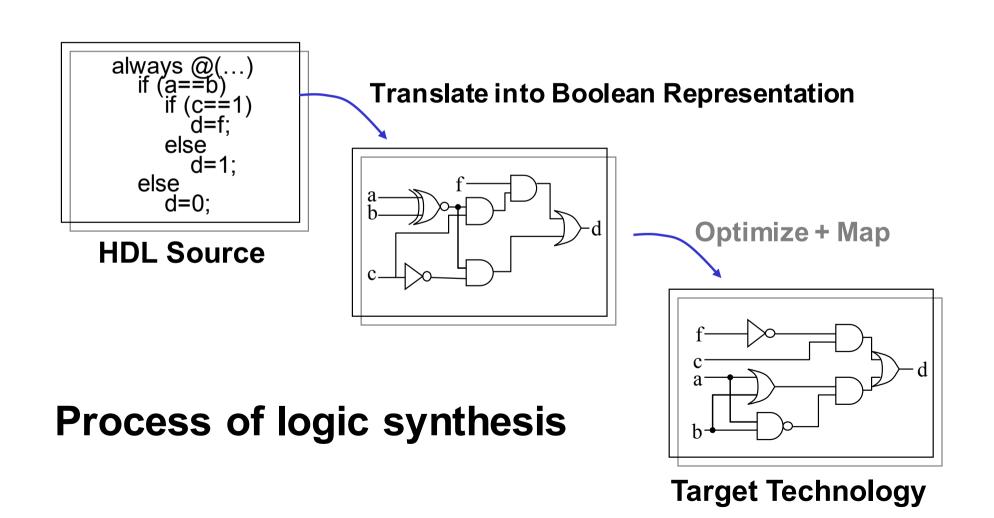
1. Describe the circuits with **Hardware Description Language** (HDL硬體描述語言)

2. Synthesis (合成) the circuits



# **Synthesis**

• Synthesis = Translation + Optimization + Mapping



## 2020 Top 10 Fabless IC Suppliers

https://www.telecomlead.com/wp-content/uploads/2020/08/Top-10-IC-design-companies-2020.png

Table: 2Q20 Revenue Ranking of Top 10 IC Design Companies (Unit: Million USD)

	Rank	Company	2Q20 Revenue	2Q19 Revenue	YoY Change
	1	Broadcom	3,976(E)	4,265	-6.8%
	2	Qualcomm	3,807	3,567	6.7%
	3	Nvidia	3,461	2,352	47.1%
聯發科★	4	MediaTek	2,259	1,977	14.2%
	5	AMD	1,932	1,531	26,2%
	6	Xilinx	727	850	-14.5%
<b>A</b>	7	Marvell	716	659	8.7%
聯詠 📩	8	Novatek	622	527	18.1%
瑞昱 🕇	9	Realtek	579	488	18.8%
	10	Dialog	302	336	-10.1%

#### Notes:

- This table shows only the top 10 IC design companies with publicly disclosed earnings
- NVIDIA's revenue excludes its OEM/IP businesses
- Qualcomm's revenue includes its QCT business only and not QTL; Broadcom's revenue includes its semiconductor business only
- 2Q20 USD/TWD = 1:29.93; 2Q19 USD/TWD = 1:31.14
- Dialog's 2Q19 revenue does not include the \$300 million payment it received from Apple Source: TrendForce, Aug. 2020

## 2020台灣IC設計公司營收

排名	公司	千元	一十十一位	11	矽創	13,804,562
1	聯發科	322,145,988	三千兩百億	12	敦泰	13,800,348
2	聯詠	79,955,521		13	創意	13,569,441
3	瑞昱	77,759,469			<i>&gt;-</i> <b>4.3</b>	, ,
	群聯 [*]	48,496,522		14	天鈺	10,884,838
	擎亞[*]	26,889,818		4 =	ı	0.1.10.01
4	奇景光電	26,214,000		15	原相	8,148,017
	新唐[*]	20,668,056		16	致新	7,407,799
5	- **/   - **	15,507,030		17	祥碩	6,987,470
6	譜瑞	15,278,350		18	威盛	6,502,741
7	品豪	15,268,091				
8	義隆	15,099,690		19	神盾	6,224,427
9	瑞鼎	14,425,152		20	盛群	5,614,539
				21	智原	5,498,295
10	矽力	13,936,157		22	凌陽	6,439,865
-	<i>,</i>	- ) )		23	茂達	5,389,874

## **Outline**

- Chapter 1: Introduction
- Chapter 2: Semi Custom Design Flow
- Chapter 3: RTL Coding-Part I
- Chapter 4: RTL Coding-Part II
- Chapter 5: Digital System Design
- Chapter 6: Control Unit
- Chapter 7: Datapath
- Chapter 8: Case Study
- Chapter 9: System on a Chip
- Chapter 10: Low-Power Design