

Implement a Load-Store Unit (LSU) to manage memory-mapped in Table 1.

32 bit ADDR

32 bit Data

	Boundary address	Mapping	
	0x7820 -- 0xFFFF	(Reserved)	
1 res	0x7810 -- 0x781F	Buttons 16res) input - bank K	
1 res	0x7800 -- 0x780F	Switches (required) 16res	
	0x7040 -- 0x70FF	4thanh (Reserved)	
30 → 33	1 res	0x7030 -- 0x703F LCD Control Registers	
20 → 23	2 res	0x7020 -- 0x7027 7024 4thanh Seven-segment LEDs	output - bank (peripheral)
24 → 27	1 res	0x7010 -- 0x701F 4thanh Green LEDs (required)	
10 → 13	1 res	0x7000 -- 0x700F 4thanh Red LEDs (required)	
00 → 03	1 res	0x4000 -- 0x6FFF (Reserved) (2 ; 3)	
	0x2000 -- 0x3FFF	Data Memory (8KiB using SDRAM) (required) D mem - Bank	
	0x0000 -- 0x1FFF	Instruction Memory (8KiB) (required) (output peripheral mem)	

Table 1: LSU memory mapping

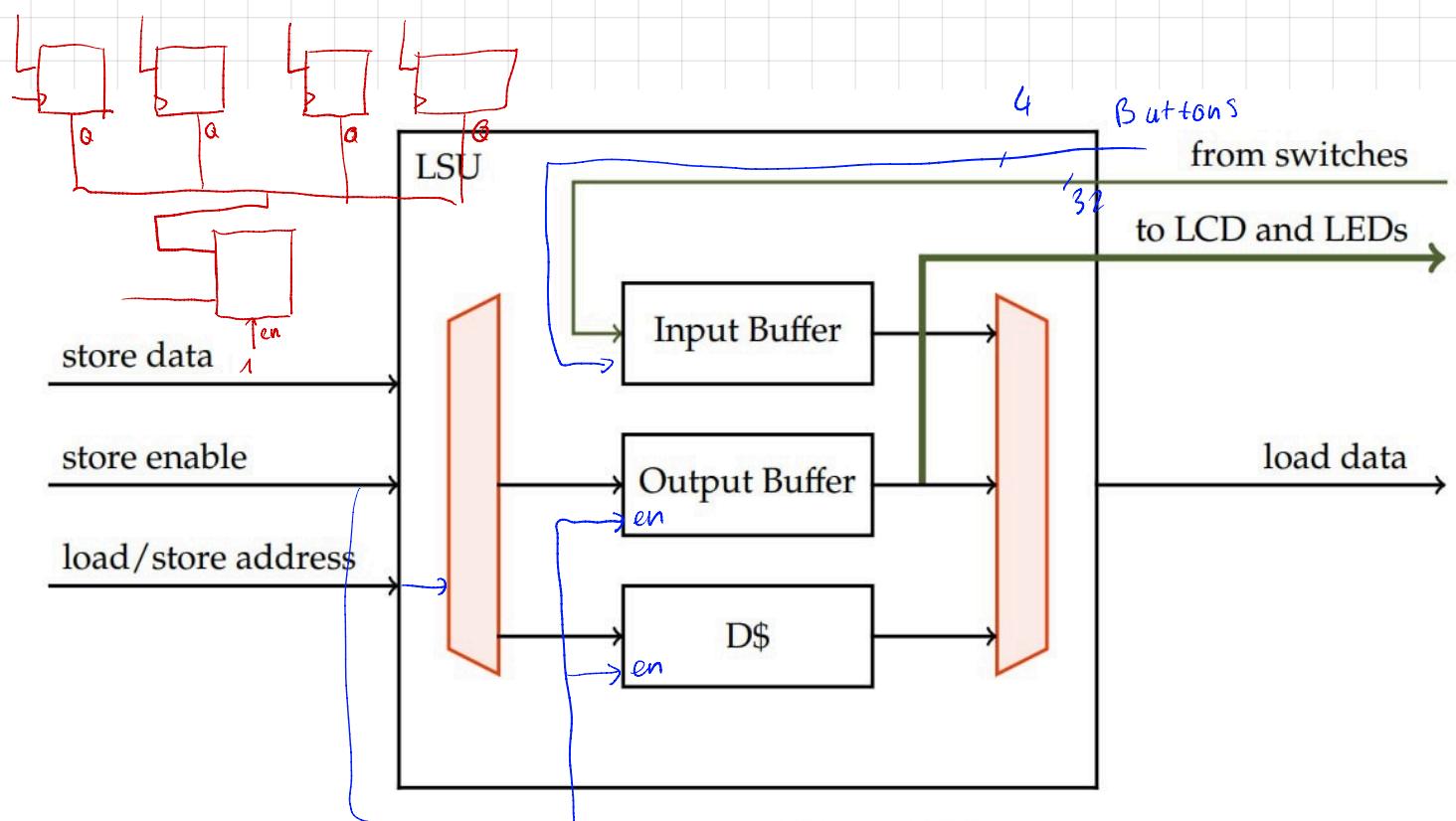
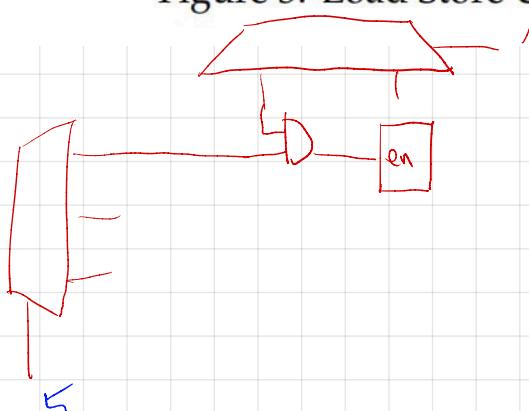


Figure 3: Load Store Unit



Bank K

input	(78) - FF	0111 1000	\rightarrow	X111	
output	(70)	0111 0000	0111	0000	
sram	(20-3F)	0010 0011 0000 1111	001X	XXXX	[15; 8]

input output sram

Bank K_Sel

X111 1XXX
0111 0000
001X XXXX

0	0	0
1	0	0
0	1	0
0	0	1

vẽ bảng ra tính



15 14 13 12
0 1 X 1
0 1 1 1
0 0 0 0

addr [15:8]

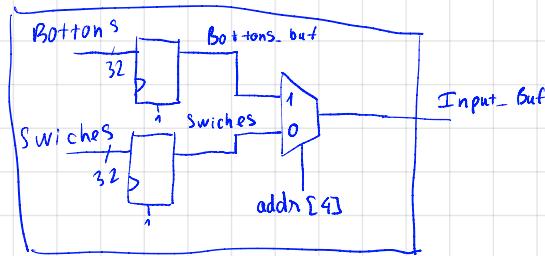
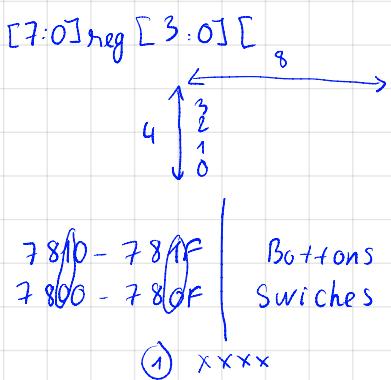
$$\text{output_buf_en} = \overline{15} \cdot (14, 13, 12), \overline{(11+10+9+8)}, i_lsu_wren$$

$$\text{sdram_en} = \overline{15} \cdot \overline{14} \cdot 13 \cdot i_lsu_wren$$

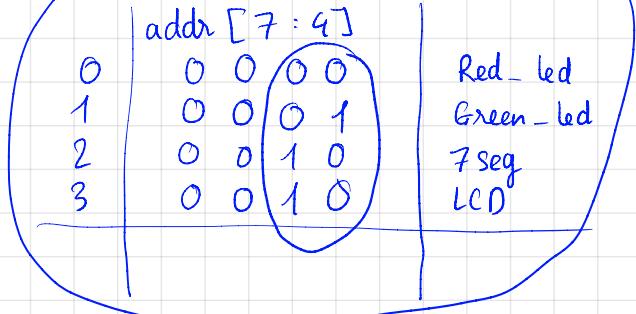
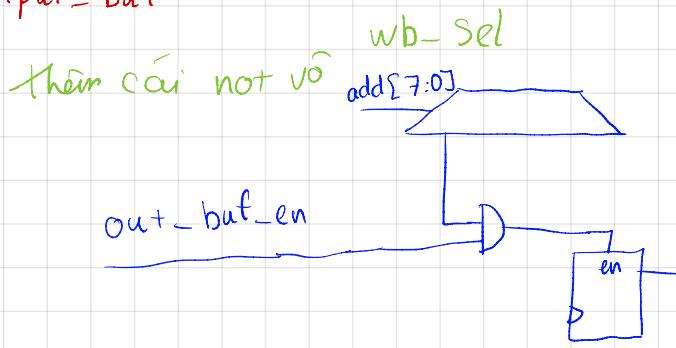
output sd
0 1
1 0
1 0

Decoder_buf

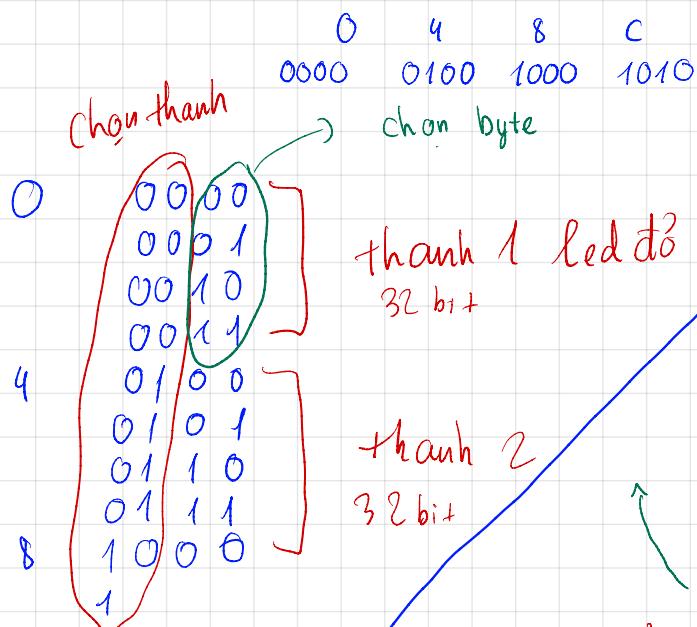
Input_buf



Output_buf

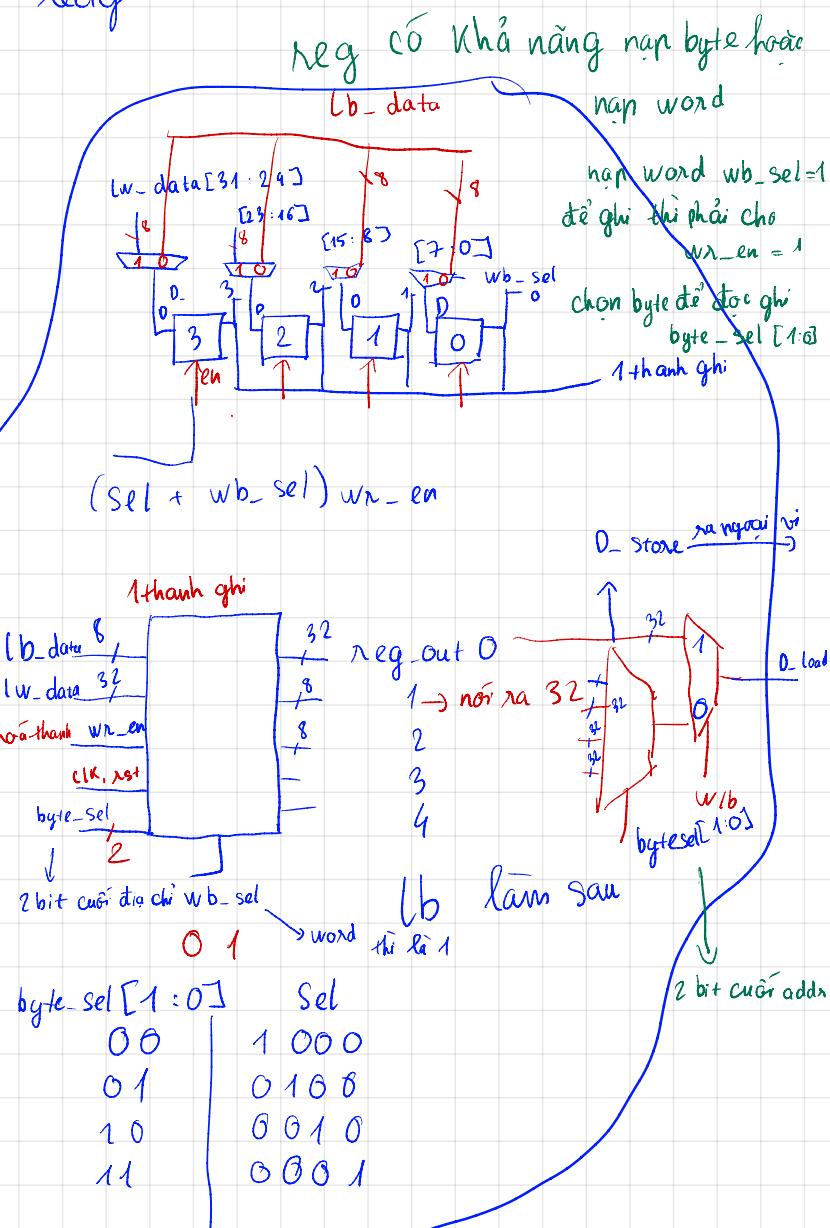


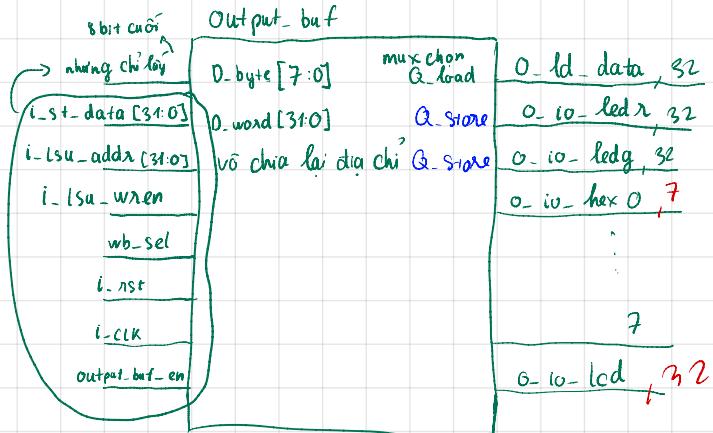
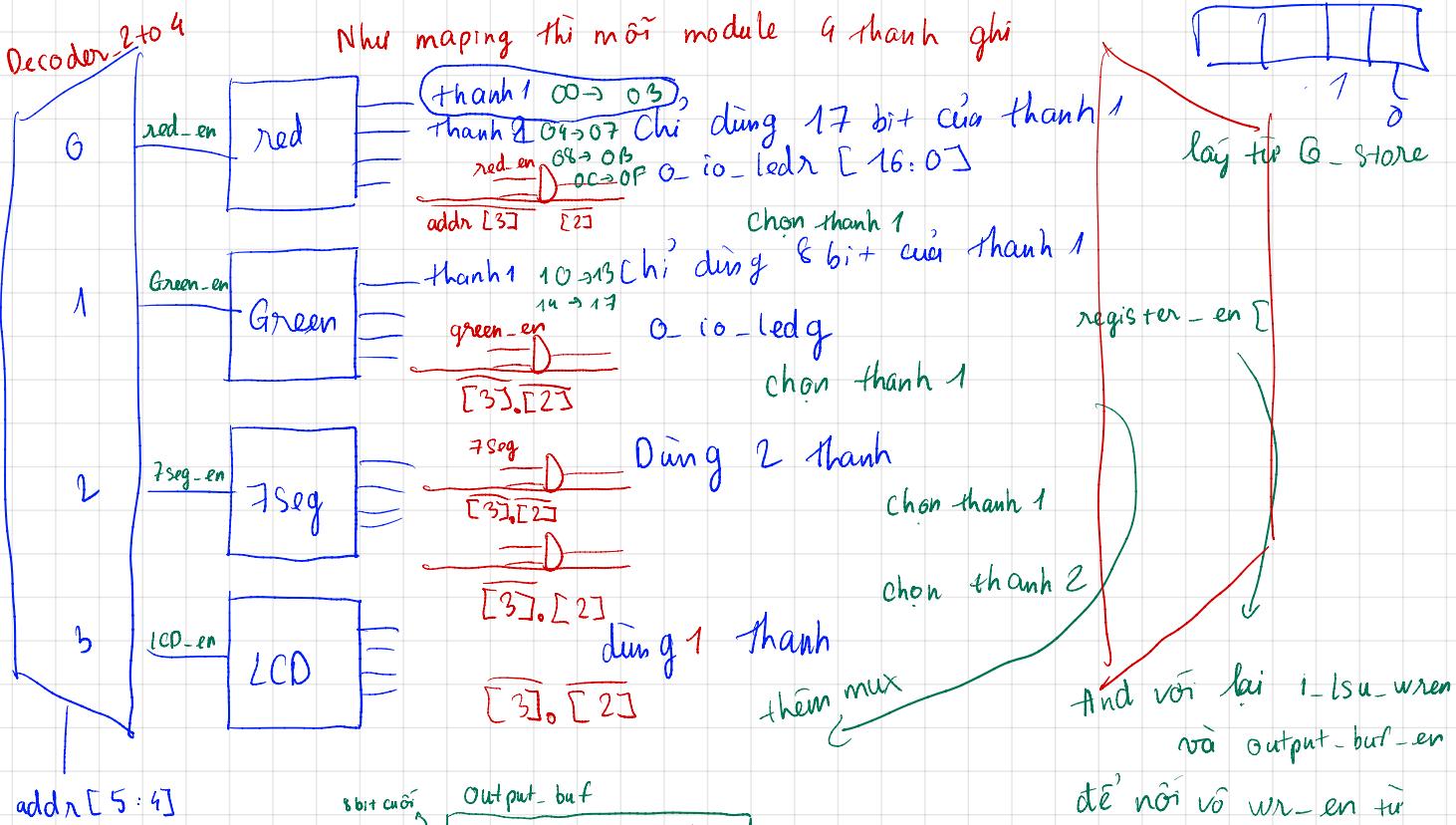
$0x7000 \rightarrow 0x200F$



Với reg này load thi
đọc đc dc đúng giá trị
hiệu tại luôn

Nhưng store phải
đợi CLK tiếp theo byte_sel [1:0]





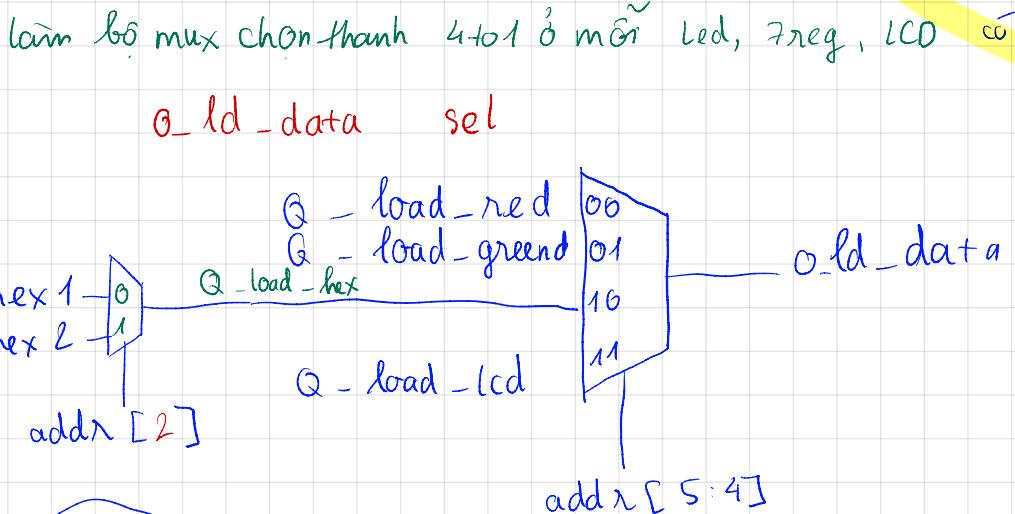
Chú ý Array

[6:0] 0-io-hex [7:0]

mỗi con led

8 con led

có 7 bit dù 7bit



4F 100 1111

6C 110 1100

ở ngõ ra sau khi làm xong sdram thi mới dùng mux

0x7000 : 8 con led đầu cuối

7001 : 8 con led đầu thứ 2

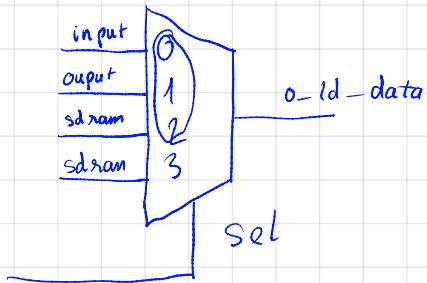
7810 - 781F Buttons → lw 0x7810 → 32 bit

7800 - 780F Switches → lw 0x7800 → 32 SW

(1) xxxx

hex 0 = 0x7020	hex 4 = 0x7024
hex 1 = 0x7021	hex 5 = 25
hex 2 = 7022	hex 6 = 26
hex 3 = 7023	hex 7 = 27

Out - mux



Bank

input	(78) FF	0111 1000	$\rightarrow X111$	
output	(70)	0111 0000	0111 0000	
sram	(20-3F)	0010 0000 0011 1111	001X XXXX	[15; 8]

Bank-Sel	input	output	sram	sel
6 3	0 0	0		
X111 1XXX	1 0	0		0
0111 0000	0 1	0		1
001X XXXX	0 0	1		2

$$ip_en = [6] \oplus [3]$$

$$op_en = [6] \oplus \overline{[3]}$$

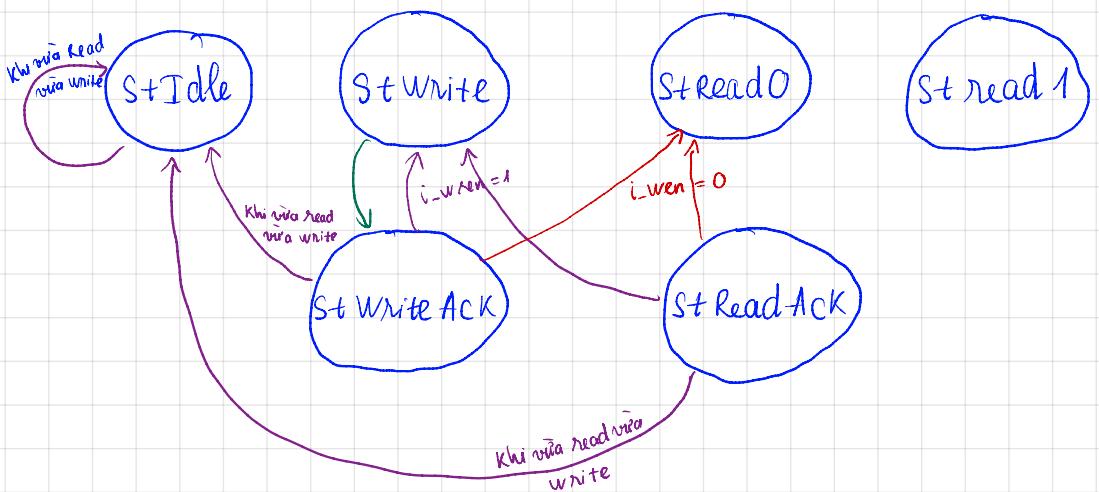
$$sram_en = [6] \oplus [5]$$

sram	ip op	00	01	11	10
0					
1					

ip	op	sram	sel [1:0]
0	0	1	10
0	1	0	01
1	0	0	00

$$sel[0] = \overline{ip} \wedge \overline{op} \wedge sram$$

$$sel[1] = \overline{ip} \wedge op \wedge \overline{sram}$$



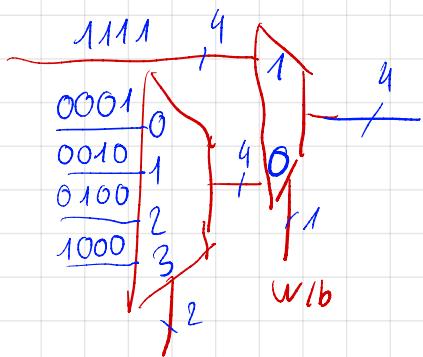
Ghi và đọc đều đọc 2 byte thay vì 1 byte
mỗi and với 18'h 3FFE trước rồi Khi qua state
ACK thì mới tiếp tục đọc ghi với 16 bit cao

d là tiếp theo q là hiện tại

SRAM-DQ thô nối để K0 ảnh hưởng đến data trong sram

$$wb_sel = 1 \rightarrow i_B\ MASK = 1111$$

○ → .



byte_sel [1:0]

byte_sel [1:0]	i_B Mask
00	0001
01	0010
10	0100
11	1000

$$\text{byte_sel} = \text{addr}[1:0]$$

