DESIGN AMBA WITH AHB - APB SPECIFICATION

**COMMUNICATION WITH UART**

Report No.01

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July 8th, 2024

# Brief introduction

1. ***Reason for selecting topic:***

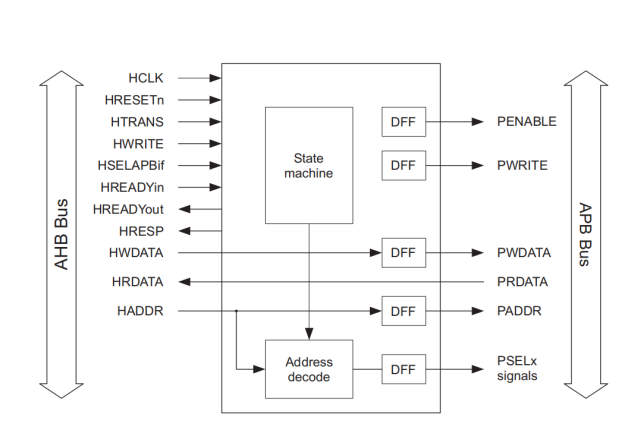
* As I have do experiences and worked with **UART** (Universal Asynchronous Receiver/Transmitter) communication protocol before, Most of Peripheral application protocol nowadays are based on this method. Advantage can be considered with this is the connection’s requirement is only 2 wire for Receiver/Transmitter purpose, which lead the system not too complicated; Moreover, this protocols also support various of speed that commonly nowadays. (4800, 9600, 19.2K, 57.6K, and 115.2K). Moreover, there is an optional parity bit can be used to detect single bit errors which can be used with the design of AMBA AHB – APB specification.
* **Some specific example of UART communication**: RS-232 interfaces, external modules like: GPS, Sensor, RF, Communications Modules,..etc..
* AlthoughUART is still a widely used serial data protocol, there are others protocol such as SPI, I2C, USB, and Ethernet have been used in recent years. However, this protocol seem to be still familiar to most of us and suitable for currently experiment in this Capstone Project 2.

1. ***Development Path***

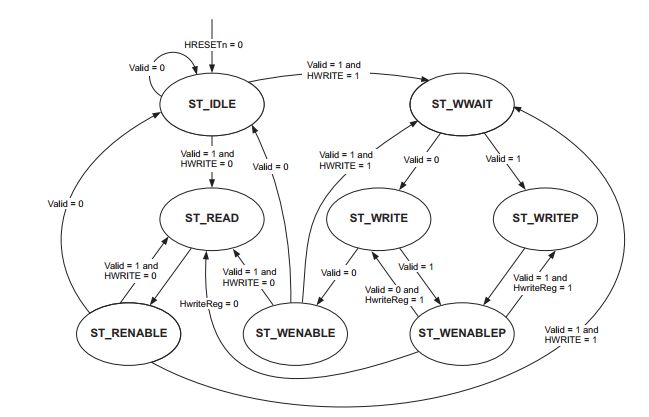
* In the future, if I success with this path, I will continue with its applied, where I will combine this AMBA specification with RISC-V CPU to a fully structure of Computer Architecture to be my final Graduation Project.

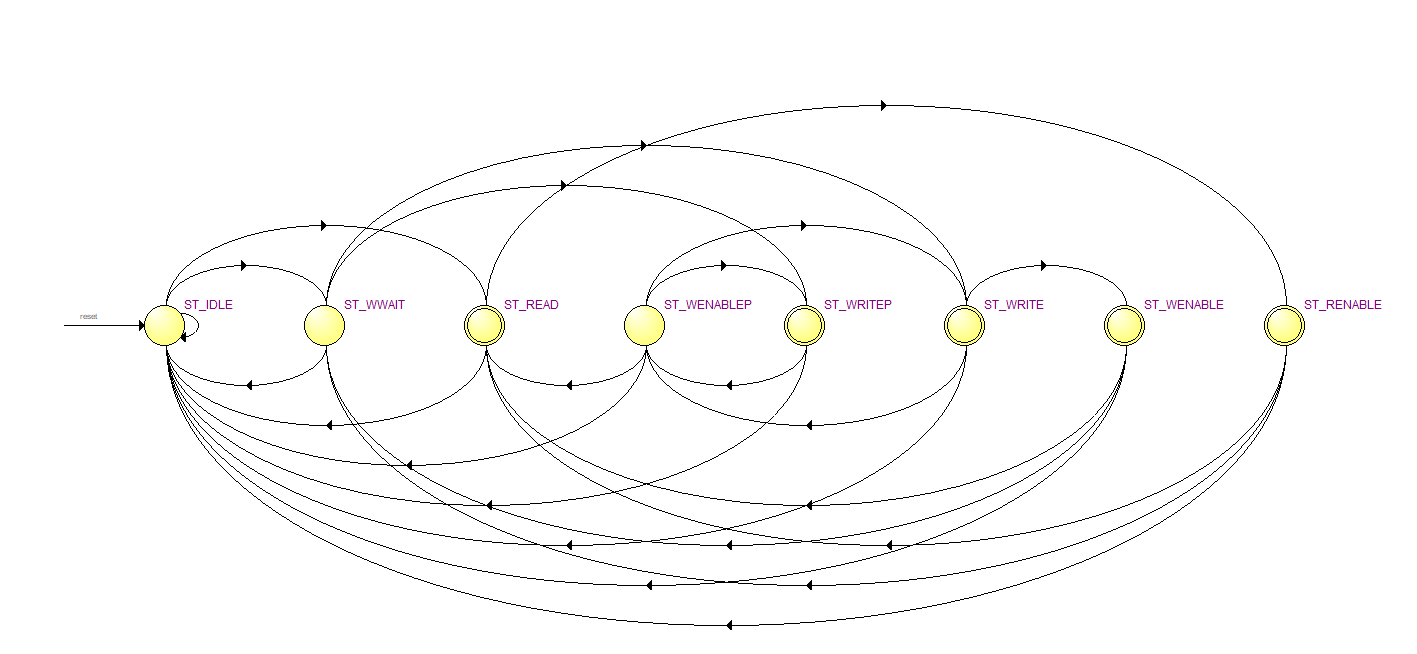
# Problems I anticipated

## Problem 1: *Design an AHB to APB Bridge architecture based on* <https://bvmengineering.ac.in/NAAC/Criteria1/1.3/1.3.4/16EL032.pdf>

<https://developer.arm.com/documentation/ddi0170/a/I967114>

*AHB to APB Bridge block diagram (AHB slave)*

Firstly, I choose to work with **FSM** of **AHB slave,** because to me, this is an easy way for knowing briefly about its operation.

*State machine for AHB to APB interface*

Based on the FSM given, I can generally construct the the flow of data inside AHB slave. Then I come with trouble where the HwriteReg, Valid as you can see in the given state machine’s design is a signal come outside. (I think must be related to HWRITE, HADDR (not present in this graph), also HWDATA).

**Solution**

Fisrtly, About **HwriteReg** first, I have not read found documents relate to this problem yet, so I have used my own way by checking data of the upper signal.

If (**HWRITE** (high active for write) && **HADDR** ?= 0 && **HWDATA** ?= 0) and this did solve the currently problem. I don’t make sure it work with the whole system yet but to me this can be considered the problem is solved.

Secondly, come to **Valid**, this is simple because it already explained in the documents in which is used as a signal to indicate whether there is another peripheral write transfer need to be performed in case that maybe the peripheral require some Gain, Offset,..etc.. I thought it easy, until I come to implement this thought:

if ( **HWRITE** && **ACK** ( a signal I created) ) to check whether there is **HWDATA** exist in the next clock.

At the end, I have not finished with this in this week yet, although you told me to arrive at Unversity room if I met any trouble that I can sold, I thought I able to solve this, just need a little more time.

## Problem 2: Finding an suitable example structure of UART communication protocol

## For my project development and application for testing, I have found this UART model when I had no idea how to solve the previous problem (Valid signal).

# Solution

I am continuing with my project with this struct, because not only it can gave me the detail of each block interfacing, but also the application. So I will try to experience more with this until I find a practical, more suitable to your advice in the next week.

# References

1. ***AMBA AHB Protocol Specification*** <https://developer.arm.com/documentation/ihi0033/latest/>
2. ***AHB Example AMBA System Technical Reference Manual*** <https://developer.arm.com/documentation/ddi0170/a/I967114>
3. ***DirectCore Advanced Microcontroller Bus Architecture - Bus Functional Model*** <https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/UserGuides/CoreAMBA_BFM_UG.pdf>
4. ***Effective Design and Implementation of AMBA AHB Bus Protocol using Verilog*** <https://www.researchgate.net/publication/337510558_Effective_Design_and_Implementation_of_AMBA_AHB_Bus_Protocol_using_Verilog>
5. ***AMBA AHB Protocol*** <https://fr.scribd.com/doc/41197279/AMBA-AHB-Protocol-Presentation>
6. ***PrimeCell UART (PL011) Technical Reference Manual*** <https://developer.arm.com/documentation/ddi0183/g>
7. ***Design and FPGA Implementation of UART Using Microprogrammed Controller***

<https://www.researchgate.net/publication/282030059_Design_and_FPGA_Implementation_of_UART_Using_Microprogrammed_Controller>