DESIGN AMBA WITH AHB - APB SPECIFICATION

**COMMUNICATION WITH UART**

Report No.02

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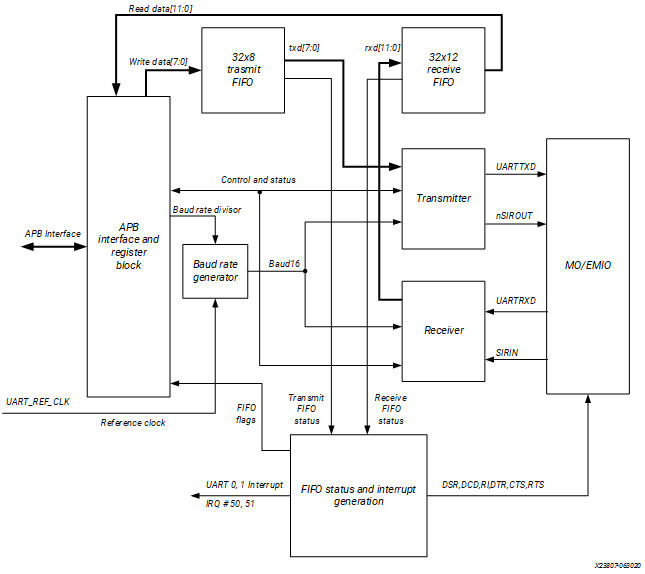
July 17th, 2024

# Problems I anticipated

## Problem 1: structure of UART communication protocol

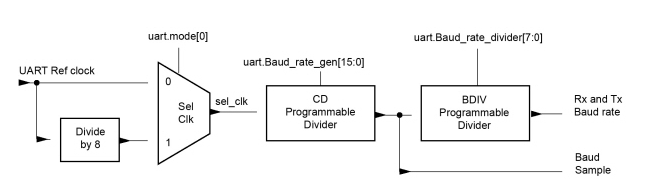
**Figure: APB UART block diagram**

As I have researched during this week, inside APB UART (APB Slave), there are several sub-blocks, took different responsibility such as (based on below figure):



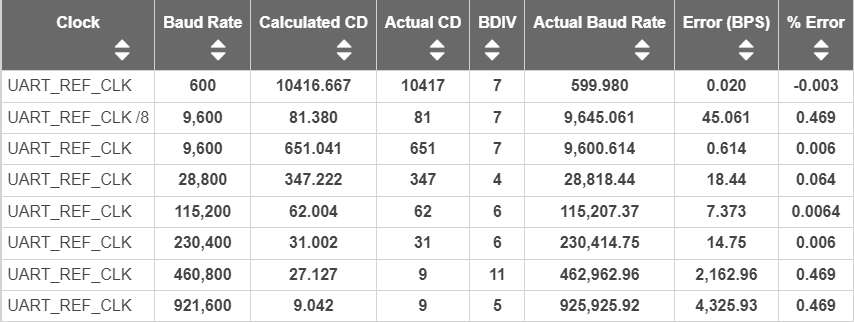
***Figure 1.1: General Block Diagram of APB UART***

* **Baudrate Generator** (theory): furnishes the bit period clock, or baud rate clock, for both the receiver and the transmitter. The baud rate clock is implemented by distributing the base clock UART\_REF\_CLK and a single cycle clock enable to achieve the effect of clocking at the appropriate frequency division.

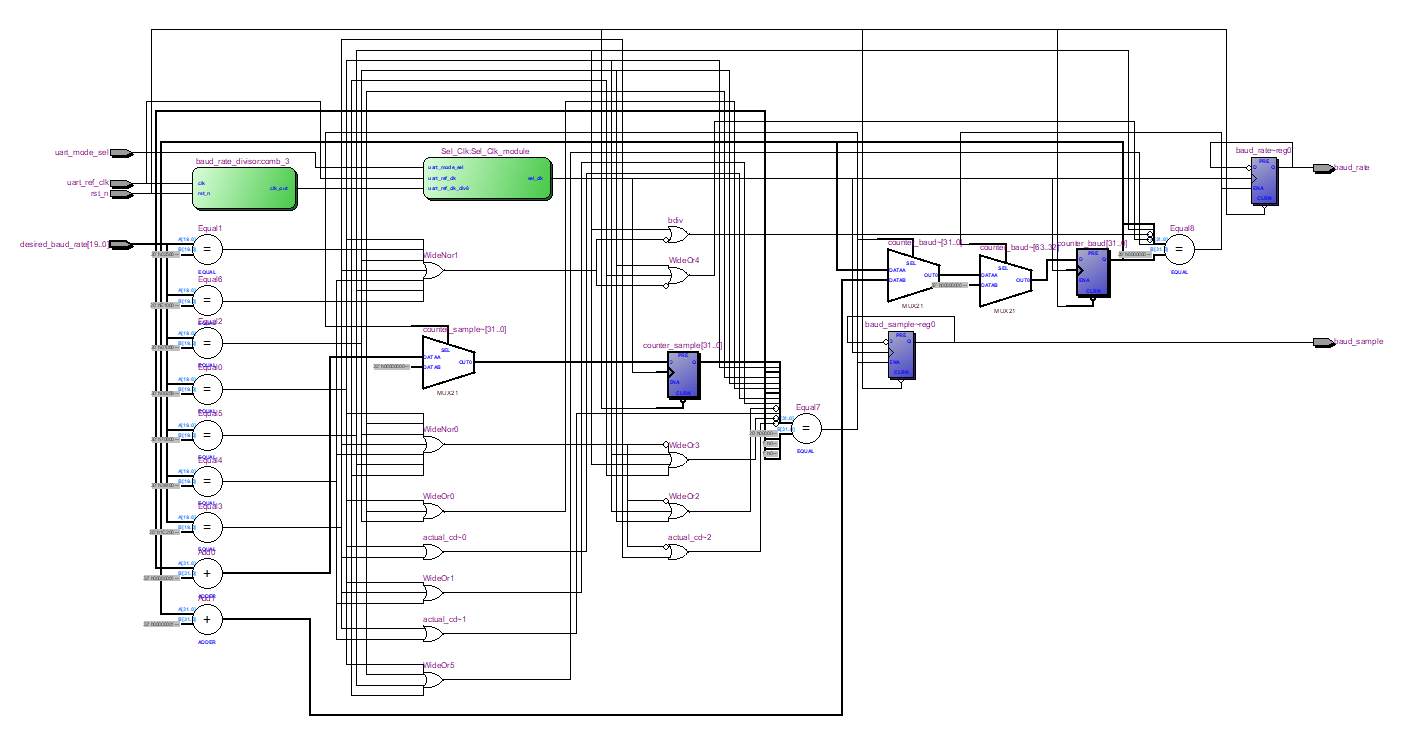
 ***Figure 1.2: Block flow design (compenent inside Baud Rate Generator)***

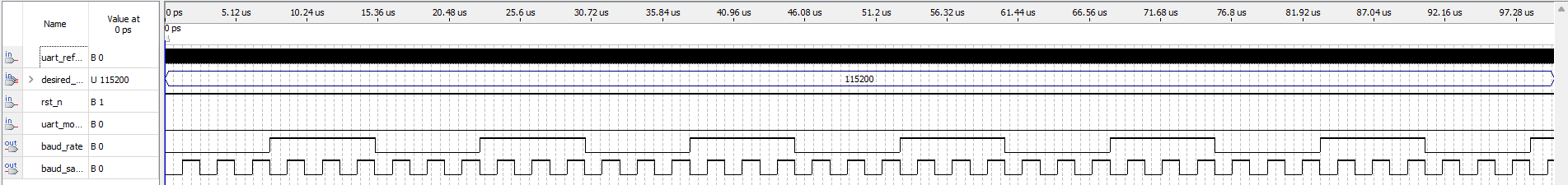
Baud Rate Divisor = UARTx\_REF\_CLK/8= [DIVINT] . [DIVFRAC] (\*\*)

**Note**: This is the value come out from Divide\_8 block due to Figure 1.2

* **Problem arise:** I have not tried to change the CD signal into floating point yet, so there would be error of displaying baud rate exactly value. I already has the way to solve this problem based on the (\*\*) function, in the next few weeks, after I finished with the UART APB block, I’ll comeback and solve this error different problems.

***Table 1.3: UART Parameter Value Examples***

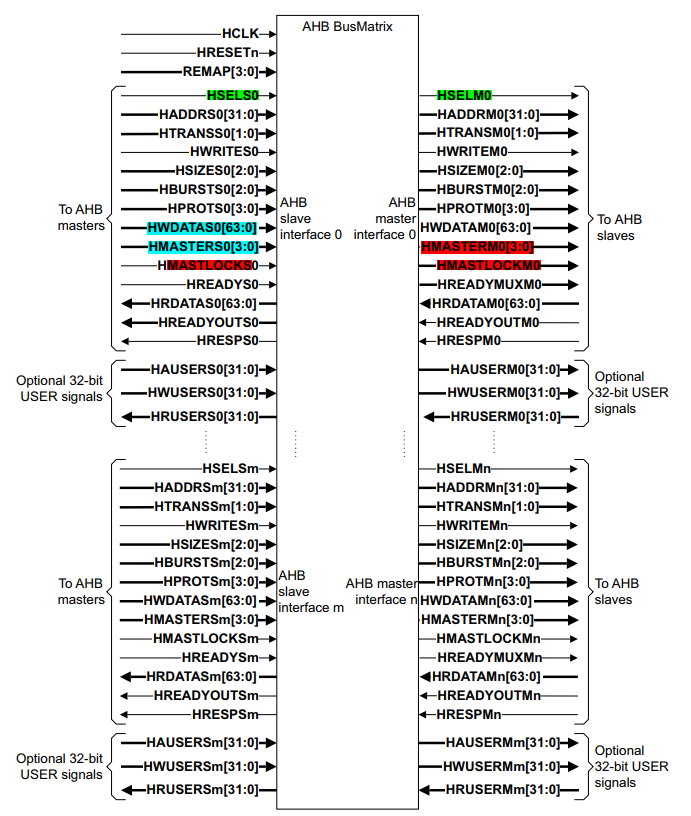
* Come to General Block diagram of BAUD RATE GENERATOR: Here is the block structure that I have based on <https://docs.amd.com/r/en-US/ug1085-zynq-ultrascale-trm/Baud-Rate-Generator>
* ***Figure 1.4: block diagram of UART Baudrate Generator***

And the following ModelSim simulation for making sure that this block run correctly.

***Figure 1.5: Simulation of UART baud rate generator***

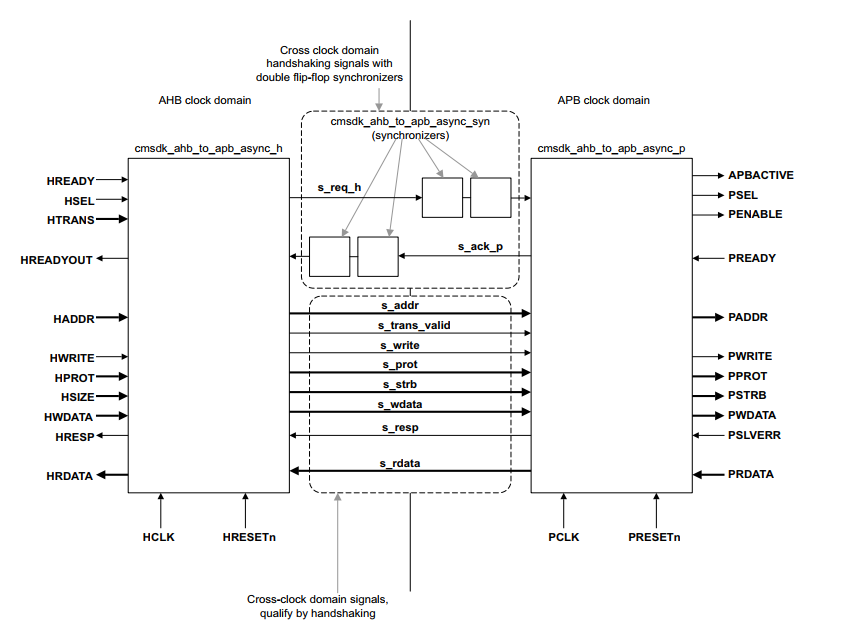
**Where**: In this example, I used UART Baudrate Generator to create an baudrate at 115200 (baud/s), so as result, I insert the value of Baudrate into desire\_baud\_rate (signal) anh this block will do its responsibility. For more details, as I inputted 115200 into desire\_baud\_rate signal, this block generated **CD** (clock divider) and **BDIV** (baudrate divider) so that by dividing the uart\_ref\_clk by 62 time, meaning each 62 clocks counting, the block will inverse the status of previous **clk\_div** value and generate **baud\_sample** and for each 6 times of clk\_div changing state, the baud\_rate output signal will inverse its state. And that is the general operation for this UART Baudrate Generator.

* **Problem that I have solved**: At first, I was misunderstood the functionality of this block so I inserted the value of Frequency instead of generating pulses -> I took too much times for doing with this. However, after doing simulation and look for references, I did figured out and able to solve this.

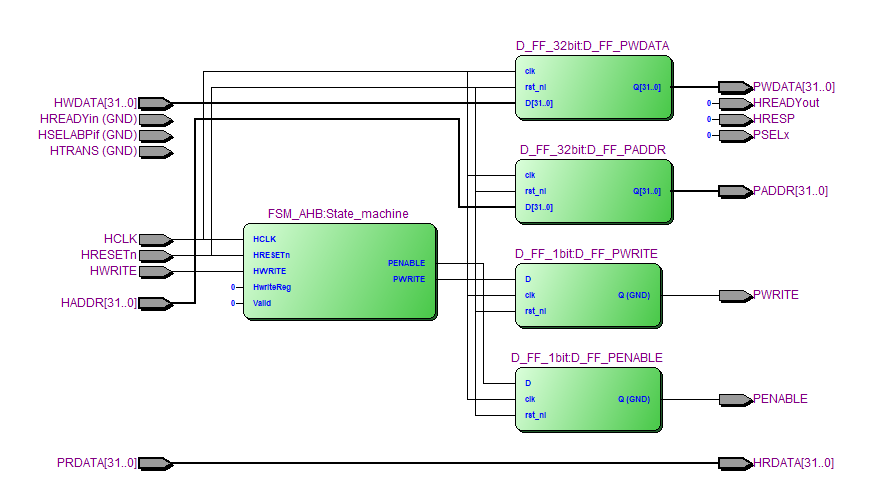
**Problem 2: Construct of communication protocol AHB master – AHB Bus Matrix – APB Bridge (APB Slave) – APB UART**.

***Figure 2.1: Bus matrix module components***

This is the example of general AHB Bus Matrix for communication between Master and Slave that I have found and based on, with this feature, I currently want to use only one Master represent for CPU to control and Slave is APB Bridge.

**Problem: Complete AHB – APB bridge** ****

***Figure 2.2: Block diagram of bridge module***

Based on this design, I was generally finised the structure.

***Figure 2.3: Block diagram of bridge module (via RTL view)***

However, as you can see in the RTL generated via Quartus, the signal is not complete yet because I still have troubled with the **Address decode** block; however, I have found a related example for this, in which I will use **HADDR**, **HRESETn** and addition **REMAP** signal to generate PSELx**.**

# References

1. ***AMBA AHB Protocol Specification*** <https://developer.arm.com/documentation/ihi0033/latest/>
2. ***AHB Example AMBA System Technical Reference Manual*** <https://developer.arm.com/documentation/ddi0170/a/I967114>
3. ***DirectCore Advanced Microcontroller Bus Architecture - Bus Functional Model*** <https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/ProductDocuments/UserGuides/CoreAMBA_BFM_UG.pdf>
4. ***Effective Design and Implementation of AMBA AHB Bus Protocol using Verilog*** <https://www.researchgate.net/publication/337510558_Effective_Design_and_Implementation_of_AMBA_AHB_Bus_Protocol_using_Verilog>
5. ***AMBA AHB Protocol*** <https://fr.scribd.com/doc/41197279/AMBA-AHB-Protocol-Presentation>
6. ***PrimeCell UART (PL011) Technical Reference Manual*** <https://developer.arm.com/documentation/ddi0183/g>
7. ***Design and FPGA Implementation of UART Using Microprogrammed Controller***

<https://www.researchgate.net/publication/282030059_Design_and_FPGA_Implementation_of_UART_Using_Microprogrammed_Controller>