Capstone Project 2

Week 7 (33) – Semester 233

Student: Vo Viet Hung – 2051076

**Implementation of AHB-APB and APB-UART bridges**

# The problem: APB UART

In the past week, I dedicated most of my time to expanding and refining the functions and states of two key blocks in the APB UART system: the TX FSM and RX. This was a crucial step in optimizing and enhancing the overall performance of the system. Furthermore, during testing operation, I still struggle with numerous issues so I have still not finished with the design flow of my project.

*1.1.* ***Summary***

For the TX FSM block, I added new states to improve the data transmission process. These states not only enable more efficient management of routine scenarios but also enhance the handling of exceptional conditions, ensuring that data transmission occurs smoothly and without limitation due to some customize methodologies of sending data (such as 2 stop bits, 5-6-7-8 bits of data instead of steady 8 bits, parity bit check or not,…).

Similarly, the RX block was expanded with new states (IDLE) to improve its flow operating whether to listen for RXen ability to receive and process incoming data. These states play a vital role in synchronizing data and ensuring that all received information is accurately decoded and processed related to input RXD or some specific modules’ operation. Moreover, I introduced functions for error checking and data validation, which help to promptly detect and address any issues arising during data reception, thereby increasing the system's reliability.

These improvements not only optimize the performance of data transmission and reception but also contribute to the stability and reliability of the entire APB UART block in real-world operating conditions. By expanding and fine-tuning the states and functions of the TX FSM and RX blocks, the system has become more robust and better prepared for the next stages of testing and integration.

***1.2. Solution***

The solution that I supposed is come from the document [DDI0183G\_uart](https://developer.arm.com/documentation/ddi0183/latest/programmers-model/register-descriptions/primecell-identification-registers--uartpcellid0-3), in which there is a supposed features for an complete UART operation and by followed that, I have re-customized my APB UART structure for a better flexibility to diversity of communicating configuration. Moreover, after I added these, I have troubled with the signal generated out and I am on the way to solve them.

**2. Planning for next week working**

For the next week, If I am able to complete what I have extended well, I would continue combining the AHB Slave (AHB-APB Bridge) together with APB UART and run whole simulation of it again.

**----------------Thanks for reading my Journal-------------**