Final Project Proposal:

An Exploration of L2 Cache Associativity and L1 Cache Implementations; A Simulator Implementation of a LRU-Based Column Associative Cache

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The objective of this paper is to explore the implementation of L1 and L2 data caching techniques, notably column-associative, and LRU-based column-associative cache implementations in L1 with 2-way and 4-way associative L2 cache implementations. The implementations of these data caching techniques and their miss-hit rates will be compared against direct-mapped L1 caches, with 2-way and 4-way associative L2 cache configurations. The simulated caches will be evaluated across multiple cache sizes (2KB and 4KB for the L1 with a constant 8KB L2 cache) with a constant 64 Byte block size. To simulate the direct-mapped, 2-way associative and 4-way associative caches, DineroIV will be used. The L1 and L2 implementations of a column-associative cache and a LRU-based column-associative cache will be simulated using python, with the cache structures being declared as classes, each containing a cache Data Frame (chosen for their readability during debugging, and back-end implementation in C). To generate data cache address streams, a Pin tool called pinatrace will be used. Pinatrace generates read and write address traces in reference to main memory in a readable format that can be translated into the address stream format utilized by DineroIV. Two separate programs will be instrumented upon using the pin tool, with one program relying heavily on matrix-based operations and another program relying on non-locality focused operations (such as sparse graph traversal).

The experiment will generate the following miss-hit rate results:

Experiment Number	L1 Cache Implementation	L1 Cache Size	L2 Cache Implementation	L2 Cache Size
1	Direct Mapped	2KB	2-Way Associative	8KB
2	Direct Mapped	4KB	2-Way Associative	8KB
3	Direct Mapped	2KB	4-Way Associative	8KB
4	Direct Mapped	4KB	4-Way Associative	8KB
5	Column Associative	2KB	2-Way Associative	8KB
6	Column Associative	4KB	2-Way Associative	8KB
7	Column Associative	2KB	4-Way Associative	8KB
8	Column Associative	4KB	4-Way Associative	8KB
9	LRU-Column Associative	2KB	2-Way Associative	8KB
10	LRU-Column Associative	4KB	2-Way Associative	8KB
11	LRU-Column Associative	2KB	4-Way Associative	8KB
12	LRU-Column Associative	4KB	4-Way Associative	8KB

The associated grades that I would expect to receive upon the completion of this assignment are:

- A = All cache configurations studied as above, two address traces used (plus the address trace given in homework 4).
- A- = All cache configurations studied as above; one address trace used.
- B+ = All cache configurations evaluated, only 1 cache size evaluated for L1, one address trace used.
- B = 4-way associative caches not evaluated, only 1 cache size tested for L1, one address trace used.
- B- = 2-way associative caches not evaluated, 4-way associative caches not evaluated, only 1 cache size tested for L1, one address trace used.

- C+ = Only a comparison between LRU-based column associative, column associative caches and direct mapped caches performed, one address trace used, one cache size per cache used.
- C = Only a comparison between LRU-based column associative and column associative caches performed, one address trace used.