Sequential circuits

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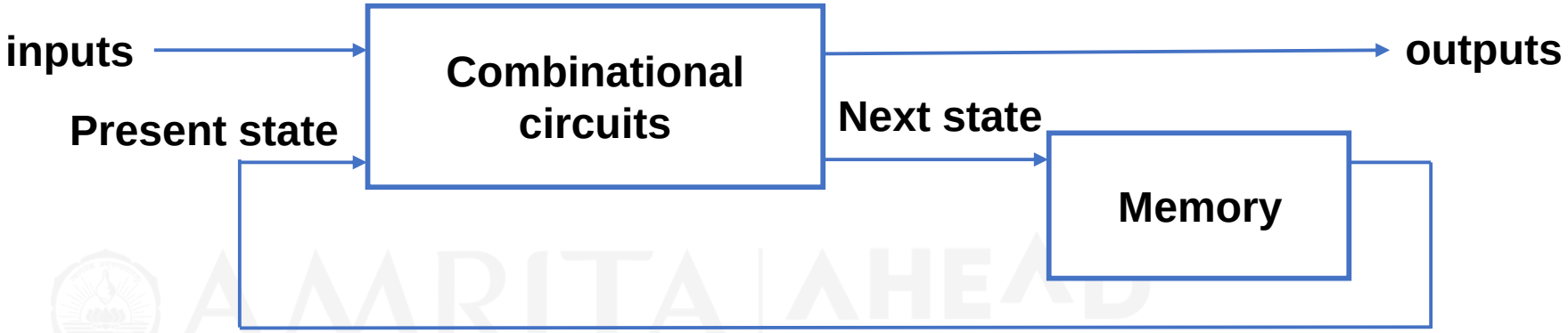
Objective

- Introduction to sequential circuits.

Sequential circuits

- Combinational circuits = no memory (inputs —outputs)
- Sequential circuit output depends not only on the present value of the input but also on previous value of the input signal.
- Sequential circuits = Combinational circuits + memory elements.
- Sequential circuit uses a memory element like flip-flops as feedback circuit to store past values.

Sequential circuits

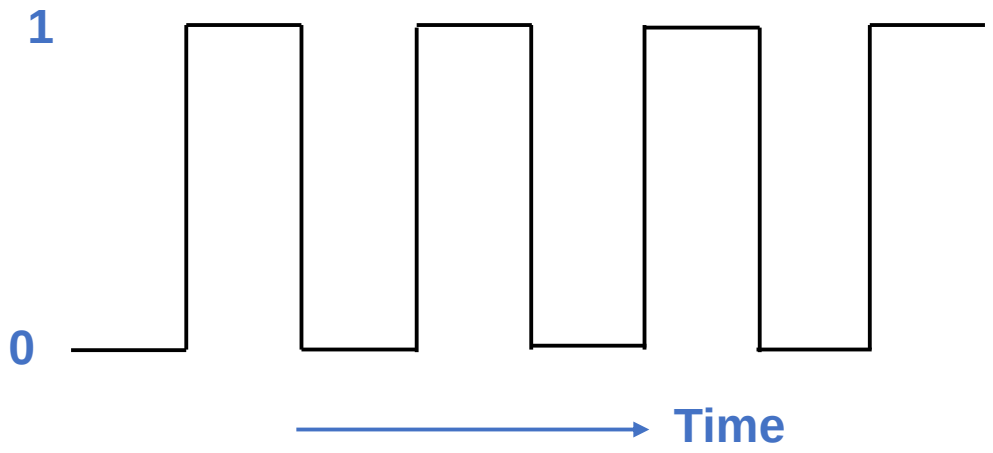


Block diagram of sequential circuit

- Memory : device capable of storing binary information i.e., state.
- (inputs , present state) ⟶ (outputs , next state)

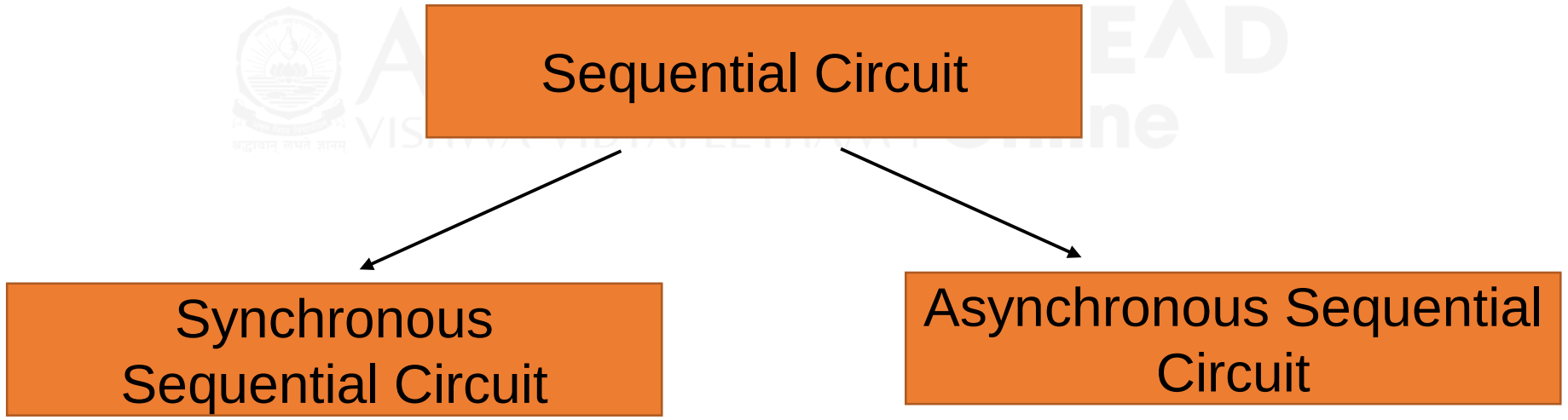
Clock Signal in Sequential circuit

- A clock is a signal which oscillate between logic level 0 and logic level 1 repeatedly.
- Sequential circuit retains its state till the next clock edge occurs



Sequential circuits

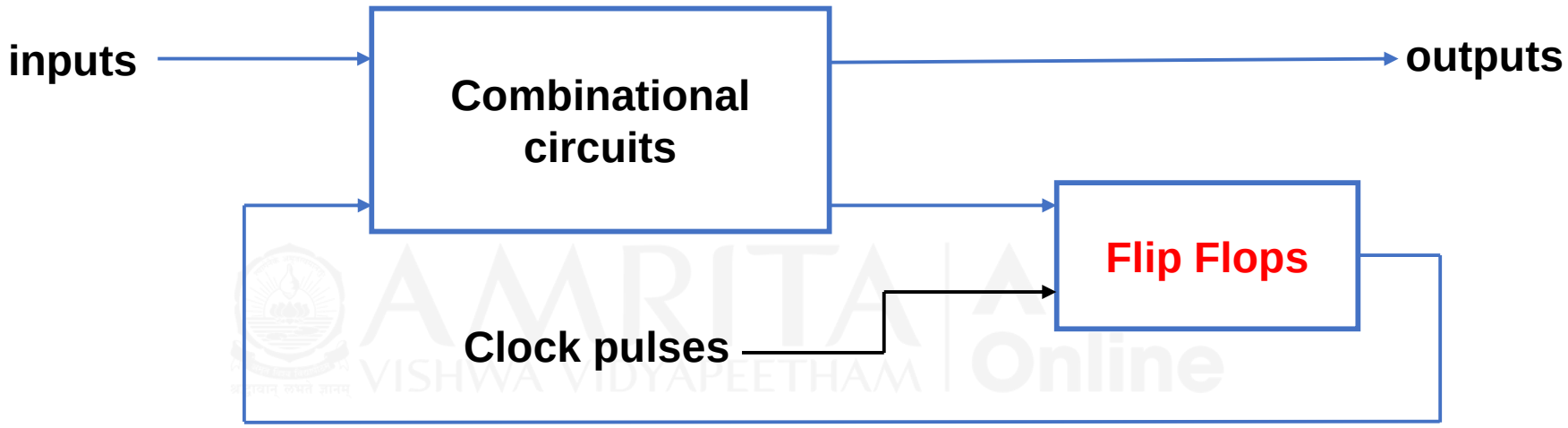
- Two types based on the timings of signal



Synchronous Sequential circuit

- Synchronization is achieved by a timing signal called master-clock generator which generates a periodic clock pulses.
- SS circuits using clock pulses in the input of memory elements are called clocked sequential circuits.
- Clock signal is used to control the exact time at which any output can change its state.
- Memory in clocked sequential circuits are designed using **flip flops.**

Synchronous Sequential circuit

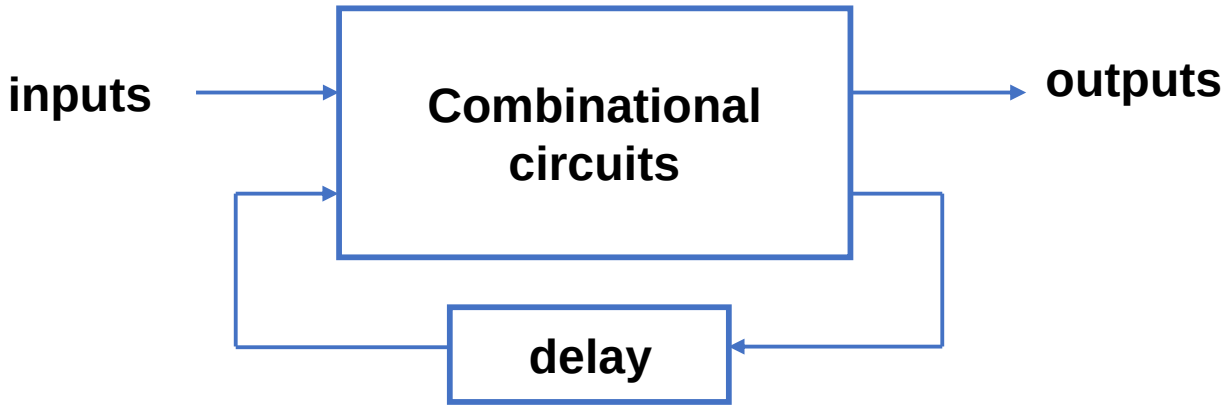


Block diagram of Synchronous sequential circuit

- Flip flops receive inputs from combinational circuits and from clock signal with pulse that occur at fixed interval of time.

Asynchronous Sequential circuits

- System behavior depends on the order in which its input signals change and can occur at any instant of time.
- Do not use clock pulses, so change of state occur at any time.
- Memory elements used are latch or time delay elements.



Summary

- Explained about sequential circuits

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- Gideon Langholz, Abraha& Joe L Mott - Digital Logic Design - World Scientific Publishing Co Ltd
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition

Flip Flops

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Objective

- Introduction to basic building blocks of memory in digital systems : FLIP-FLOPS

Introduction

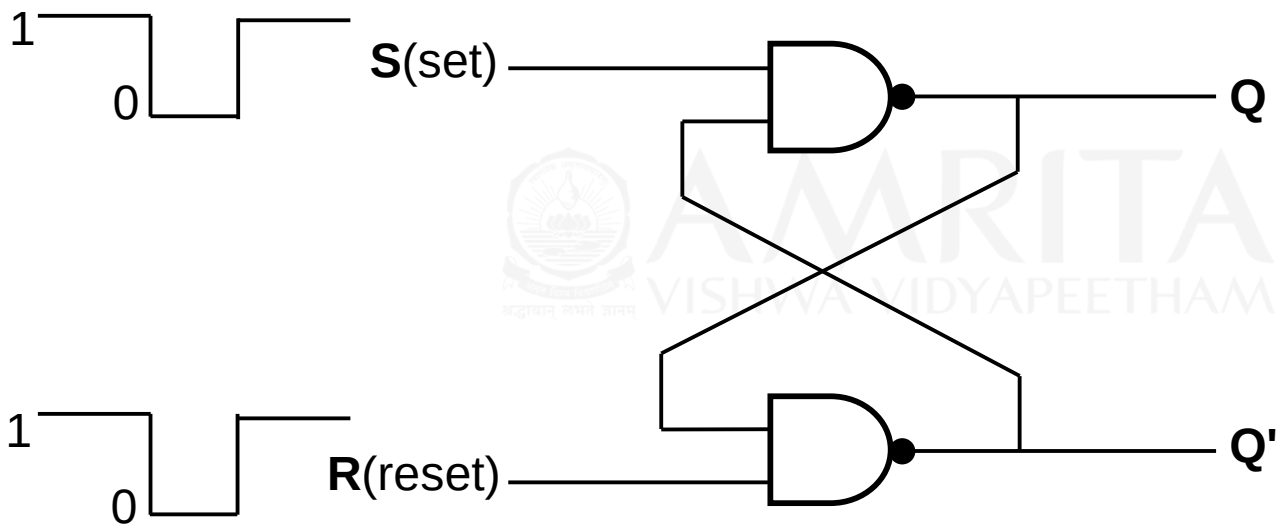
- **Flip-flops** are the building blocks of most sequential circuits.
- Flip-flops used as memory elements can store one bit of information.
- Clocked flip-flop serve as the memory element in synchronous sequential circuits.
- Unclocked flip-flops (latches) act as the memory element in asynchronous sequential circuits.
- Output in sequential circuit is from combinational circuit or flip-flop or both.

Basic Flip-flop circuits

- Flip-flops can be constructed using two NAND gates or two NOR gates.
- Cross-coupled connection from the output of one gate to the input of the other is the feedback path.
- 4 types of flip-flops : SR flip-flop, JK flip-flop, D flip-flop, T flip-flop.
- Application of flip-flop : Counters
  Shift Register
  Storage Register

SR latch with NAND gate

- Most basic sequential logic circuit with inputs “**SET**” (output = 1) and “**RESET**”(output = 0).



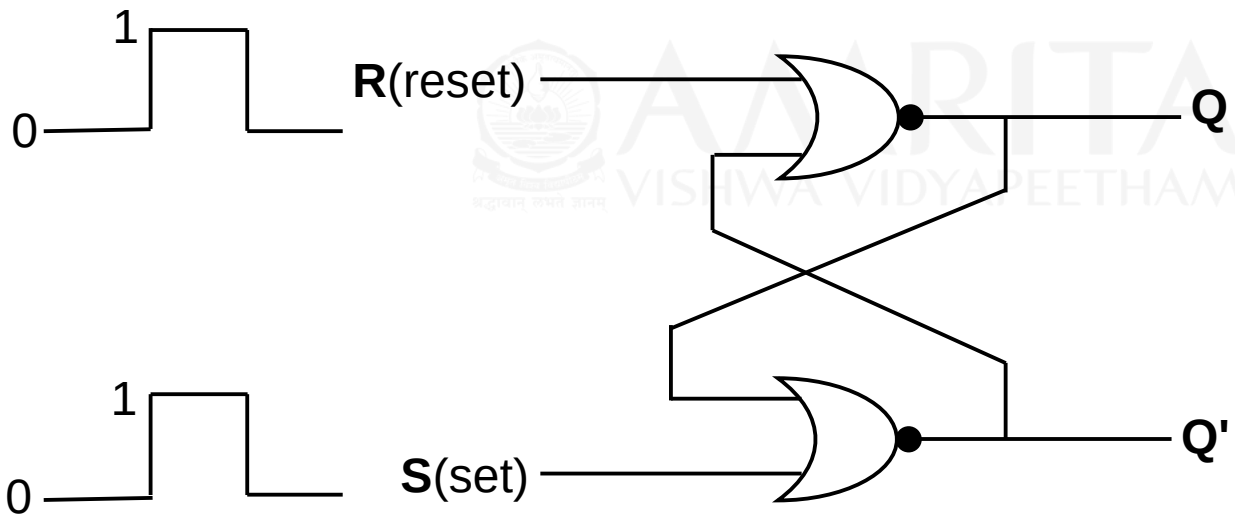
Logic diagram

Truth table

S	R	Q	Q'	
1	0	0	1	reset
1	1	0	1	No change
0	1	1	0	set
1	1	1	0	No change
0	0	-	-	undefined

For NAND gate, if any input is 0,output is 1
R = S =1 ;keep previous state

SR Latch with NOR gate



Logic diagram

Truth table

S	R	Q	Q'	
1	0	1	0	set
0	0	1	0	No change
0	1	0	1	reset
0	0	0	1	No change
1	1	-	-	undefined

For NOR gate, if any input is 1,output is 0
R = S =0 ;keep previous state

Summary

- Explained about fundamentals of flip-flops

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- Gideon Langholz, Abraha& Joe L Mott - Digital Logic Design - World Scientific Publishing Co Ltd
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition

Flip Flops-II

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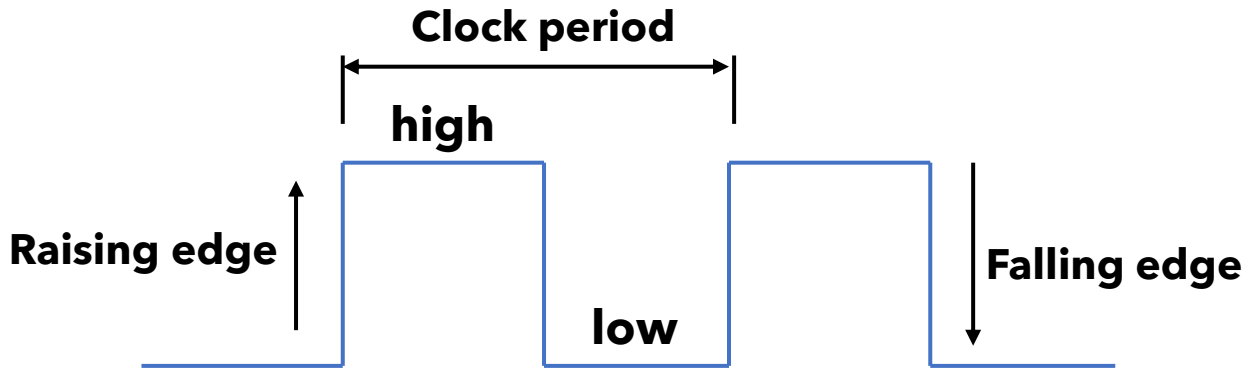
Objective

- Introduction to clocked flip-flops

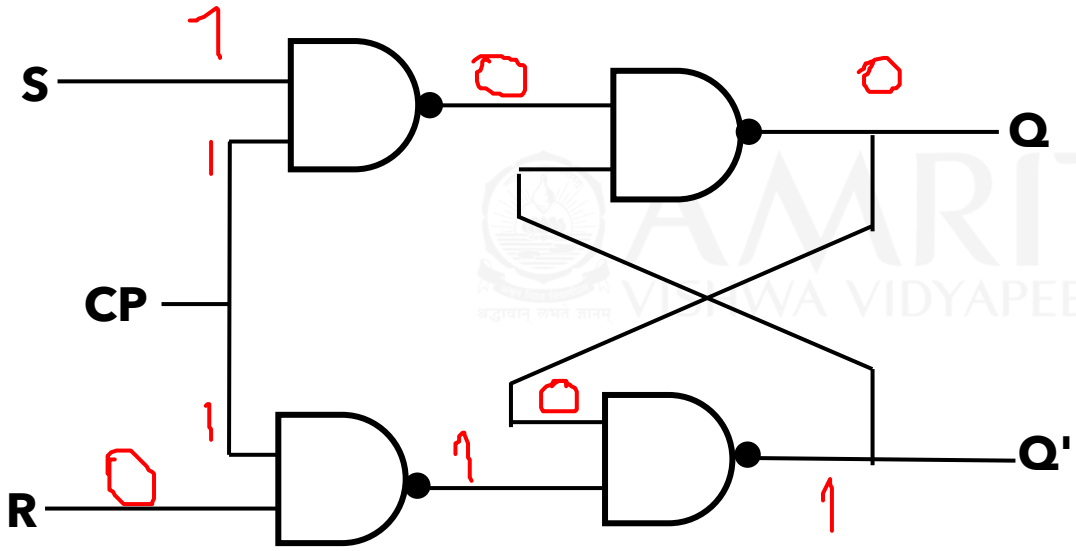
Clocked Flip-flops

- Operation of basic flip-flop can be modified by an additional control input which determine the change of state in circuit.
- Basic flip-flop circuits with additional NAND gates.
- Clock Pulse input act as the other inputs.



RS Flip-flop

- Basic flip-flop circuit with 2 additional NAND gates.



Logic diagram

Q	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

Characteristic table

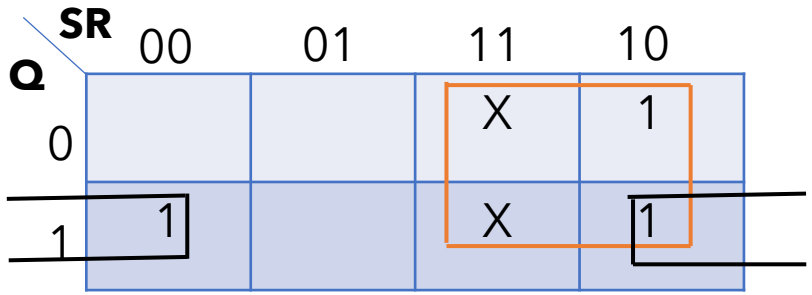
RS flip-flop

- Characteristic equation

$$Q_{t+1} = S + R'Q$$

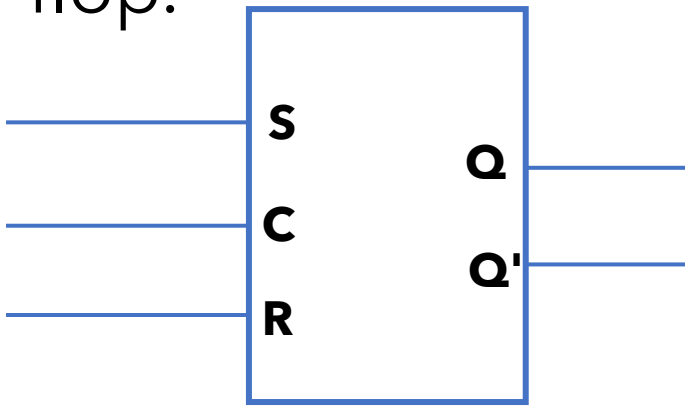
$$SR = 0$$

Next state = (present state, inputs)



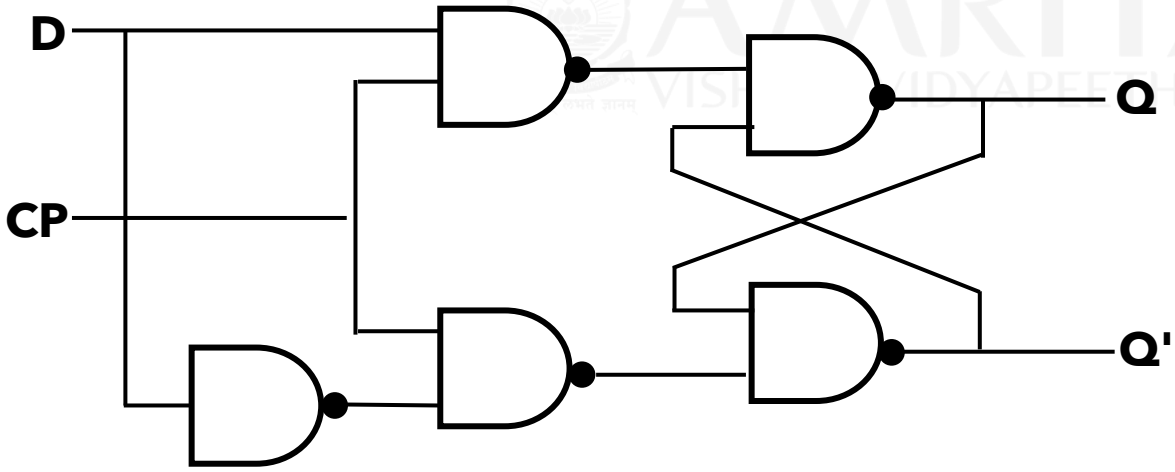
- Given present state and the inputs S, R of a single pulse in the input go to the next state Q_{t+1} in flip-flop.

Graphic symbol

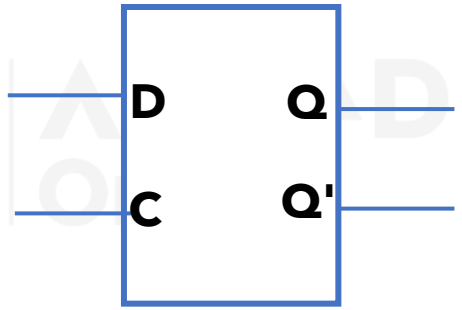


D Flip-flop

- To eliminate the intermediate state in RS flip-flop by never having value 1 to the inputs at the same time.
- Modification of RS flip-flop



Logic diagram



Graphic symbol

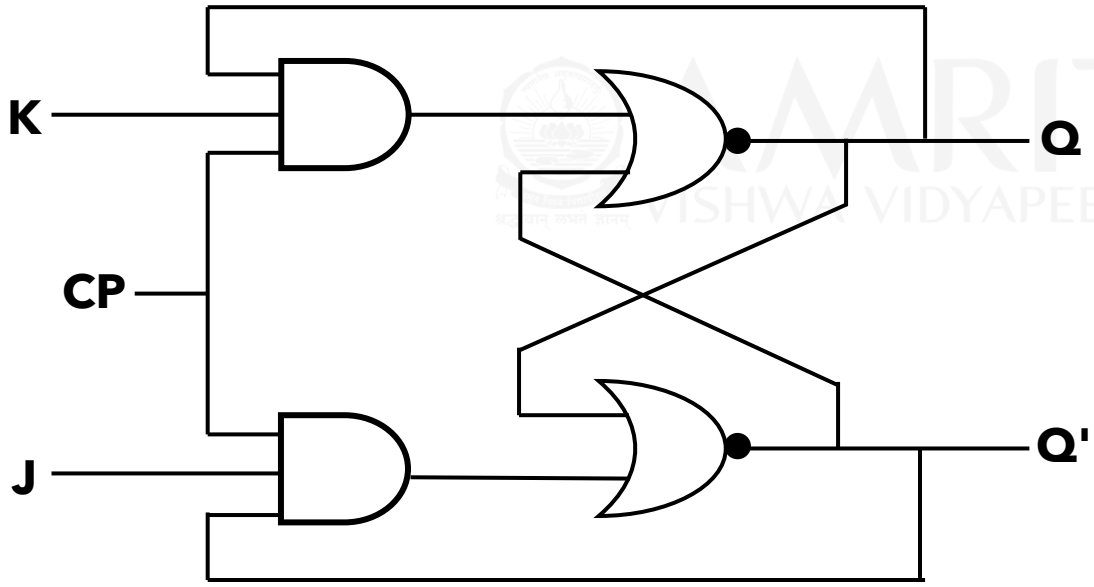
Q	D	Q_{t+1}	
0	0	0	
0	1	1	
1	0	0	reset
1	1	1	set

Q \ D	0	1
0		1
1		1

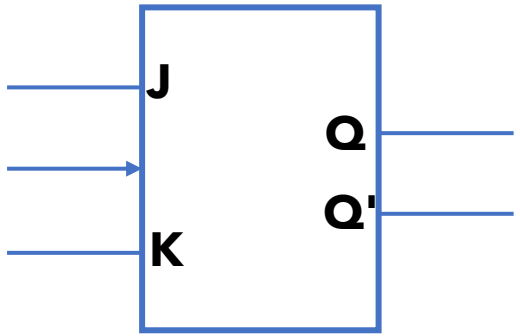
Characteristic equation, $Q_{t+1} = D$

JK Flip-flop

- Refinement of RS flip-flop with definition for the intermediate state is JK type.



Q	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

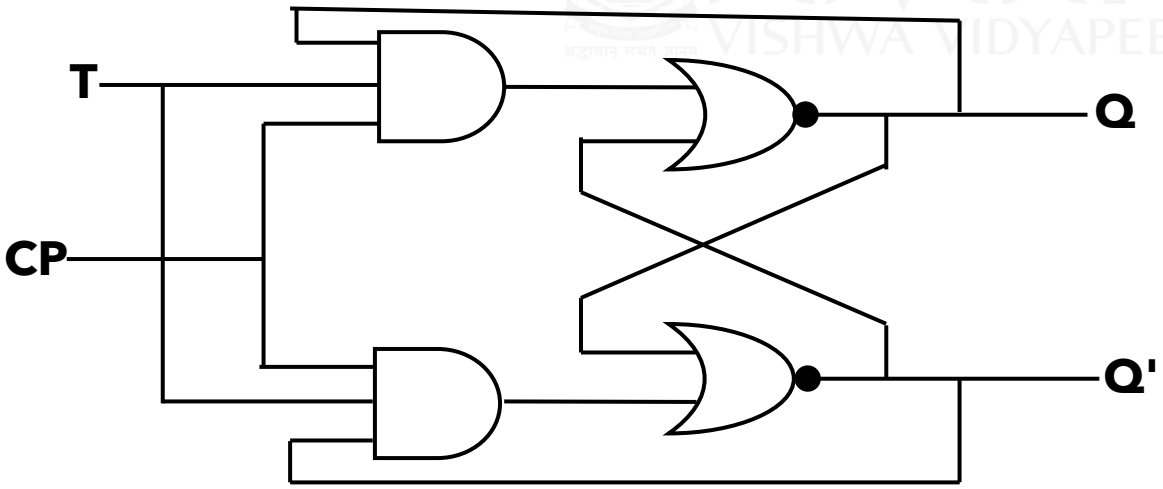


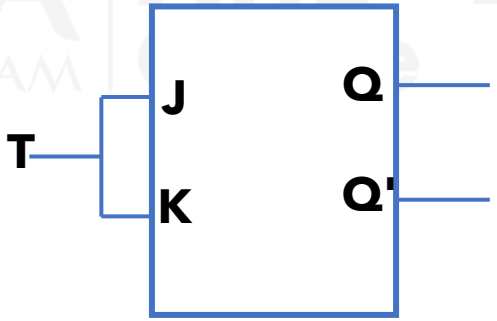
$Q_{t+1} = JQ' + K'Q$

- If J and K are both high at the clock edge, output will toggle from one state to the other

T flip-flop

- T means the ability of flip-flop to “toggle” or complement its state.
- Flip-flop complements its output when the clock pulse occurs while input is 1,regardless of present state.





Q	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0

$Q_{t+1} = TQ' + T'Q$
$= T \oplus Q$

Excitation Table

- Characteristic table specifies the next state of flip-flop given inputs and present state.
- Excitation table : For a particular transition to take place what should be the inputs.(if Q is 0 and to get Q' as 1 what should be the inputs)

Q	Q_{t+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

RS flip-flop

Q	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK flip-flip

Q	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D flip-flop

Q	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T flip-flop

Summary

- Basics of RS, D, T and JK flip-flops

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- Gideon Langholz, Abraha& Joe L Mott - Digital Logic Design - World Scientific Publishing Co Ltd
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition

Registers

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Objective

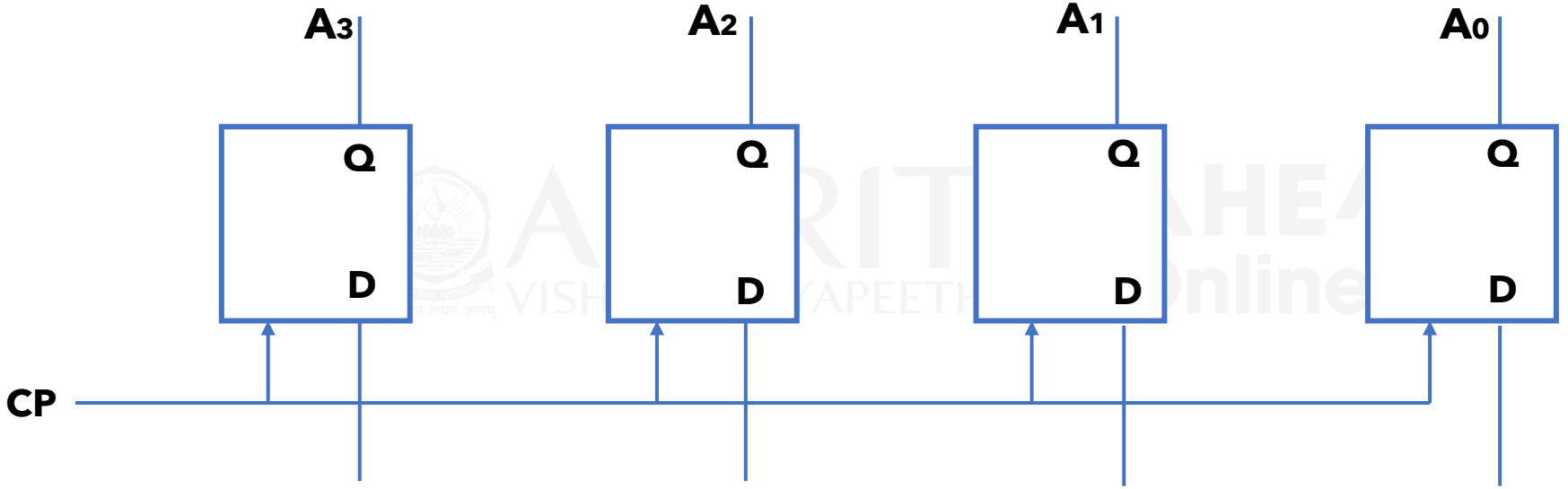
- Fundamentals about Registers

Introduction

- One flip-flop can store one bit of information.
- A group of flip-flops which can store multiple bits of information is called a **register**.
- Register is a device used to store information.
- **n-bit register** has a group of n flip-flops capable of storing n-bit binary information's .
- To store 16-bit data need a set of 16 flip-flops

Registers

- Simplest register consist of only flip-flops without any external gates.



4-bit register

4 D flip-flop + clock

- Clock pulse enables all flip-flops, so the information at four inputs can be transferred into the 4-bit register.

Shift Registers

- Binary data in a register can be moved within the register from one flip-flop to another.
- **Shift register** : Sequential logic circuit capable of storing and transferring of binary data.
- It can shift its binary data either to the right or to the left.
- Simplest possible shift register is the one with flip-flops only.

Shift register Operations

- There are four mode of operations of a shift register.
- ➢ Serial Input Serial Output (SISO)

Only 3 connections: Serial input (SI) to left flip-flop, serial output (SO) from right flip-flop and sequencing clock signal.

Operation:

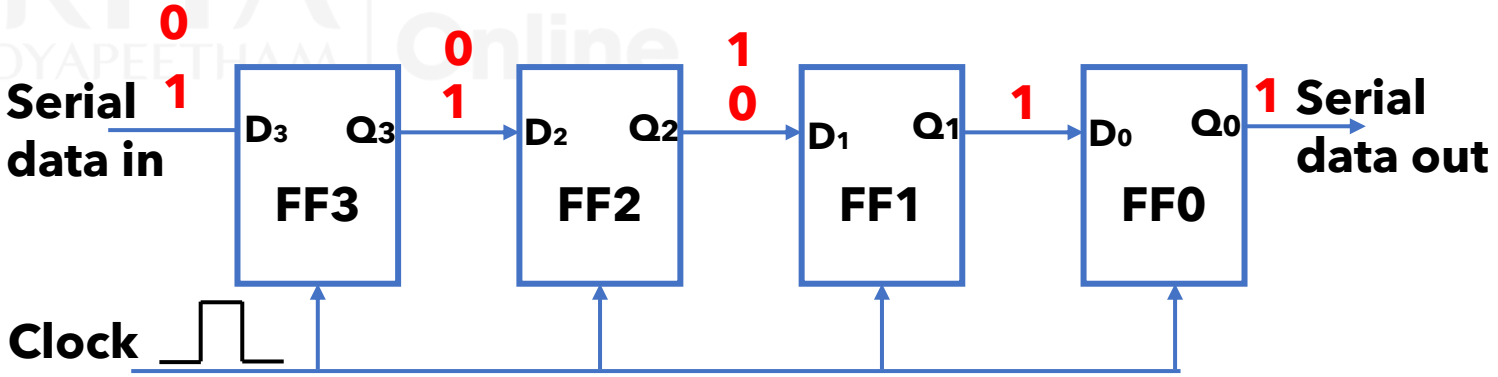
Initially $Q_3Q_2Q_1Q_0 = 0000$

IN = D_3 =1;Apply clock; FF3 set; Q_3=**1**

IN = 1; FF2 set;Q_3Q_2 = **1**1

IN = 0;FF1 set; $Q_3Q_2Q_1$ = **0**11

IN = 1; FF0 SET; $Q_3Q_2Q_1Q_0$ = **1**011



Act as temporary storage or time delay device

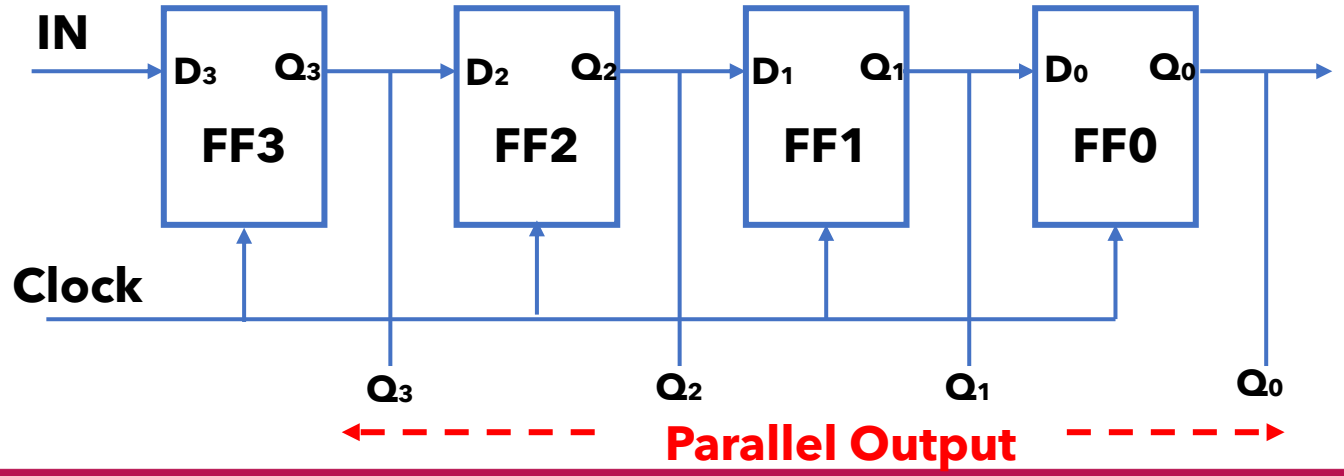
Mode of Operations

➢ Serial Input Parallel Output (SIPO)

- Data entered serially and taken out in parallel fashion.
- Data loaded bit by bit. Output disabled while data is loading.
- Once data loading completed, flip-flops contain the required data , outputs are enabled thus data is available at the same time.

4-bit word need clock cycles

Speed : SISO = SIPO



Mode of Operations

➢ Parallel Input Serial Output(PISO)

- Opposite of SIPO
- Data is loaded into the register in parallel format i.e., all data bits enter their input simultaneously.
- Data is outputted one bit in each clock cycle in a serial format.

➢ Parallel Input Parallel Output(PIPO)

- Data is loaded and unloaded in parallel format.
- One clock pulse loads and unloads the register.
- Also act as temporary storage or delay device as SISO.

Universal Shift Register

- Shift register capable of shifting in one direction is called unidirectional shift register.
- Shift register shifting in both direction are bi-directional shift register.
- Universal shift register : Shift data in both direction as well as load it parallelly.
- Operations: Parallel loading, Left shifting, Right shifting

Application of Registers

- Temporary data storage
- Data transfer
- Data manipulation
- As counters

Summary

- Explained about Registers

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- Gideon Langholz, Abraha& Joe L Mott - Digital Logic Design - World Scientific Publishing Co Ltd
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition

Counters

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Objective

- Counters
  - **Synchronous counter**
  - **Asynchronous counter**

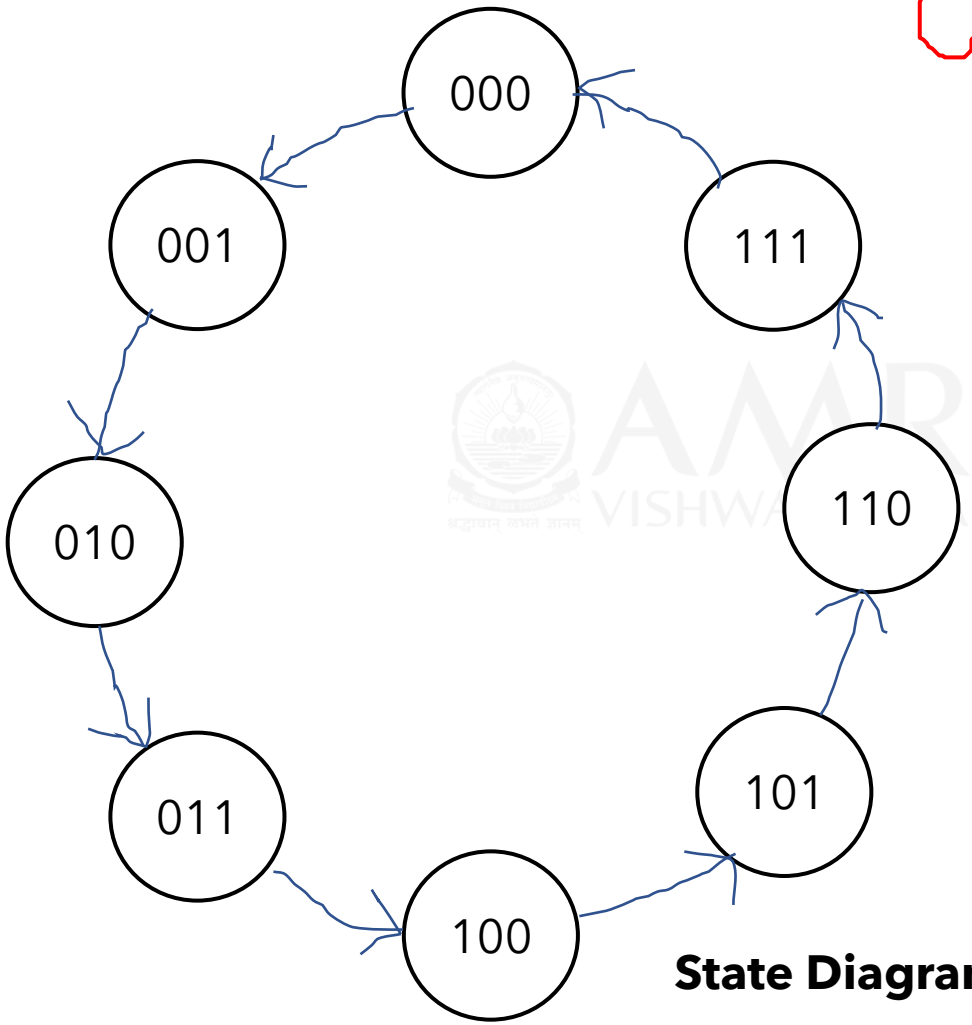
Introduction

- **Counter** is a sequential digital device used for counting(up or down).
- It is a group of flip-flops which outputs sequence of states on applying clock signal as input.
- **n-bit binary counter** consist of n flip-flops and count in binary from 0 to 2^n-1.

Types of counters

- Asynchronous Counter (Ripple counter)
- Synchronous Counter (Parallel counter)

Design of 3-bit Binary Counter



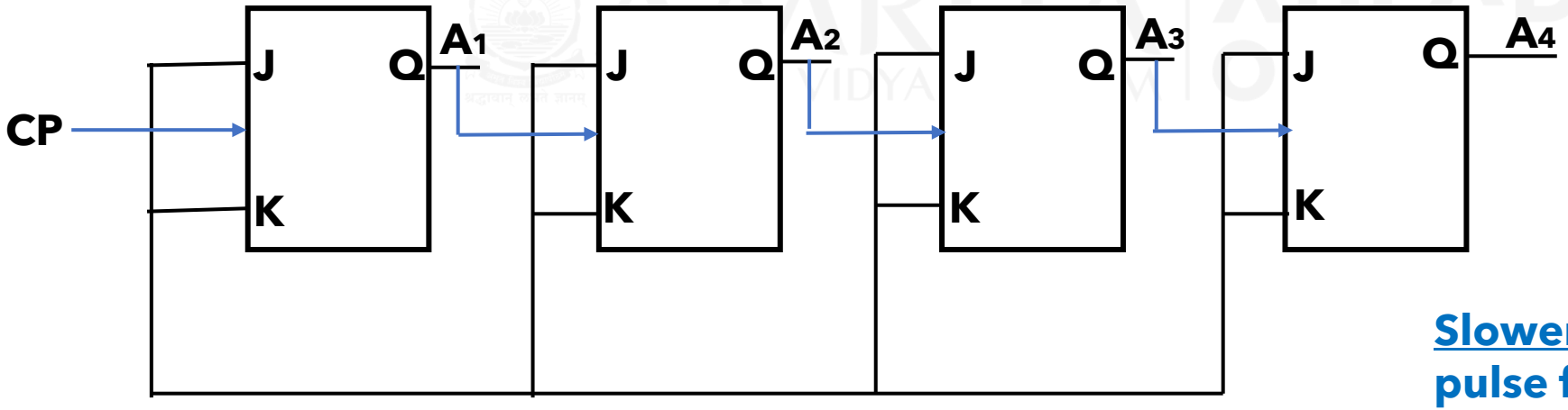
State Diagram

	P.State	N.State	
0	000	001	1
1	001	010	2
2	010	011	3
3	011	100	4
4	100	101	5
5	101	110	6
6	110	111	7
7	111	000	0

Excitation Table

Asynchronous Counter (Ripple Counter)

- The flip-flop output transition serves as the input for triggering other flip-flops. The input pulse is applied only to the first flip-flop.



4-bit binary ripple counter

Slower – delay in transmission of pulse from flip-flop to flip-flop

Synchronous counter

- Clock pulses are applied to the CP inputs of all flip-flops so the delay problem in ripple counter get solved.
- Common clock pulse triggers all the flip-flops simultaneously unlike ripple counter.
- Synchronous counters have a regular pattern and can be constructed by complementing the flip-flops and gates.
- Design is complex when compared to asynchronous counter.

Difference

Synchronous Counter	Asynchronous Counter
All flip-flops are triggered with same clock	Different clock is applied to different flip-flops
Faster	Slower
Design is complex	Design is comparatively easy
Any flip-flop can be used	All flip-flops are toggle flip-flops
Expensive	Less costly

Application of Counter

- Frequency counter
- Digital clocks
- Analog to digital converter
- Time measurements

Summary

- Explained about counters, different types of counters along with its application

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- Gideon Langholz, Abraha& Joe L Mott - Digital Logic Design - World Scientific Publishing Co Ltd
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition