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Combinational circuits

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Objective

Logic circuit

- Combinational circuit
- Sequential circuit

Digital Device **Logic gates**

Introduction

- Logic circuits for digital systems can be combinational or sequential.
- Combinational circuits consist of input variables, logic gates and output variables.
- Outputs are determined from the <u>present input states</u> not on previous states.

Block diagram of combinational circuit

n inputs -2^n input combinations

For each input combination, only one possible output.

Combinational Circuit Design

- The problem is stated
- The input and output variables are assigned letter symbols
- Truth table is derived
- The simplified Boolean function for each output are obtained
- The logic diagram is drawn.

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Combinational Circuits

- Adders
- Subtractors
- Comparators

Arithmetic and logic functions

- Decoders
- Encoders
- Multiplexers
- Demultiplexers

Data Transmission

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Adder

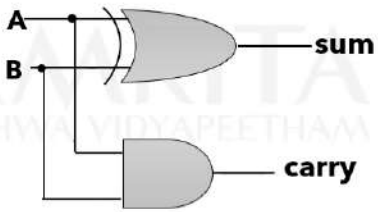
- Basic arithmetic operation in digital computer is binary addition.
- The combinational circuit which performs the addition of binary digits are called **adder**.
- **Half-adder** : Circuit performing the addition of 2 bits. 1/0 1/0
- **Full-adder** : Circuit performing the addition of 3 bits.
- Binary addition rules : **0+0 = 0 ; 0+1 = 1 ; 1+0 = 1 ; 1+1 = 0 with carry 1**

Half Adder

- 2 binary inputs augend and addend bits with 2 binary output called **sum** and **carry.**

inputs		outputs	
A	**B**	**sum**	**carry**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

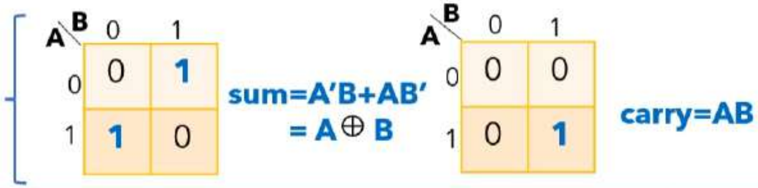
Truth table



Logic diagram

Block diagram

K-map simplification



Full Adder

- Arithmetic sum of 3 input bits where third bit is previous carry bit.

A \ BC	00	01	11	10
0	0	**1**	0	**1**
1	**1**	0	**1**	0

sum=A′B′C+A′BC′+AB′C′+ABC

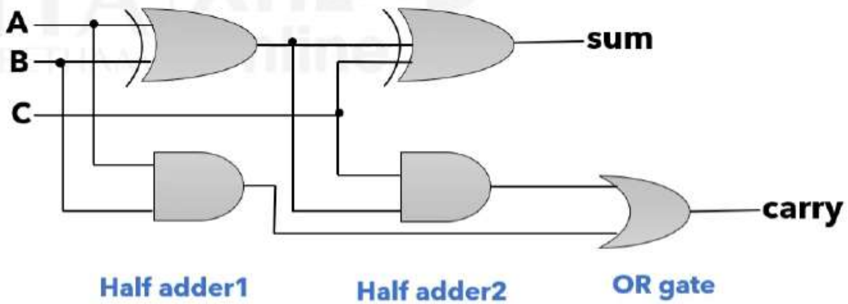
A \ BC	00	01	11	10
0	0	0	**1**	0
1	0	**1**	**1**	**1**

carry=AC+BC+AB

inputs			outputs	
A	**B**	C_{in}	**sum**	**carry**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder

- A full adder can be implemented with 2 half adders and 1 OR gate
- **sum** = $A'B'C+A'BC'+AB'C'+ABC$
  $= C\oplus(A\oplus B)$
- **carry** = $AB+BC+AC$
  $= AB+C(A\oplus B)$



Logic circuit of full adder

Summary

- Discussed basic arithmetic combinational circuits called adders

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Subtractors & Comparator

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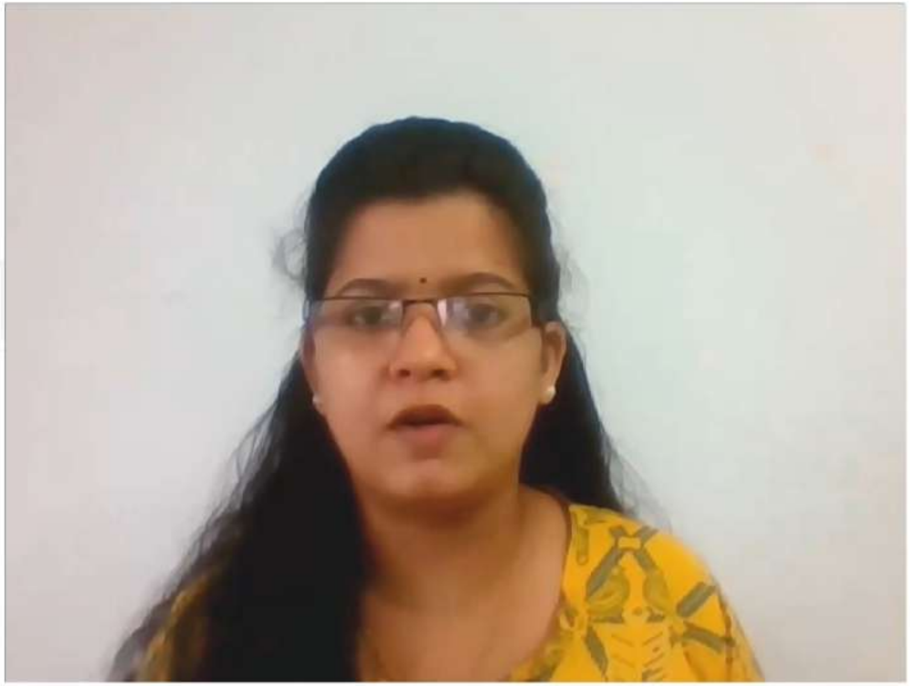
Objective

- ➢ Combinational circuits
- Subtractors
- Comparators



Subtractors

- Logic circuit to **subtract** binary numbers.
- Difference and borrow are the outputs.
- **Half subtractors** : circuit for subtracting 2 bits.
- **Full subtractors** : circuit for subtracting 3 bits.
- Binary subtractor rules : **0-0=0 ; 0-1=1 with borrow 1 ; 1-0=1 ; 1-1=0**

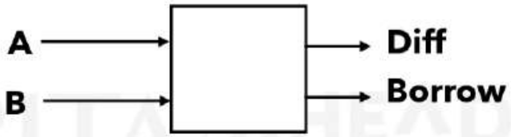
Half subtractors

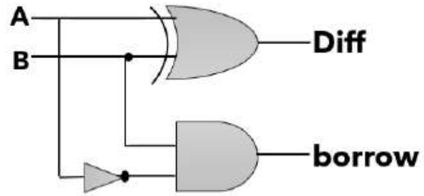
1/0 1/0

- 2 binary input bits with 2 binary output called difference and borrow.

inputs		outputs	
A	**B**	**diff**	**borrow**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

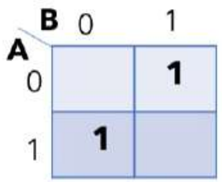
Truth table



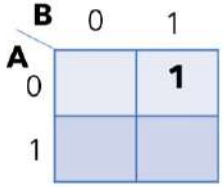


Logic diagram

Diff = A'B+AB'
= A⊕B



Borrow = A'B



K-map simplification

Full subtractors

- 3 inputs minuend, subtrahend, previous borrow with 2 outputs difference and borrow.

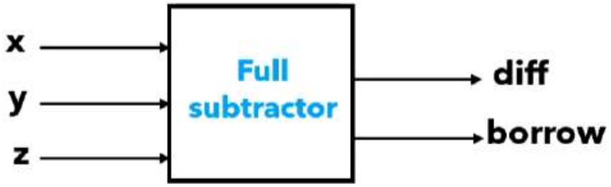
inputs			outputs	
x	**y**	**z**	**diff**	**borrow**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

x \ yz	00	01	11	10
0		1		1
1	1		1	

Diff = x'y'z + x'yz' + xy'z' + xyz

x \ yz	00	01	11	10
0		1	1	1
1			1	

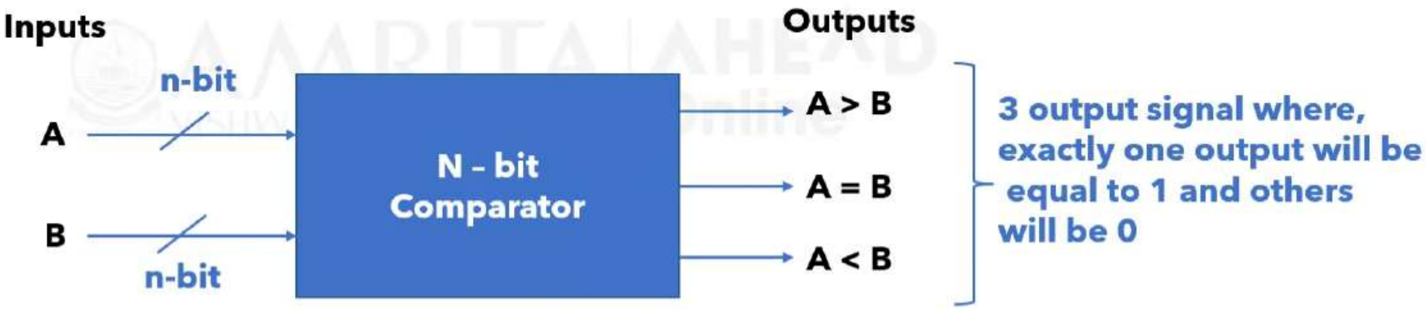
Borrow = x'z + yz + x'y



Block diagram

Magnitude Comparator

- A combinational circuit that compares two numbers A & B to determine whether: **A > B** or **A = B** or **A<B**



1-bit Comparator

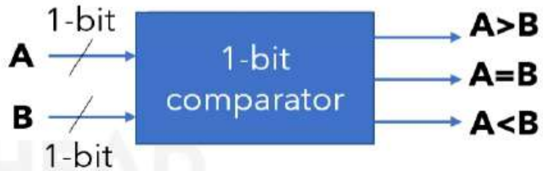
- To compare two single bit number

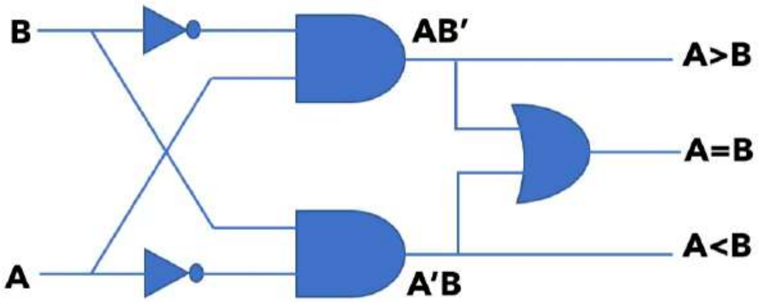
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

A>B : AB′

A=B : A′B′ + AB

A<B : A′B





Summary

- Explained combinational circuits called subtractors and comparators

Parallel adders & subtractors

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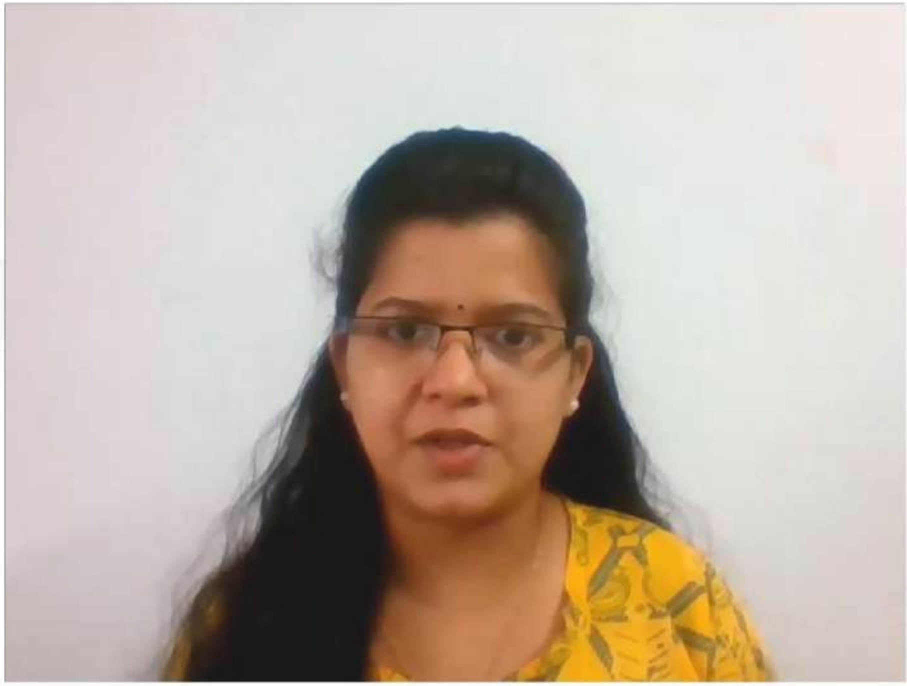
Objective

- Combinational circuits : Parallel adders and subtractors



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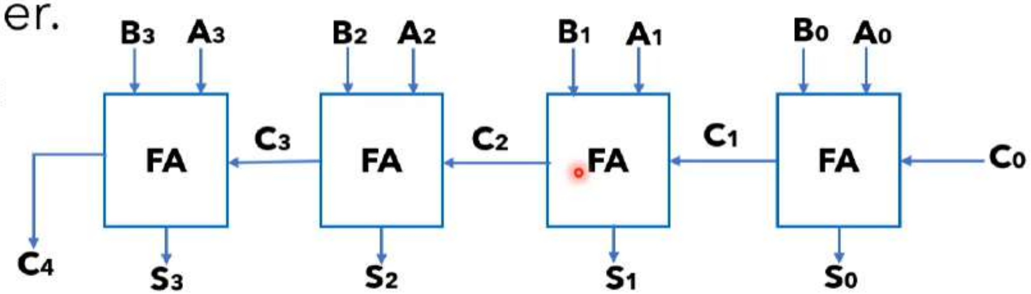
Binary Parallel Adder

- Digital circuit which perform the arithmetic addition of 2 binary numbers in parallel by <u>cascading full adders</u>.
- To add two n-bit binary numbers we need **n-bit binary adder**.
- Connect the carry output of each full adder to the carry input of the next full adder.

<u>4-bit binary adder</u>

$$\begin{array}{r} A_3\ A_2\ A_1\ A_0 \\ +\ B_3\ B_2\ B_1\ B_0 \end{array}$$



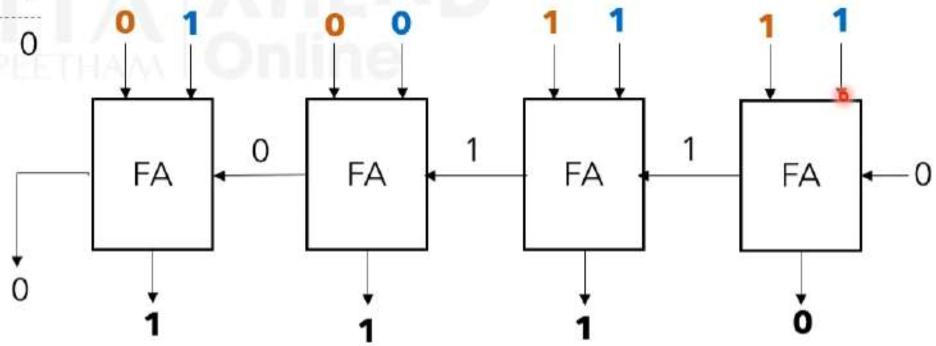
4-bit binary adder example

- Addition of decimal numbers 11 and 3

Augend	11
Addend	3
sum	14
Carry	0

Binary addition

	MSB			LSB
Augend(Ai)	1	0	1	1
Addend(Bi)	0	0	1	1
Carry (Ci)	0	1	1	0
Sum(Si)	1	1	1	0
Carry out	0			

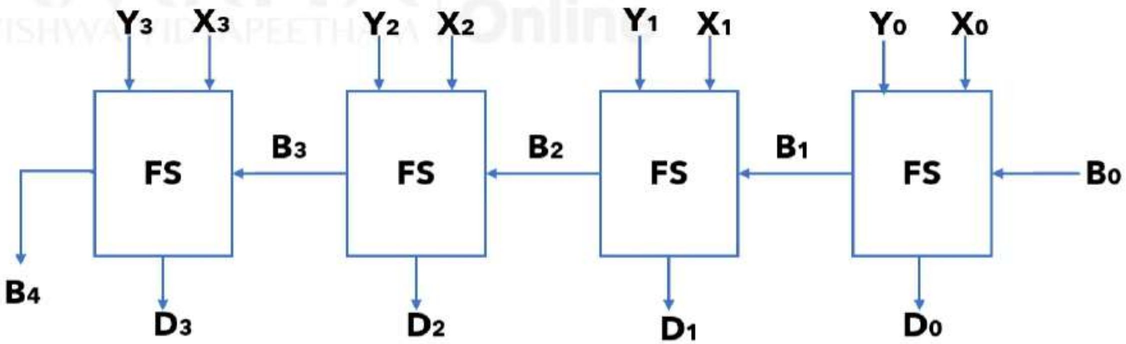


Binary Parallel Subtractor

- Digital circuit which perform the arithmetic subtraction of 2 binary numbers in parallel by <u>cascading full subtractors.</u>

- Binary adder can also be used to perform binary subtraction.

<u>4-bit binary subtractor</u>



Summary

- Explained how to perform n-bit binary numbers arithmetic operations using Parallel adders and subtractors

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Data Transmission circuits

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Objective

➢ Data transmission circuits

- Decoders
- Encoders
- Multiplexers
- Demultiplexers

Decoders

- n-bit binary number can represent maximum 2^n distinct elements of coded information.

  e.g., 3-bit : 8 elements (000 – 111)

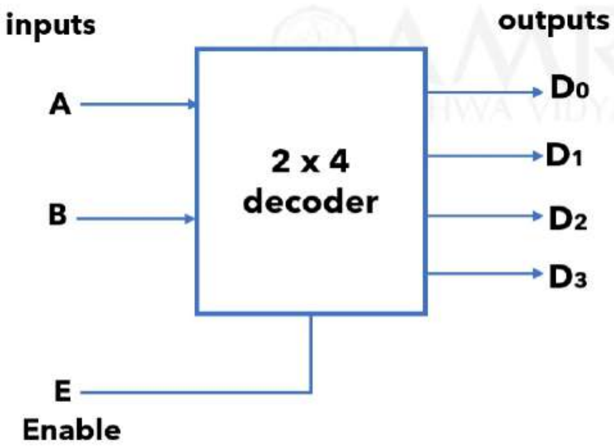
- **Decoder** is a combinational circuit with n input lines and maximum of 2^n output lines.

- One of the output will be high based on the combination of input lines.

- Translate coded information from one format to another

Decoders

- Decoder represented as **n x 2^n** provides the 2^n minterms of n input variables.

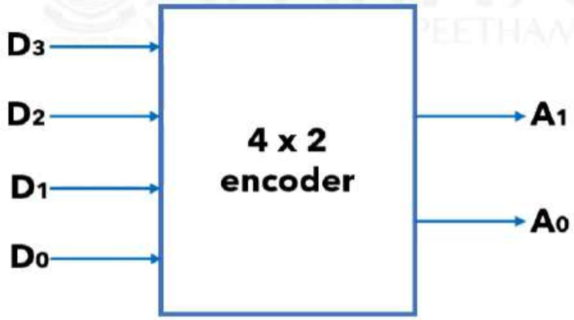


Enable	inputs		outputs			
E	A	B	D_0	D_1	D_2	D_3
0	x	x	0	0	0	0
1	0	0	**1**	0	0	0
1	0	1	0	**1**	0	0
1	1	0	0	0	**1**	0
1	1	1	0	0	0	**1**

Out of 4 outputs, only one input combination is high when enabled

Encoders

- Encoders are combinational circuit that performs the reverse operation of decoders.
- It has 2^n input lines and n output lines.



inputs				outputs	
D_3	D_2	D_1	D_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

A0 = D3 + D1 **A1 = D2 + D3**

Priority Encoder

- An encoder circuit with priority function.
- If two or more inputs are equal to 1 at the same time, the input with **highest priority** will be considered.
- After K-map simplification

$A_1 = D_2 + D_3$

$A_0 = D_3 + D_1 D_2'$

$v = D_0 + D_1 + D_2 + D_3$

inputs				outputs		
D_3	D_2	D_1	D_0	A_1	A_0	v
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

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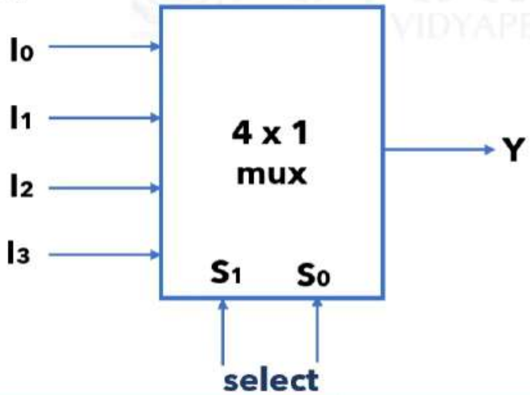
Multiplexers

- Combinational circuit with 2^n **input lines**, **n selection lines** whose bit combination determine input to be selected and a **single output line**.

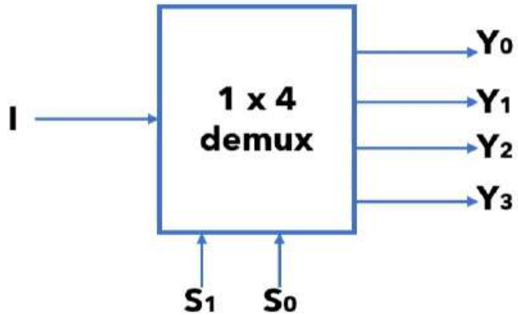
- Also called data selector, since it selects one of many inputs and outputs.



S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

De-multiplexers

- Combinational circuit that performs the reverse operation of multiplexer.
- It has one input line , n select lines to choose one output out of 2^n possible output lines.



S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	**1**
0	1	0	0	**1**	0
1	0	0	**1**	0	0
1	1	**1**	0	0	0

Summary

- Discussed data transmission combinational circuits