CPU Organization

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Objective

- Covers different types of CPU organization

CPU Organization

- Computer performs a task based on the instruction with different fields.
- Common fields are operation field ,address field and mode field.

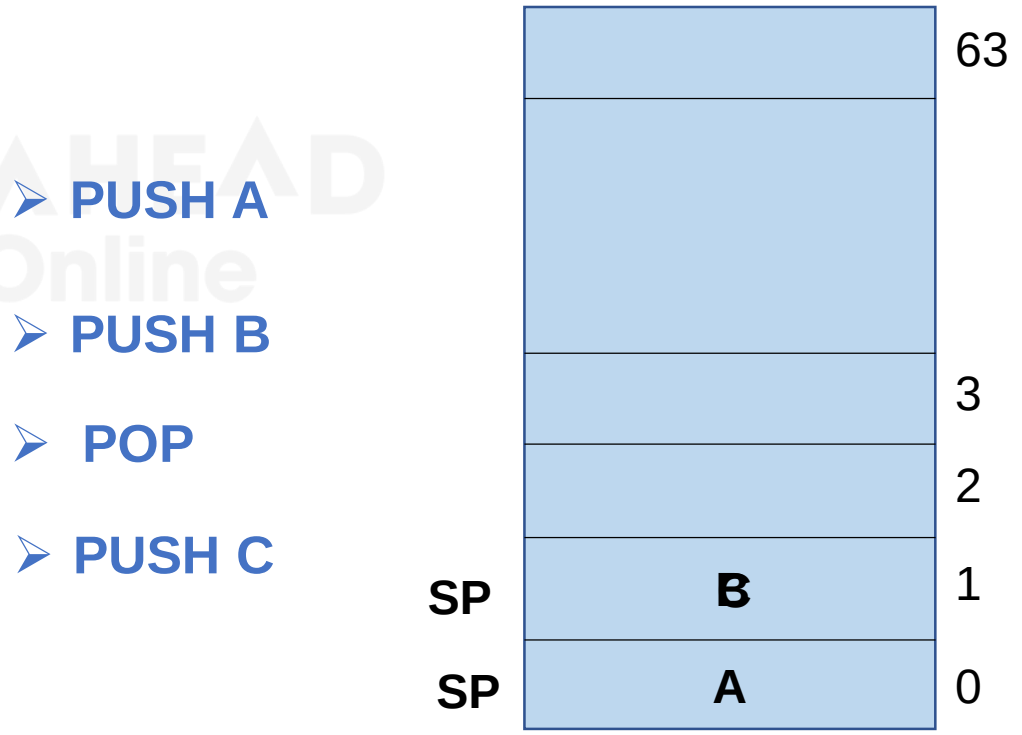
- Instruction is of variable length depending on the number of addresses it contain.
- Multiple CPU organization based on the number of address field

Stack CPU organization

- In stack CPU organization all the arithmetic and logic operations are done using stacks.
- Stack is a storage device that stores information in such a manner that the item stored last is the first item retrieved.
- 2 operations of stack : **Push** – New item inserted to top of stack
  Pop – Removing the top element
- Main memory have pre-defined space for allocating the ALU stack.

Stack

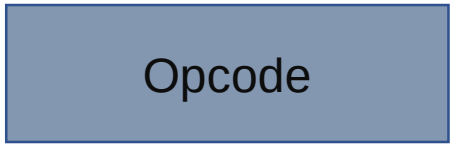
- LIFO - Item stored last is the first item retrieved.
- Stack Pointer(SP) – Register that holds the address for stack with values pointing to top item.
- 2 operations Push(insertion) and Pop(deletion).
- Stack can be a Register stack or memory stack.



Zero address Instruction

- In stack CPU organization all ALU instructions (MUL, ADD, SUB etc.) are **zero address instruction**.
- Non-ALU instruction need not be zero address instructions.

  i.e., MOV A, 2080 (executing in stack CPU but not zero address instn)
- In zero address instruction only operation field (opcode) no address field.



I1 : MOV A, 2080

I2 : MOV B, 2090

I3 : PUSH A

I4 : PUSH B

I5 : MUL

I6 : POP C

Zero address instruction

- Instruction cycle : **MUL**

- Fetch : Read MUL from memory to CPU based on PC location by the control unit.

- Execute : Interpret the opcode – MUL (2 operands)

  POP (pop B and store it in accumulator)

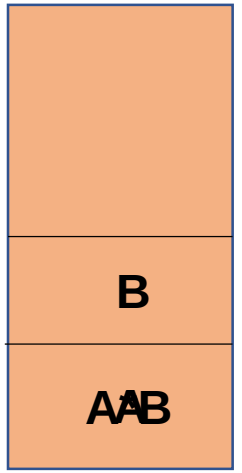
  Before next pop operation copy value in acc to TR

  POP (pop A and store in acc)

  MUL (ALU reads the data from acc and TR & perform A*B)

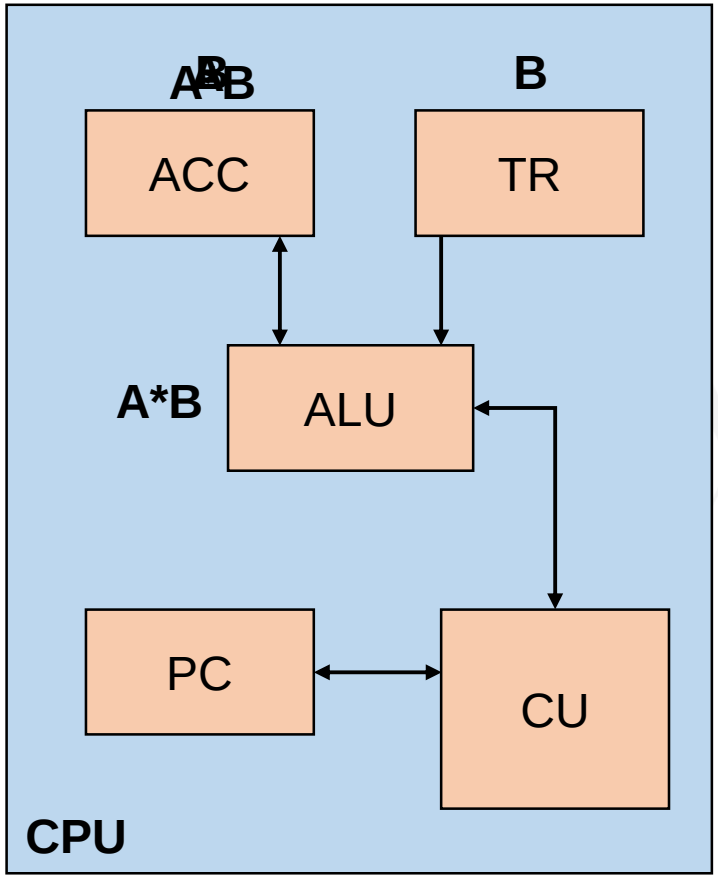
  Resultant value is stored back in accumulator

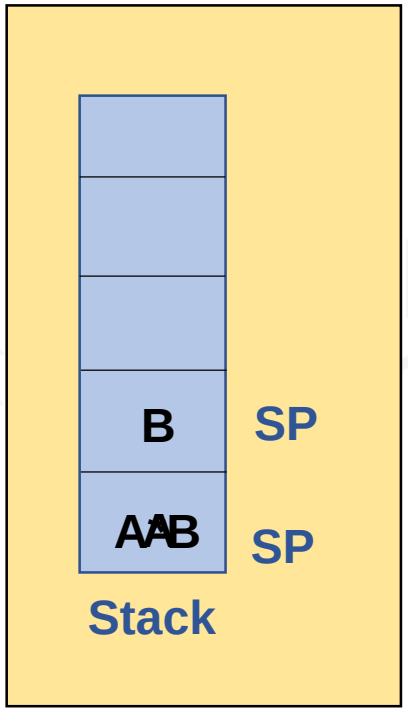
  PUSH (push A*B value to the stack top)



Stack

Stack CPU organization





Memory

Expression C = A*B

I1 : MOV A, 2080

I2 : MOV B, 2090

Copy from memory to registers A, B

I3 : PUSH A

I4 : PUSH B

I5 : MUL (zero address instruction)

I6 : POP C

Summary

- Discussed about Stack based CPU organization

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- P Pal Chaudhuri - Computer Organization and Design - PHI - Second Edition
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition

Accumulator CPU Organization

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Objective

- Introduction to Accumulator CPU organization
- One address instruction

Accumulator CPU Organization

- Uses an implied accumulator (AC) register for all data manipulation.
- Called accumulator CPU -1st operand always in accumulator and result stored back to accumulator.
- 2nd operand can be in memory or in GPR.
- MUL 2090 **one address instruction** (1 address field-operand)

opcode **operand**

One address instruction

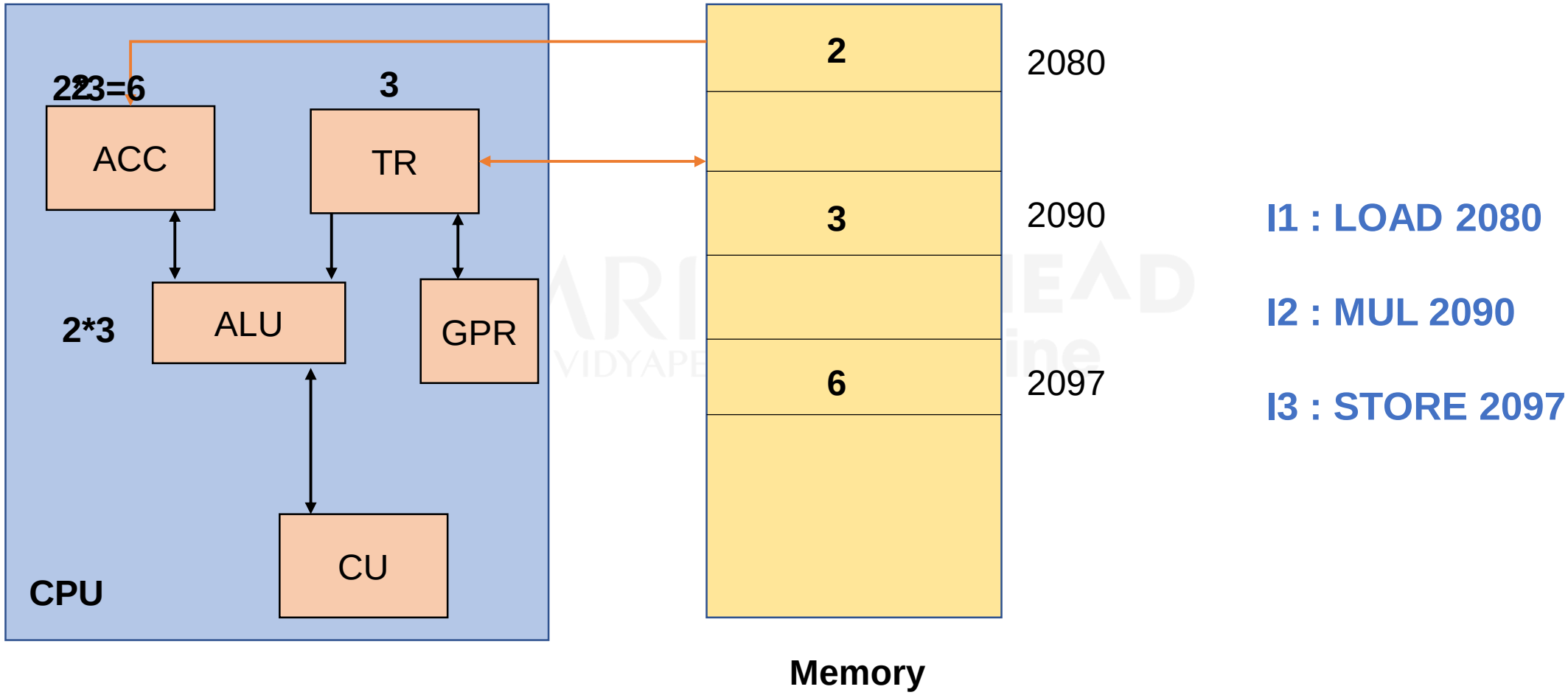
- Instruction cycle : **MUL 2090**
- Fetch : Read MUL and 2090 from memory
- Execute : Interpret the opcode (MUL is one address instruction with 1 operand in acc and 2nd operand in memory location 2090)

TR ← M [2090] (whatever in 2090 copy it to TR)

Multiply in ALU (1 operand in acc and 2nd operand in TR)

ACC ← ACC * M [2090] (Result is stored in accumulator)

Accumulator CPU organization



I1 : LOAD 2080

I2 : MUL 2090

I3 : STORE 2097

One address Instruction

- Example : **X ← (A + B) * (C + D)**

LOAD	A	AC ← M[A]
ADD	B	AC ← AC + M[B]
STORE	T	M[T] ← AC
LOAD	C	AC ← M[C]
ADD	D	AC ← AC + M[D]
MUL	T	AC ← AC * M[T]
STORE	X	M[X] ← AC

Summary

- Explained about accumulator CPU organization along with one address instruction

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
- P Pal Chaudhuri - Computer Organization and Design - PHI - Second Edition
- Thomas C Bartee - Digital Computer Fundamentals - Tata Mc Graw Hill - Sixth Edition

General Purpose Register CPU Organization

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Objective

- Basics of General Purpose Register CPU Organization

General Purpose Register CPU Organization

- Registers are the memory location within CPU.
- General register CPU organization of 2 types :

Register-memory Reference Architecture (CPU with less number register)
One operand in register and other operand can be present either in register or memory.

Register-register reference architecture (CPU with more registers)
Operands are placed in registers.
After manipulation, the result also stored back in register

Register-memory Reference Architecture

- A collection of registers from R0 to Rn-1 called register file.
- ALU picks first operand from these registers, second operand from memory and result stored back in register.
- E.g. : ADD R0, 2080 **two address instruction**

opcode

Operand 1

Operand 2

Register value

Memory address

Two address instruction

- I1 : **ADD R0 , 2080**

- Fetch : Read opcode and operands form memory

- Execute : Interpret opcode ADD (for addition need 2 operands)

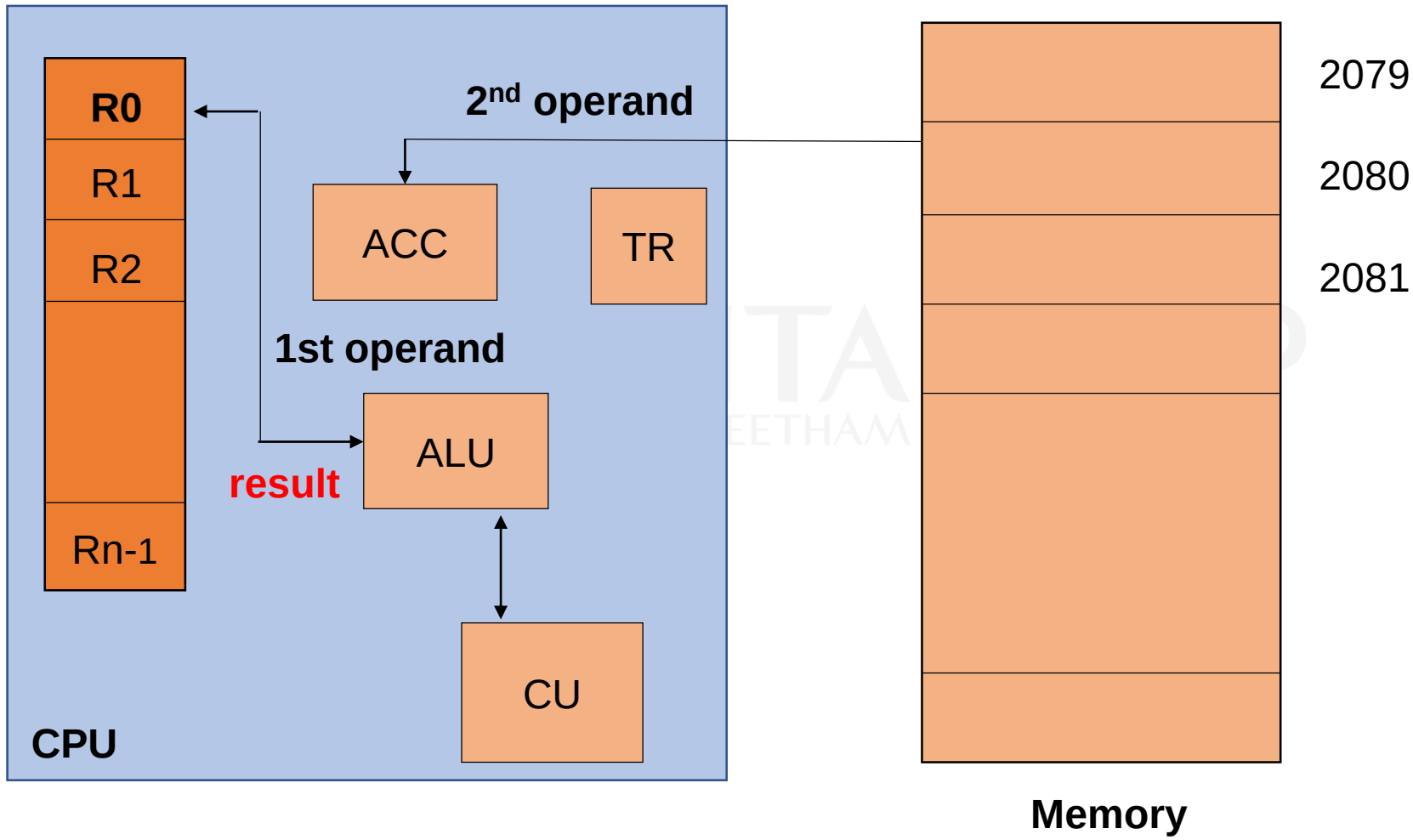
ALU⟵ M[2080] (fetch content from memory location 2080 the 2nd operand place it as input to ALU)

ADD R0 + M[2080]

⟵

R0 R0 + M[2080] (Result stored back in R0)

Register-memory Reference Architecture

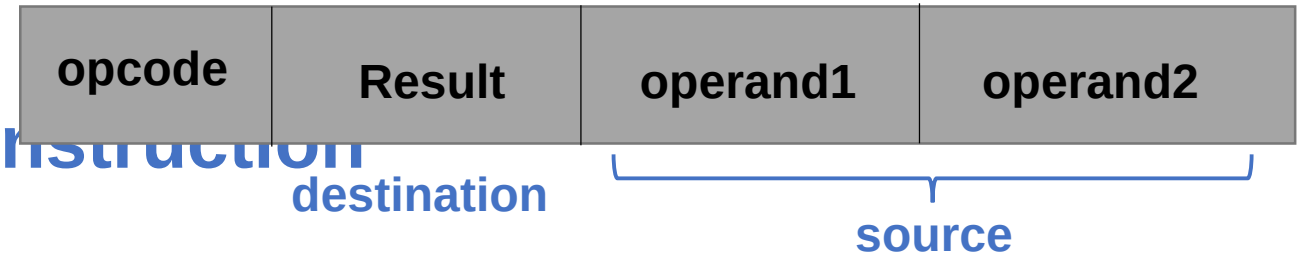


I1 : ADD R0, 2080

Register-register reference organization

- Both operands are from register file.
- ALU takes two inputs from the register and result is stored back in another register.
- E.g., ADD R0, R1, R2 (R0 ← R1 + R2)

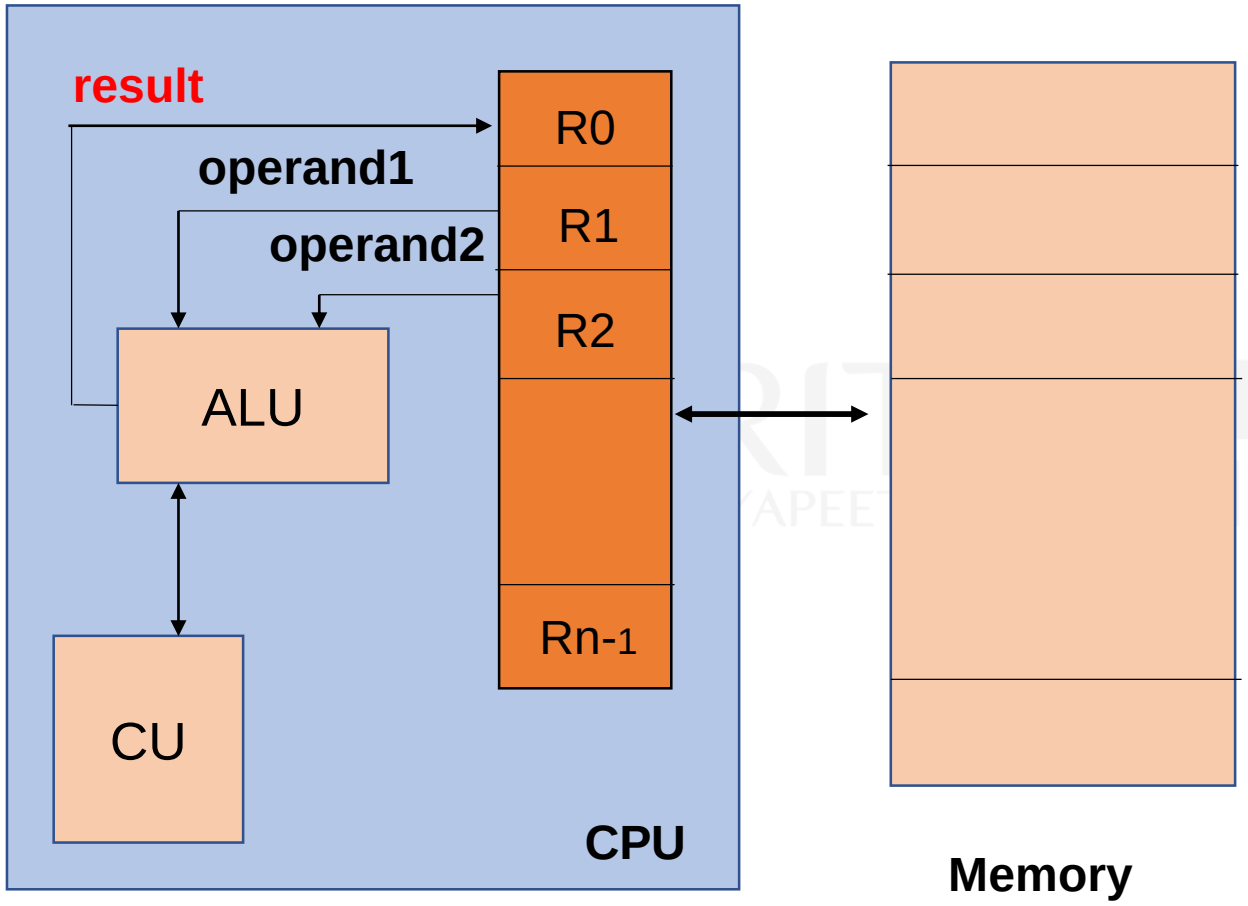
result operand1 operand2



Three address

(1 destination address & 2 source address)

Register-register reference organization



I1 : ADD R0, R1, R2

Data loaded to register file from main memory using **LOAD** & **STORE** instruction.

LOAD : CU loads data from memory to register

STORE : CU stores data from register to memory.

Summary

- Explained about general purpose register CPU organization

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
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Instruction Set

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Objective

- Discuss about set of all instructions a microprocessor has

Introduction

- The ISA (Instruction Set Architecture) define the type of instructions to be supported by processor.
- The instruction set provides commands to the processor, to tell it what it needs to do.
- 3 types of instructions :

  Data transfer instructions

  Data manipulation instructions

  Transfer of control instructions

Data transfer instruction

- Instruction responsible for transfer of instruction from memory to the processors register and vice-versa.

Instruction	Definition
MOV	Transfer word/byte from memory to register and vice-versa
PUSH	Transfer byte from source to top of stack
POP	Transfer word from stack top to destination
LOAD	Transfer from memory to other location
STORE	Transfer from a location to memory

Data manipulation instruction

- Arithmetic and logical operation performed by ALU.

Instruction	Definition
Arithmetic	ADD, SUB, MUL, DIV, INC, DEC
Logical	AND, OR, NOT, XOR
Shift	Shift the binary data to right or left within the memory location

Transfer of control instruction

- Transfer the control from one instruction to another for execution.
- There are 2 types of such instructions:

  Unconditional transfer instructions – No condition to be checked before transferring control

  CALL, RET

  Conditional transfer instructions – Condition need to be checked before control transfer

  JZ, JNZ

Summary

- Explained about Instruction Set

Reference

- M Morris Mano - Computer System Architecture - PHI - Third Edition
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Computer Architecture Fundamentals

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Objective

- Covers fundamental concepts

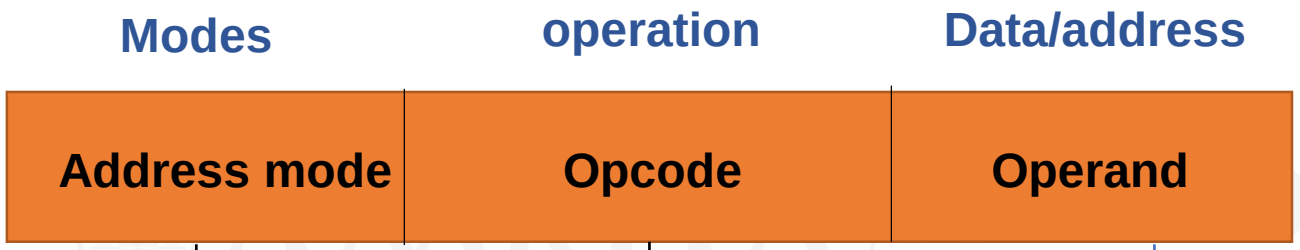
Computer Program

- Set of program statements also called program instructions.
- Program instructions are machine instructions in binary format that CPU can directly execute.
- OS loads machine instruction to main memory RAM to initiate execution.
- The control unit decodes the machine instructions as per instruction format

Instruction Set Architecture

- CPU executes the machine instruction by repetitively performing machine cycle.
- The set of instructions implemented by the CPU is called Instruction Set Architecture (ISA).
- Instruction format defines the structure of program instruction that can be executed by CPU.
- Instruction format consist of OPCODE, OPERAND and addressing mode

Instruction Format



Operation to be performed by CPU while executing instruction

Rule for the CPU while operating on the OPERAND part of machine instruction

The data on which the CPU performs the desired operation

Instruction cycle

- Machine cycle is a part of instruction cycle.
- The CPU might perform number of machine cycles to execute one single instruction.

Fetch : CPU fetch data and instruction from RAM

Decode : Control Unit decodes the instruction

Execute : ALU executes instructions & operates on data

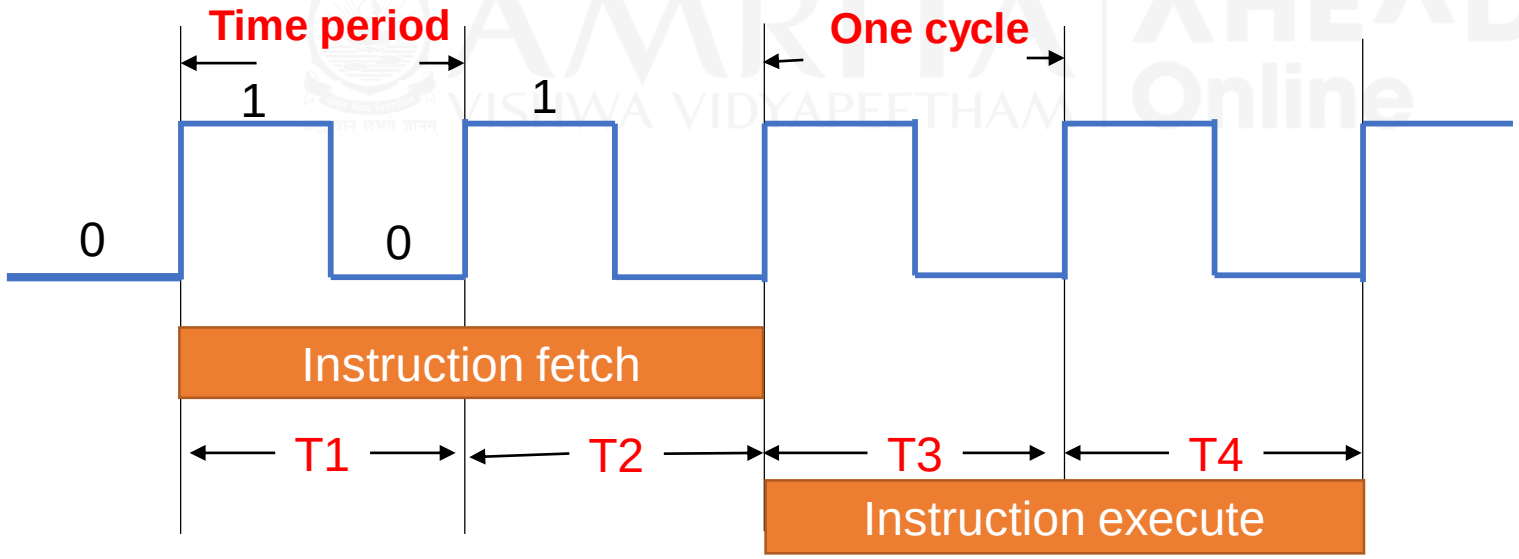
Store : Processed data is stored in RAM

Computer Function

- Basic function performed by computer is the execution of program (set of instructions) stored in memory.
- Processor reads (*fetches*) instructions from memory one at a time and *executes* each instruction.
- The processing required for a single instruction is called an instruction cycle.
- The 2 main steps of an instruction cycle is fetch cycle and execute cycle.

Instruction cycle

- The processor is driven by an internal clock.
- The clock generates a stream of clock pulses and for each clock cycle CPU completes a part of execution process.



Summary

- Explained some basic concepts.

Reference

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