VERSION HISTORY

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Revision Description Date Drawn Checked Approved

Ver 2.0 Release Version 2020-12-4

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P03 POWER TREE

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P06 POWER2

P07 SOC

P08 FLASH

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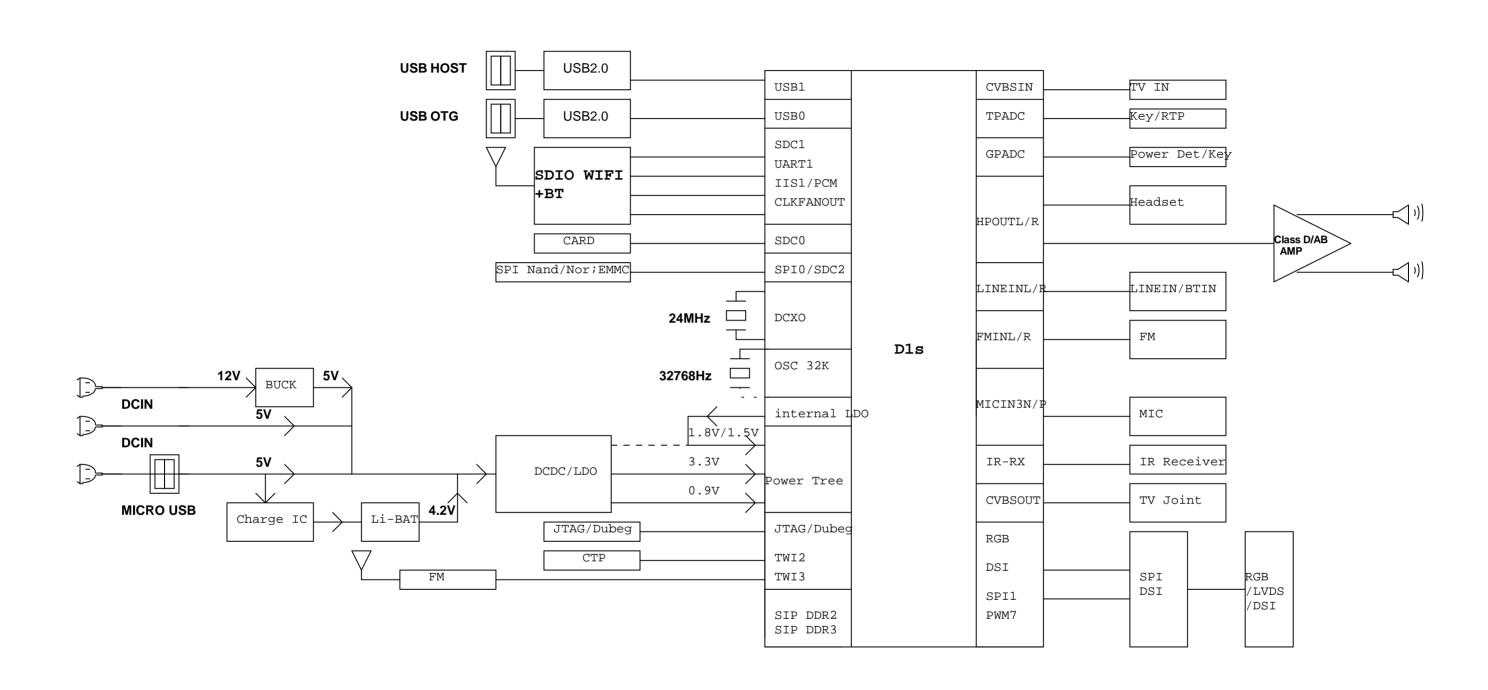
P10 AUDIO

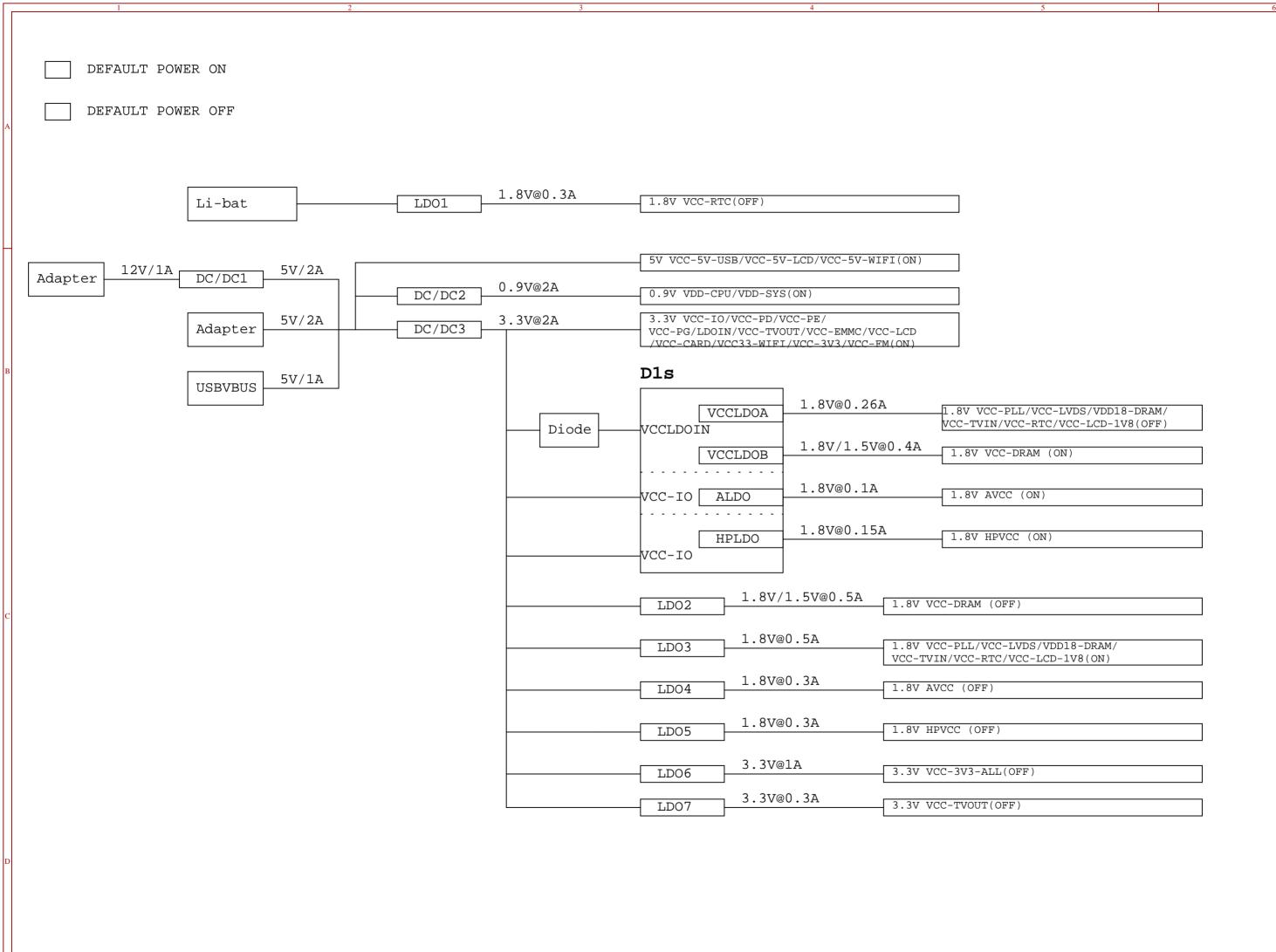
P11 CARD USB

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BLOCK





GPIO ASSIGNMENT

Pin Number	Pin Name	GPIO Multiplex Function
86	PB2	LCD0_D0/I2S2_DOUT2/TWI0_SDA/I2S2_DIN2/LCD0_D18/UART4_TX/PB_EINT2
85	PB3	LCD0_D1/I2S2_DOUT1/TWI0_SCK/I2S2_DIN0/LCD0_D19/UART4_RX/PB_EINT3
84	PB4	LCD0_D8/I2S2_DOUT0/TWI1_SCK/I2S2_DIN1/LCD0_D20/UART5_TX/PB_EINT4
82	PB5	LCD0_D9/I2S2_BCLK/TWI1_SDA/PWM0/LCD0_D21/UART5_RX/PB_EINT5
80	PB6	LCD0_D16/I2S2_LRCK/TWI3_SCK/PWM1/LCD0_D22/UART3_TX/CPUBIST0/PB_EINT6
79	PB7	LCD0_D17/I2S2_MCLK/TWI3_SDA/IR_RX/LCD0_D23/UART3_RX/CPUBIST1/PB_EINT7

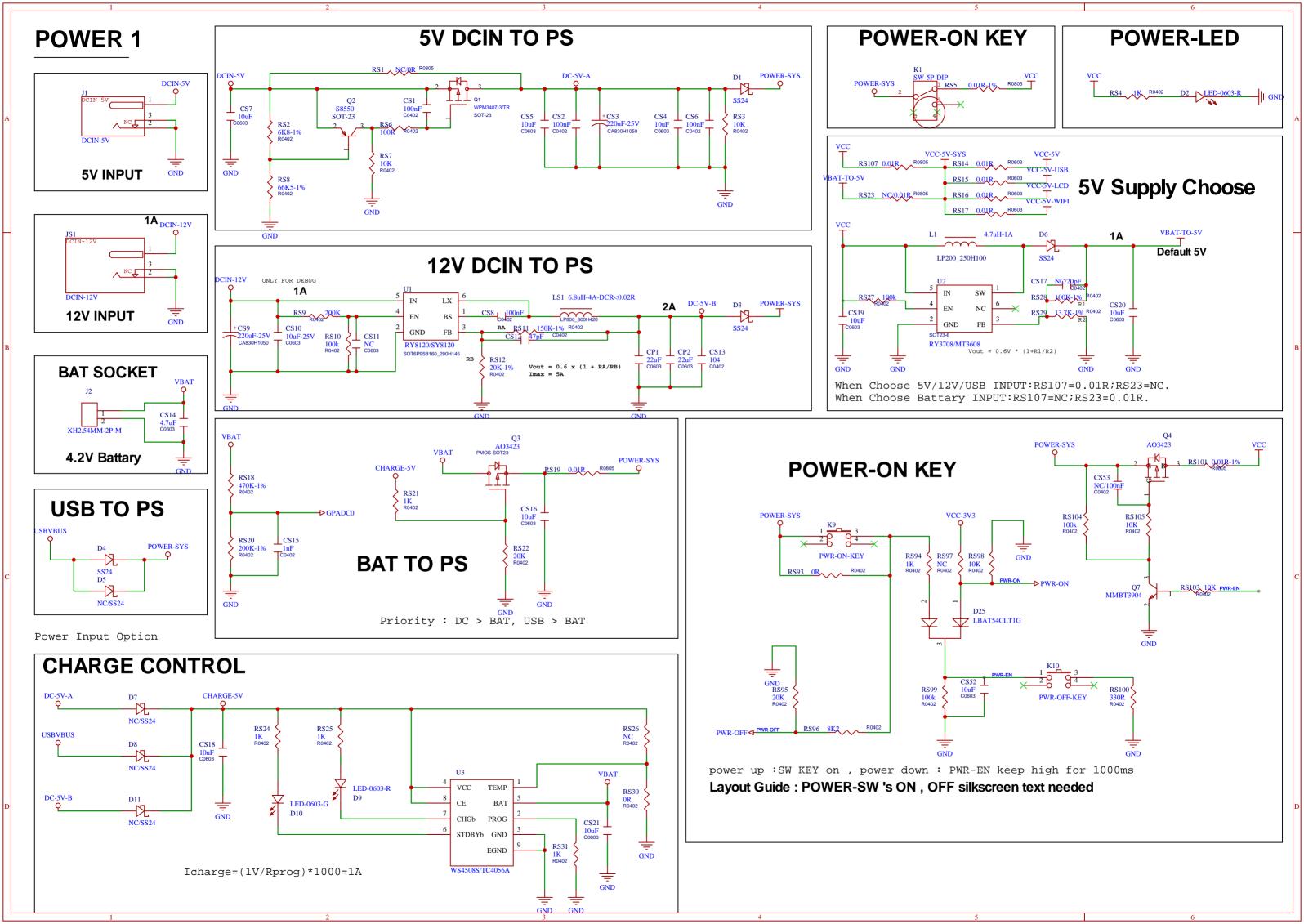
Pin Number	Pin Name	GPIO Multiplex Function
19	PC2	SPIO_CLK/SDC2_CLK/PC_EINT2
18	PC3	SPIO_CSO/SDC2_CMD/PC_EINT3
17	PC4	SPIO_MOSI/SDC2_D2/BOOT_SEL0/PC_EINT4
16	PC5	SPIO_MISO/SDC2_D1/BOOT_SEL1/PC_EINT5
15	PC6	SPIO_WP/SDC2_D0/UART3_TX/TWI3_SCK/DBG_CLK/PC_EINT6
14	PC7	SPIO_HOLD/SDC2_D3/UART3_RX/TWI3_SDA/TCON_TRIG/PC_EINT7

Pin Number	Pin Name	GPIO Multiplex Function
55	PD0	LCD0_D2/LVDS0_V0P/DSI_D0P/TWI0_SCK/PD_EINT0
56	PD1	LCD0_D3/LVDS0_V0N/DSI_D0N/UART2_TX/PD_EINT1
57	PD2	LCD0_D4/LVDS0_V1P/DSI_D1P/UART2_RX/PD_EINT2
58	PD3	LCD0_D5/LVDS0_V1N/DSI_D1N/UART2_RTS/PD_EINT3
59	PD4	LCD0_D6/LVDS0_V2P/DSI_CKP/UART2_CTS/PD_EINT4
60	PD5	LCD0_D7/LVDS0_V2N/DSI_CKN/UART5_TX/PD_EINT5
61	PD6	LCD0_D10/LVDS0_CKP/DSI_D2P/UART5_RX/PD_EINT6
62	PD7	LCD0_D11/LVDS0_CKN/DSI_D2N/UART4_TX/PD_EINT7
63	PD8	LCD0_D12/LVDS0_V3P/DSI_D3P/UART4_RX/PD_EINT8
64	PD9	LCD0_D13/LVDS0_V3N/DSI_D3N/PWM6/PD_EINT9
67	PD10	LCD0_D14/LVDS1_V0P/SPI1_CS/DBI_CSX/UART3_TX/PD_EINT10
68	PD11	LCD0_D15/LVDS1_V0N/SPI1_CLK/DBI_SCLK/UART3_RX/PD_EINT11
70	PD12	LCD0_D18/LVDS1_V1P/SPI1_MOSI/DBI_SD0/TWI0_SDA/PD_EINT12
69	PD13	LCD0_D19/LVDS1_V1N/SPI1_MISO/DBI_SDI/DBI_TE/DBI_DCX/UART3_RTS/PD_EINT1
71	PD14	LCD0_D20/LVDS1_V2P/SPI1_HOLD/DBI_DCX/DBI_WRX/UART3_CTS/PD_EINT14
72	PD15	LCD0_D21/LVDS1_V2N/SPI1_WP/DBI_TE/IR_RX/PD_EINT15
73	PD16	LCD0_D22/LVDS1_CKP/DMIC_DATA3/PWM0/PD_EINT16
74	PD17	LCD0_D23/LVDS1_CKN/DMIC_DATA2/PWM1/PD_EINT17
75	PD18	LCD0_CLK/LVDS1_V3P/DMIC_DATA1/PWM2/PD_EINT18
76	PD19	LCD0_DE/LVDS1_V3N/DMIC_DATA0/PWM3/PD_EINT19
54	PD20	LCD0_HSYNC/TWI2_SCK/DMIC_CLK/PWM4/PD_EINT20
53	PD21	LCD0_VSYNC/TWI2_SDA/UART1_TX/PWM5/PD_EINT21
52	PD22	SPDIF_OUT/IR_RX/UART1_RX/PWM7/PD_EINT22

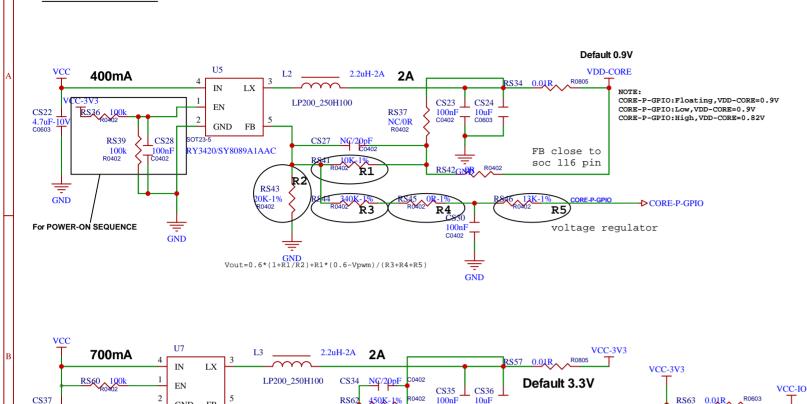
Pin Number	Pin Name	GPIO Multiplex Function
7	PF0	SDC0_D1/JTAG_MS/R_JTAG_MS/I2S2_DOUT1/I2S2_DIN0/PF_EINT0
8	PF1	SDC0_D0/JTAG_DI/R_JTAG_DI/I2S2_DOUT0/I2S2_DIN1/PF_EINT1
9	PF2	SDC0_CLK/UART0_TX/TWI0_SCK/LEDC_DO/SPDIF_IN/PF_EINT2
10	PF3	SDC0_CMD/JTAG_DO/R_JTAG_DO/I2S2_BCLK/PF_EINT3
11	PF4	SDC0_D3/UART0_RX/TWI0_SDA/PWM6/IR_TX/PF_EINT4
12	PF5	SDC0_D2/JTAG_CK/R_JTAG_CK/I2S2_LRCK/PF_EINT5
13	PF6	SPDIF_OUT/IR_RX/I2S2_MCLK/PWM5/PF_EINT6

Pin Numbe	r Pin Name	GPIO Multiplex Function
44	PE0	NCSIO_HSYNC/UART2_RTS/TWI1_SCK/LCDO_HSYNC/
		RGMII_RXCTRL/RMII_CRS_DV/PE_EINT0
45	PE1	NCSIO_VSYNC/UART2_CTS/TWI1_SDA/LCDO_VSYNC/
		RGMII_RXD0/RMII_RXD0/PE_EINT1
35	PE2	NCSIO_PCLK/UART2_TX/TWIO_SCK/CLK_FANOUT0/UART0_TX/
		RGMII_RXD1/RMII_RXD1/PE_EINT2
33	PE3	NCSIO_MCLK/UART2_RX/TWIO_SDA/CLK_FANOUT1/UARTO_RX/
		RGMII_TXCK/RMII_TXCK/PE_EINT3
43	PE4	NCSIO_DO/UART4_TX/TWI2_SCK/CLK_FANOUT2/D_JTAG_MS/R_JTAG_MS/
		RGMII_TXD0/RMII_TXD0/PE_EINT4
42	PE5	NCSIO_D1/UART4_RX/TWI2_SDA/LEDC_DO/D_JTAG_DI/R_JTAG_DI/
		RGMII_TXD1/RMII_TXD1/PE_EINT5
41	PE6	NCSIO_D2/UART5_TX/TWI3_SCK/SPDIF_IN/D_JTAG_DO/R_JTAG_DO/
		RGMII_TXCTRL/RMII_TXEN/PE_EINT6
40	PE7	NCSIO_D3/UART5_RX/TWI3_SDA/SPDIF_OUT/D_JTAG_CK/R_JTAG_CK/
		RGMII_CLKIN/RMII_RXER/PE_EINT7
39	PE8	NCSIO_D4/UART1_RTS/PWM2/UART3_TX/JTAG_MS/MDC/PE_EINT8
38	PE9	NCSIO_D5/UART1_CTS/PWM3/UART3_RX/JTAG_DI/MDIO/PE_EINT9
37	PE10	NCSIO_D6/UART1_TX/PWM4/IR_RX/JTAG_DO/EPHY_25M/PE_EINT10
36	PE11	NCSIO_D7/UART1_RX/I2SO_DOUT3/I2SO_DIN3/JTAG_CK/RGMII_TXD2/PE_EINT11
32	PE12	TWI2_SCK/NCSI0_FIELD/I2S0_DOUT2/I2S0_DIN2/RGMII_TXD3/PE_EINT12
31	PE13	TWI2_SDA/PWM5/I2S0_DOUT0/I2S0_DIN1/DMIC_DATA3/RGMII_RXD2/PE_EINT13

Pin Number	Pin Name	GPIO Multiplex Function
120	PG0	SDC1_CLK/UART3_TX/RGMII_RXCTRL/RMII_CRS_DV/PWM7/PG_EINT0
118	PG1	SDC1_CMD/UART3_RX/RGMII_RXD0/RMII_RXD0/PWM6/PG_EINT1
119	PG2	SDC1_D0/UART3_RTS/RGMII_RXD1/RMII_RXD1/UART4_TX/PG_EINT2
121	PG3	SDC1_D1/UART3_CTS/RGMII_TXCK/RMII_TXCK/UART4_RX/PG_EINT3
123	PG4	SDC1_D2/UART5_TX/RGMII_TXD0/RMII_TXD0/PWM5/PG_EINT4
122	PG5	SDC1_D3/UART5_RX/RGMII_TXD1/RMII_TXD1/PWM4/PG_EINT5
1	PG6	UART1_TX/TWI2_SCK/RGMII_TXD2/PWM1/PG_EINT6
2	PG7	UART1_RX/TWI2_SDA/RGMII_TXD3/SPDIF_IN/PG_EINT7
3	PG8	UART1_RTS/TWI1_SCK/RGMII_RXD2/UART3_TX/PG_EINT8
4	PG9	UART1_CTS/TWI1_SDA/RGMII_RXD3/UART3_RX/PG_EINT9
5	PG10	PWM3/TWI3_SCK/RGMII_RXCK/CLK_FANOUT0/IR_RX/PG_EINT10
6	PG11	I2S1_MCLK/TWI3_SDA/EPHY_25M/CLK_FANOUT1/TCON_TRIG/PG_EINT11
124	PG12	<pre>i2s1_lrck/twi0_sck/rgmii_txctrl/rmii_txen/clk_fanout2/ pwm0/uart1_tx/pg_eint12</pre>
125	PG13	I2S1_BCLK/TWI0_SDA/RGMII_CLKIN/RMII_RXER/PWM2/ LEDC_DO/UART1_RX/PG_EINT13
126	PG14	I2S1_DIN0/TWI2_SCK/MDC/I2S1_DOUT1/SPI0_WP/UART1_RTS/PG_EINT14
127	PG15	I2S1_DOUT0/TWI2_SDA/MDIO/I2S1_DIN1/SPI0_HOLD/UART1_CTS/PG_EINT15



POWER 2

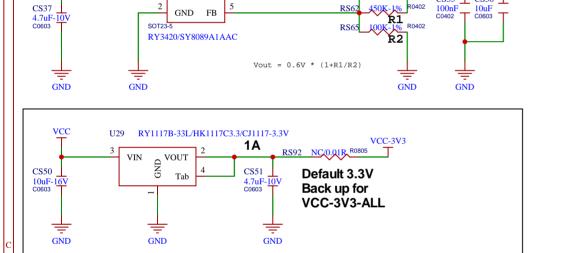


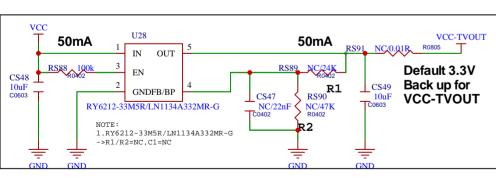
RS72 0.01R R0603

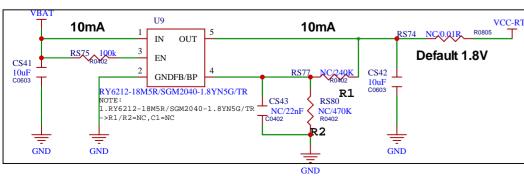
RS106 0.01R R0603

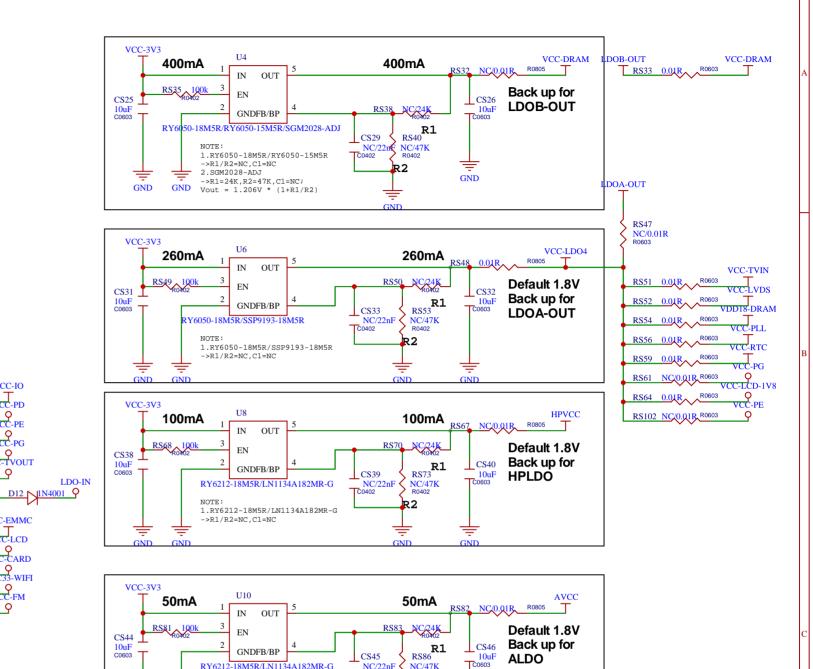
RS84 0.01R R0603

RS87 0.01R R0603









RY6212-18M5R/LN1134A182MR-G

1.RY6212-18M5R/LN1134A182MR-G ->R1/R2=NC,C1=NC

NC/22nF <

NC/47K R0402

