NAME

Md_py.py- Python code for generating synthesizable Verilog HDL for a multistage pipeline register.

DESCRIPTION

Python md_py.py [OPTIONS][PARAMETERS]

md_py is a python code which generates a Verilog code for a multistage shift register. The generated Verilog code is synthesizable. User provides required width, stages and reset value for the register. Width is the operand width and should be from 1 to 64 while stages is the number of pipeline stages and the decimal value should be from 2 to 128.

OPTIONS

--help or -h: Prints the command line options.

--param or -p: input parameter file name

--width or -w: Enter the operand width (decimal value from 1 to 64)

--stages or -s: Enter the number of pipeline stages (decimal value from 2 to 128)

--reset or -r: Enter the reset value of the register in decimal or hex

--outfile or -o: Enter the desired verilog file name

Example terminal commands:

```
python md_py.py  --param param.txt
python md_py.py  -p param.txt

python md_py.py --width 5 --stages 6 --reset 2 --outfile ver.v
python md_py.py –w 5 –r 8 –s 6 –o chkreg.v

python md_py.py --help
 pydoc md_py
```

Example parameter text file:

```
width = 16;

stages = 10;
```

outfile = chkreg.v;

reset = 8;

BUGS

If you find any bug please send an email to md6625@rit.edu.

AUTHOR

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