md_perl

NAME

md_perl - Perl code for generating synthesizable Verilog HDL for a multistage pipeline register.

SYNOPSIS

Perl md_perl.pl [OPTIONS][PARAMETERS]…

DESCRIPTION

Md_perl is a perl code which generates a Verilog code for a multistage shift register. The generated Verilog code is synthesizable. User provides required width, stages and reset value for the register. Width is the operand width and should be from 1 to 64 while stages is the number of pipeline stages and the decimal value should be from 2 to 128.

OPTIONS

-help: Prints the command line options.
-param: input parameter file name
-width: Enter the operand width (decimal value from 1 - 64)
-stages: Enter the number of pipeline stages (decimal value from 2 - 128)
-reset: Enter the 'reset'value of the register in decimal or hex
-outfile: Enter the desired verilog file name

Example terminal commands:

- perl md_perl.pl –param param.txt
- perl md_perl.pl –width 5 –stages 6 –reset 2 –outfile ver.v
- perl md_perl.pl –help

Example parameter file:
Width=7;
Stages=6;
Reset= 0x05;
Outfile= chkreg.v;

BUGS

If you find any bug please send an email to md6625@rit.edu.

AUTHOR

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