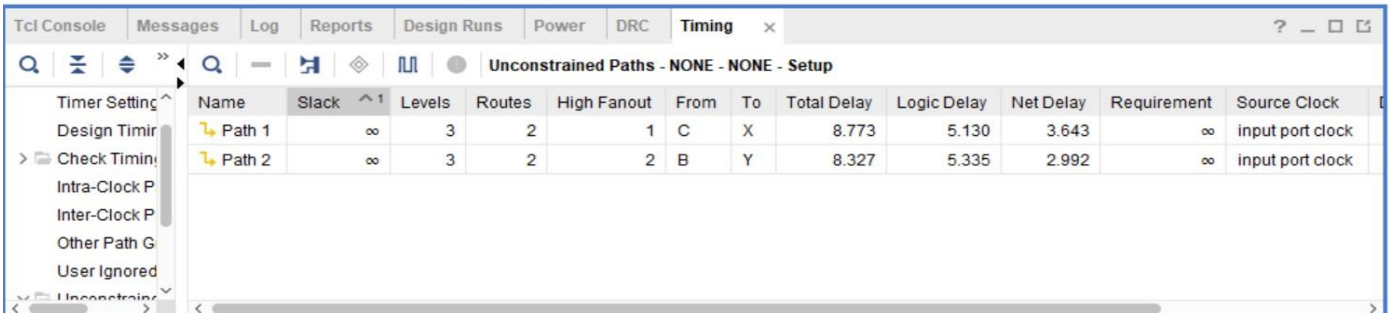
Lab Report 3

A. Truth Table

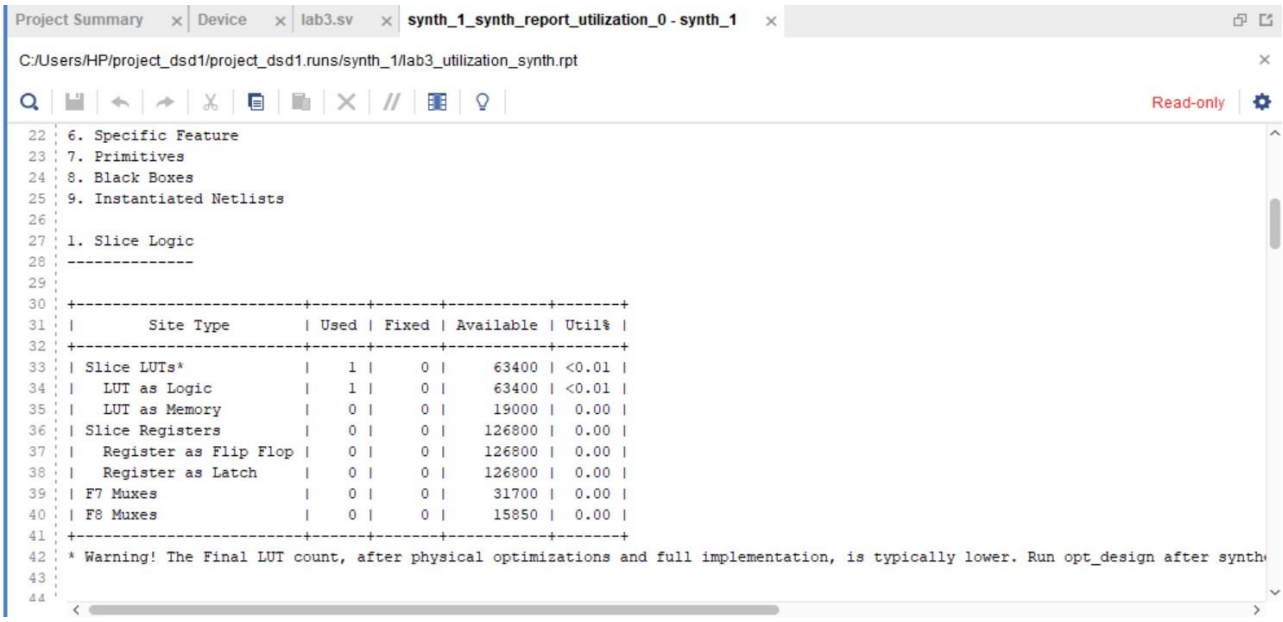
A	B	C	~C	A+B	~(A.B)	(A+B)XOR(~(A.B))=H		X= (A+B)XOR(~C)	Y= (A+B).H
0	0	0	1	0	1	1		1	0
0	0	1	0	0	1	1		0	0
0	1	0	1	1	1	0		0	0
0	1	1	0	1	1	0		1	0
1	0	0	1	1	1	0		0	0
1	0	1	0	1	1	0		1	0
1	1	0	1	1	0	1		0	1
1	1	1	0	1	0	1		1	1

B. Combinational delay



In this we can see that maximum combinational delay shows up in path from c to x which is 8.773 as observed during circuit synthesis.

C. Resource Utilization


Project Summary
Device
lab3.sv
synth_1_synth_report_utilization_0 - synth_1
C:/Users/HP/project_dsd1/project_dsd1.runs/synth_1/lab3_utilization_synth.rpt
Read-only
6. Specific Feature
7. Primitives
8. Black Boxes
9. Instantiated Netlists
1. Slice Logic
+-------------------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
Slice LUTs*	1	0	63400	<0.01
LUT as Logic	1	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00
+-------------------------+------+-------+-----------+-------+
* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synth