

Lab Report 3

A. Truth Table

A	B	C	$\sim C$	A+B	$\sim(A.B)$	$(A+B)XOR(\sim(A.B))=H$	X= $(A+B)XOR(\sim C)$	Y= $(A+B).H$
0	0	0	1	0	1	1	1	0
0	0	1	0	0	1	1	0	0
0	1	0	1	1	1	0	0	0
0	1	1	0	1	1	0	1	0
1	0	0	1	1	1	0	0	0
1	0	1	0	1	1	0	1	0
1	1	0	1	1	0	1	0	1
1	1	1	0	1	0	1	1	1

B. Combinational delay

Tcl ConsoleMessagesLogReportsDesign RunsPowerDRCTiming x? _ □

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Unconstrained Paths - NONE - NONE - Setup

Timer Setting ^

Design Timer

> Check Timing

Intra-Clock P

Inter-Clock P

Other Path G

User Ignored

Unconstrained

Name	Slack ^ 1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
🔗 Path 1	∞	3	2	1	C	X	8.773	5.130	3.643	∞	input port clock
🔗 Path 2	∞	3	2	2	B	Y	8.327	5.335	2.992	∞	input port clock

In this we can see that maximum combinational delay shows up in path from c to x which is 8.773 as observed during circuit synthesis.

C. Resource Utilization

Project Summary x Device x lab3.sv x synth_1_synth_report_utilization_0 - synth_1 x

C:/Users/HP/project_dsd1/project_dsd1.runs/synth_1/lab3_utilization_synth.rpt

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Read-only

22 6. Specific Feature

23 7. Primitives

24 8. Black Boxes

25 9. Instantiated Netlists

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27 1. Slice Logic

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31 | Site Type | Used | Fixed | Available | Util% |

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33 | Slice LUTs* | 1 | 0 | 63400 | <0.01 |

34 | LUT as Logic | 1 | 0 | 63400 | <0.01 |

35 | LUT as Memory | 0 | 0 | 19000 | 0.00 |

36 | Slice Registers | 0 | 0 | 126800 | 0.00 |

37 | Register as Flip Flop | 0 | 0 | 126800 | 0.00 |

38 | Register as Latch | 0 | 0 | 126800 | 0.00 |

39 | F7 Muxes | 0 | 0 | 31700 | 0.00 |

40 | F8 Muxes | 0 | 0 | 15850 | 0.00 |

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42 * Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synth

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