MUHAMMAD HUSNAIN MUBARIK

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RESEARCH INTERESTS

Computer Architecture, Hardware for Machine Learning, Hardware for Graphics (Conventional/Neural), Hardware Accelerators, Heterogeneous Parallel Systems, Printed Computer Systems, Emerging Technologies and Applications.

EDUCATION

University of Illinois at Urbana Champaign (UIUC), USA. *Jan 2019 - Present*
PhD - Electrical and Computer Engineering (ECE)
Advisor: Prof. Rakesh Kumar

National University of Sciences and Technology (NUST), Pakistan. *Sep 2013 - July 2017*
Bachelors of Science in Electrical Engineering.
CGPA: 3.95/4.00, **summa cum laude**.

RESEARCH AND WORK EXPERIENCE

Intel, USA.

- **Graphics Research Organization (GRO)** *May 2023 - **Present***
  Graduate Research Intern (Full-time)
  Managers: Tobias Zirr, Anton Sochenov, Anton Kaplanyan.
- **Next-Gen Architecture (NGA)** *August 2022 - May 2023*
  Graduate Research Intern (Part-time)
  Manager: Maxim Kazakov.
- **Graphics Research Organization (GRO)** *June 2022 - August 2022*
  Graduate Research Intern (Full-time)
  Managers: Rama Harihara, Anton Kaplanyan.
- **Cloud System Research Lab (CSR)** *Dec 2021 - May 2022*
  Graduate Research Intern (Part-time)
  Managers: Nilesh Jain, Ravishankar Iyer.
- **Heterogeneous Platforms Lab (HPL)** *May 2021 - Aug 2021*
  Graduate Research Intern (Full-time)
  Manager: Tanay Karnik.

Coordinated Science Laboratory (CSL), UIUC, USA *Jan 2019 - **Present***
Research Assistant
Advisor: Prof. Rakesh Kumar

- ML accelerators for accelerating gaming and vision applications (Ongoing)
- Hardware Acceleration of Neural Graphics (**ISCA-50th, 2023**)
- Understanding Interactions Between Chip Architecture and Uncertainties in Semiconductor Supply and Demand (Under Submission - Preprint available on arXiv.)

- Exploiting Short Application Lifetimes for Low Cost Hardware Encryption in Flexible Electronics (**DATE 2023**)
- Rethinking Programmable Earable Processors (**ISCA-49th, 2022**)
- Model-specific Design of Deeply-Embedded Tiny Neural Network Accelerators (Ongoing).
  - Current edge NN accelerator hardware designs tend to be model-agnostic and are, therefore, over designed and expensive for a specific model.
  - For a suite of tiny neural networks, we show that customizing hardware to model structure can provide 101× benefits in terms of inference throughput and 69× benefits in terms of energy efficiency over Eyeriss. Additional 4.3× and 2.4× benefits are achievable in terms of area and energy efficiency respectively if model data is also known during design time.
- Printed Machine Learning Classifiers (**MICRO-53rd, 2020**)
  - A large number of application domains have requirements on cost, conformity, and non-toxicity that silicon-based computing systems cannot meet, but that may be met by printed electronics.
  - We perform the first exploration of different classification algorithms in terms of accuracy and potential cost for two printed technologies (EGT and CNT-TFT).
  - We develop and evaluate bespoke printed classifier architectures. We show that EGT-bespoke Decision Tree implementations have 4× lower delay, 75× lower power, and 48× lower area (on average) than their conventional general-purpose counterparts. Corresponding benefits for bespoke SVM implementations are 1.4×, 12.7×, and 12.8× respectively.
  - We develop and evaluate lookup-based printed classifier. Our results show that lookup based EGT Decision Trees improve the area of bespoke counterparts by 1.93× and power by 1.65×, with 50% delay overhead. Lookup-based SVMs provide 40% reduction in delay with 8% and 1% improvement in area and power respectively.
  - We also develop and evaluate analog printed classifiers. EGT analog Decision Trees outperform their digital bespoke counterparts by 437× and 27× for area and power respectively and are 1.63× slower. Corresponding area and power benefits for analog SVM architectures are 490× and 1212× respectively.
- Printed Microprocessors (**ISCA-47th, 2020.)**
  - We present the first exploration of the design space for microprocessors implemented in printing technologies and designed standard cell libraries for printed technologies.
  - We perform a design space exploration of printed microprocessor architectures over multiple parameters - datawidths, pipeline depth, etc. We show that the best cores outperform pre-existing cores by at least one order of magnitude in terms of power and area.
  - In addition to various printed specific optimizations, we present Program-specific ISA which improves power, and area by up to 4.18× and 1.93× respectively. We also show that Cross point-based instruction ROM outperforms a RAM-based design by 5.77×, 16.8×, and 2.42× respectively in terms of power, area, and delay.

National Electronics Complex of Pakistan (NECOP), Pakistan *Jul 2017 - Oct 2018*
RF and Microwave Design Engineer - Assistant Manager

- Designed and Developed IMF Receiver, Antennas for Phased Array Radar, Branched Line Hybrid Coupler, Power Dividers and Band Pass Filters for X-Band Applications.

Research Internee at MERL - NUST, Pakistan *June 2016- July2017*

- Designed and Developed a "Low Cost Short Range Frequency Modulated Continuous Wave Radar (FMCW) Radar". (**Second Position in Rector's Gold Medal Competition - NUST.)**

PUBLICATIONS

1 **M. Mubarik**, R. Kanungo, T. Zirr, R.Kumar "Hardware Acceleration of Neural Graphics" **ISCA-50th, 2023.**

2 N. Bleier, **M. Mubarik**, S. Balaji, F. Rodriguez, A. Sou, S. White and R. Kumar, "Exploiting Short Application Lifetimes for Low Cost Hardware Encryption in Flexible Electronics," **DATE 2023.**

3 N. Bleier, **M. Mubarik**, S. Chakraborty, S. Kishore, R. Kumar, "Rethinking Programmable Earable Processors," **ISCA-49th, 2022.**

4 **M. Mubarik**, D. Weller, N. Bleier, M. Tomei, J. Aghassi-Hagmann, M. Tahoori, R. Kumar, "Printed Machine Learning Classifiers," **MICRO-53rd 2020, IEEE Micro Top Picks - Honorable Mention 2021.**

5 N. Bleier*, **M. Mubarik***, F. Rasheed*, J. Aghassi-Hagmann, M. Tahoori, R. Kumar, "Printed Microprocessors," **ISCA-47th, 2020.** [* Co-First Authors, Listed in Alphabetical Order] **Selected for the retrospective of the years 1996 through 2020 on the 50th anniversary of ISCA.**

6 R. Kanungo, S. Siva, N. Bleier, **M. Mubarik**, L. Varshney, R. Kumar "Understanding Interactions Between Chip Architecture and Uncertainties in Semiconductor Supply and Demand" - Under Submission, preprint arXiv:2305.11059, 2023.

TALKS

- Presented "Hardware Acceleration of Neural Graphics" paper at ISCA-50th, 2023.
- Gave a talk on "Neural Graphics: An Architectures Perspective" at ECE498SJP: Accelerator Architectures class at UIUC [2023].
- Gave a talk titled "Hardware Acceleration Opportunities in Neural Radiance Fields" at Intel [2022].
- Presented "Printed Machine Learning Classifiers" paper at MICRO-53rd, 2020.
- Gave a talk on "Hardware for Deep Learning" at ECE511: Advanced Computer Architecture class at UIUC [2021].

ACADEMIC ACHIEVEMENTS AND AWARDS

- **ISCA-50th 25 year retrospective (1996-2020), 2023.**
  - Selected for the retrospective of the years 1996 through 2020 on the 50th anniversary of ISCA for our paper "Printed Microprocessors" (ISCA-47th, 2020).
- **Machine Learning and Systems Rising Star, 2023.**
  - Hardvard, Google, Nvidia and ML Commons.
- **IEEE Micro Top Picks - Honorable Mention, 2021.**
  - Our paper "Printed Machine Learning Classifiers" (MICRO-53rd, 2020) ranks among the Top 24 papers published in computer architecture venues in 2020.
- **Prime Minister's Silver Medal**, NUST-CEME, 2018.
  - 2nd highest CGPA (3.95/4.00) in the Electrical Engineering Department at NUST-CEME.

- Travel award for EECamp at KAIST, South Korea, 2018.
- NUST GPA scholarships 2013-2017.
- High Achievers Award, NUST-CEME, 2015.
- Golden Star Award, NUST-CEME, 2015.
- NECOP Fellowship 2014-2017.

TECHNICAL SKILLS

- Programming languages: C++, Python, Verilog, SystemVerilog, CUDA, GLSL, Scala, SystemC, Tcl, Bash, Makefile
- Software: PyTorch, TensorFlow, TensorRT, Onnx-Runtime, Caffee, Keras, Synopsys-VCS, MATLAB, LATEX, Vim
- Frameworks: Vulkan, OpenGL, CUDA, CHISEL, gem5, Nsight (Compute/Systems/Graphics).

COURSES

- ECE498SJP: Accelerator Architectures (Sanjay Patel) - Spring 2023.
- CS534: Advanced Topics in Computer Architecture (Sarita Adve) - Spring 2022.
- ECE598JH: Advanced Memory and Storage Systems (Jian Huang) - Fall 2021.
- CS598DHK: 3D Vision (Derek Hoiem) - Fall 2021.
- CS498ME Architecture for Mobile and Edge Computing (Saugata Ghose) - Spring 2021.
- CS598LCE Languages and Compilers for Edge Computing (Vikram S. Adve) - Spring 2021.
- ECE598NSG: Deep Learning in Hardware (Naresh Shanbhag) - Fall 2020.
- ECE524/CS563: Advanced Computer Security (Adam Bates) - Spring 2020.
- CS598SVA: App-Cust Heterogeneous Systems (Sarita Adve) - Spring 2020.
- CS598JT: Energy Efficient Computer Architecture (Josep Torrellas) - Fall 2019.
- ECE511: Advanced Computer Architecture (Rakesh Kumar) - Spring 2019.
- CS533: Parallel Computer Architecture (Josep Torrellas) - Spring 2019.

MEMBERSHIPS

- Member, Computer Architecture Student Association (CASA) Jan 2021 - Present
- Reviewed papers for ISCA, MICRO, HPCA and ASPLOS.