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GRADUATION PROJECT PROGRAM

Meeting 5G Reliability Requirements in Cell Outage Compensation (COC) in Self-Organizing Networks (SONs) using Hardware Acceleration

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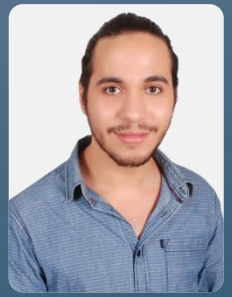
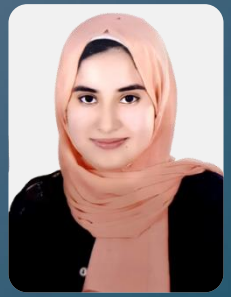
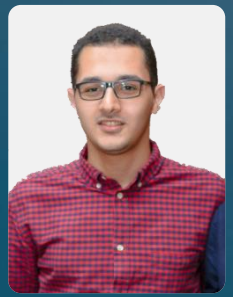
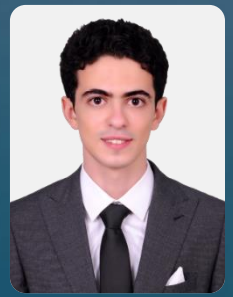
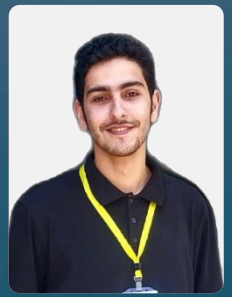
July 2023

MEET OUR TEAM

Mentor: Ensaf Atef
Senior Embedded SW Engineer,
Valeo Egypt

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01 PROBLEM DEFINITON

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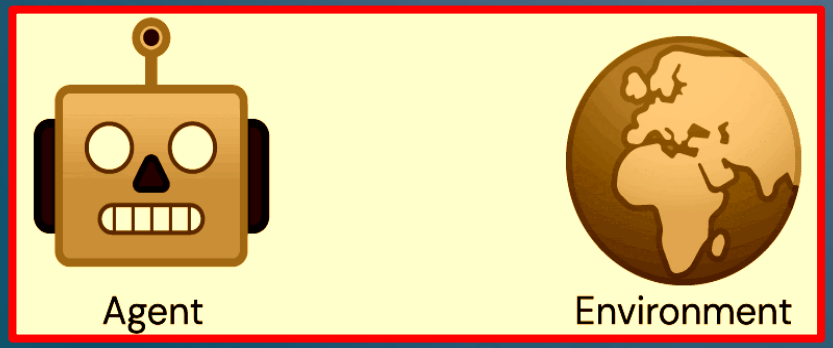
AI Algorithms DO NOT Meet Real-Time Requirements

NOT Fast Enough in Critical Decision Making



Inefficient AI-Algorithm Processing Time
(SLOW)

Efficient AI-Algorithm Processing Time
(FAST)

Research Gap

"Although RL is a great promise for general intelligence, it also has the challenge that it requires time to learn and in online form. This is a great challenge in communication network and other mission critical systems where there is no room for failure. "

S. S. Mwanje and C. Mannweiler, "TOWARDS COGNITIVE AUTONOMOUS NETWORKS IN 5G," 2018 ITU Kaleidoscope: Machine Learning for a 5G Future (ITU K), Santa Fe, Argentina, 2018, pp. 1-8, doi: 10.23919/ITU-WT.2018.8597732.

"Challenge 4: Meeting 5G latency requirements in Self-healing 5G mobile cellular networks are expected to have end-to end data latency of 1 ms. This means that any Self-healing solution deployed in the network must be able to detect, diagnose and compensate any outage in far less time than state-of-the-art solutions."

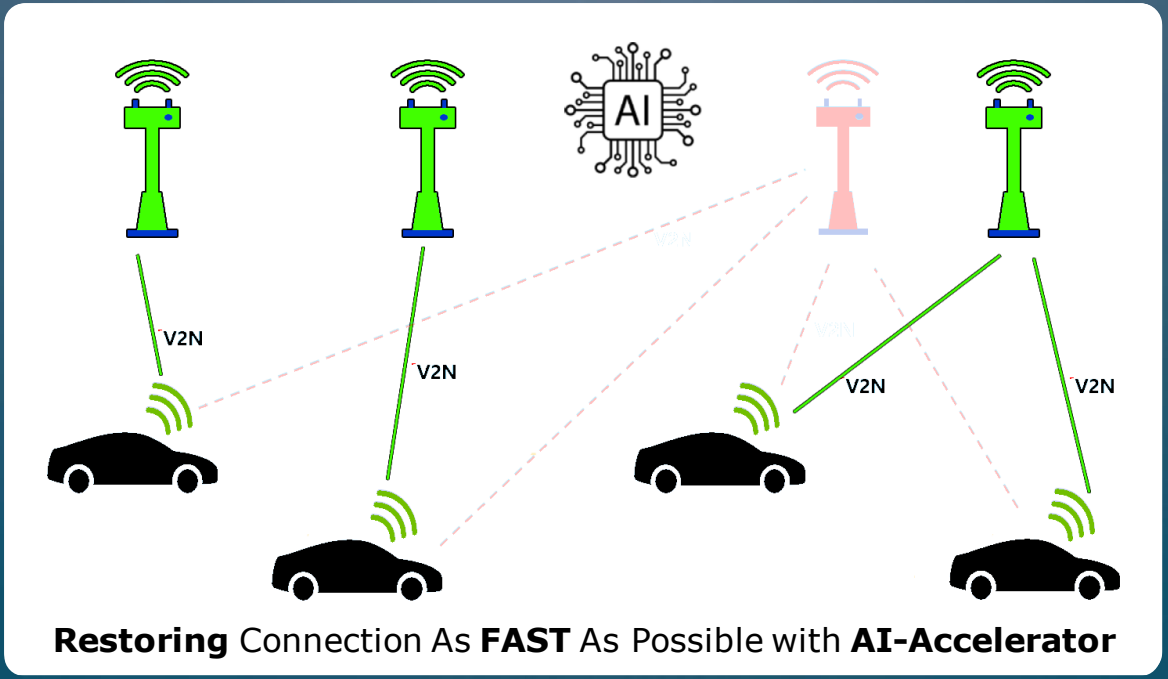
A. Asghar, H. Farooq and A. Imran, "Self-Healing in Emerging Cellular Networks: Review, Challenges, and Research Directions," in IEEE Communications Surveys & Tutorials, vol. 20, no. 3, pp. 1682-1709, thirdquarter 2018, doi:

"Real-time applications may have different time restrictions. (…) Traditional mechanisms and methods are not always able to overcome the barriers imposed by the more challenging time constraints."

L. M. D. Da Silva, M. F. Torquato and M. A. C. Fernandes, "Parallel Implementation of Reinforcement Learning Q-Learning Technique for FPGA," in IEEE Access, vol. 7, pp. 2782-2798, 2019, doi: 10.1109/ACCESS.2018.2885950.

AUTOMITIVE INDUTRY USE CASE: Vehicle-to-Network Communications (C-V2N)

AI Algorithms DO NOT Meet Real-Time Requirements in 5G Self-Healing Capabilities



Restoring Connection As **FAST** As Possible with **AI-Accelerator**

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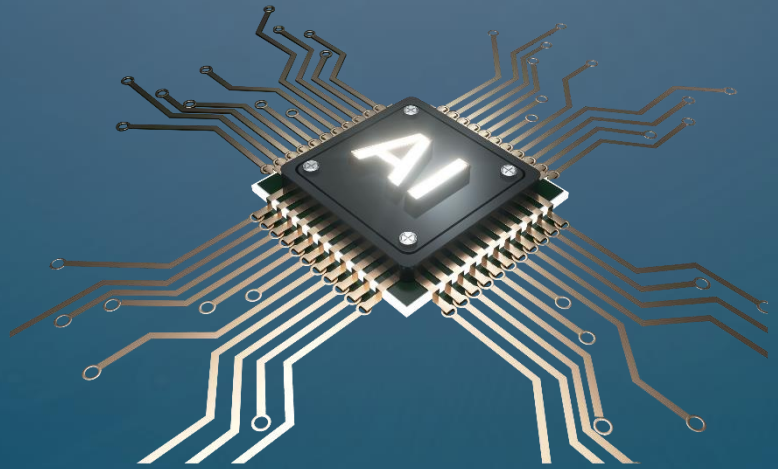
02 PROPOSED SOLUTION

Our AI-Algorithm used in 5G V2N Service Restoration Should be FASTER

Design an Intelligent AI-Accelerator to Enable 5G V2N Self-Healing Full Features



AI-Accelerator mean that AI algorithm built in specialized hardware (specific chip)

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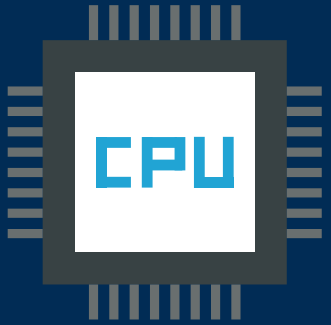
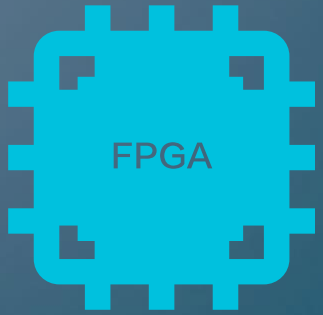
An AI-ACCELERATOR TO MEET AUTOMOTIVE CONEECTION REQUIRMENTS

FROM



CPU-Based AI

TO



FPGA-Based AI

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FPGA-Based AI

Specialized

Fixed-Function

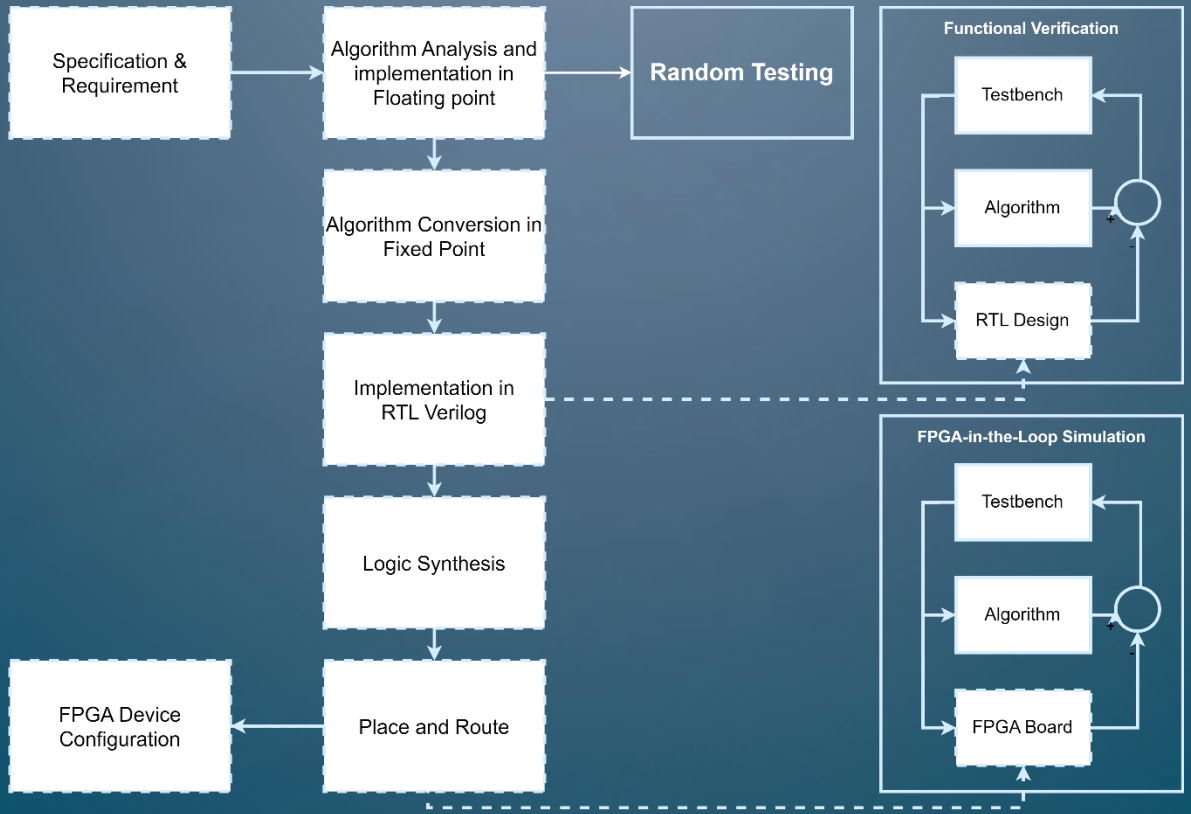
Real-Time

High Computational Power

Energy Efficiency

100-1,000x More Efficient Than CPU

03 WORKFLOW in TWO MINUTEs ☺



The figure shows the workflow of out project

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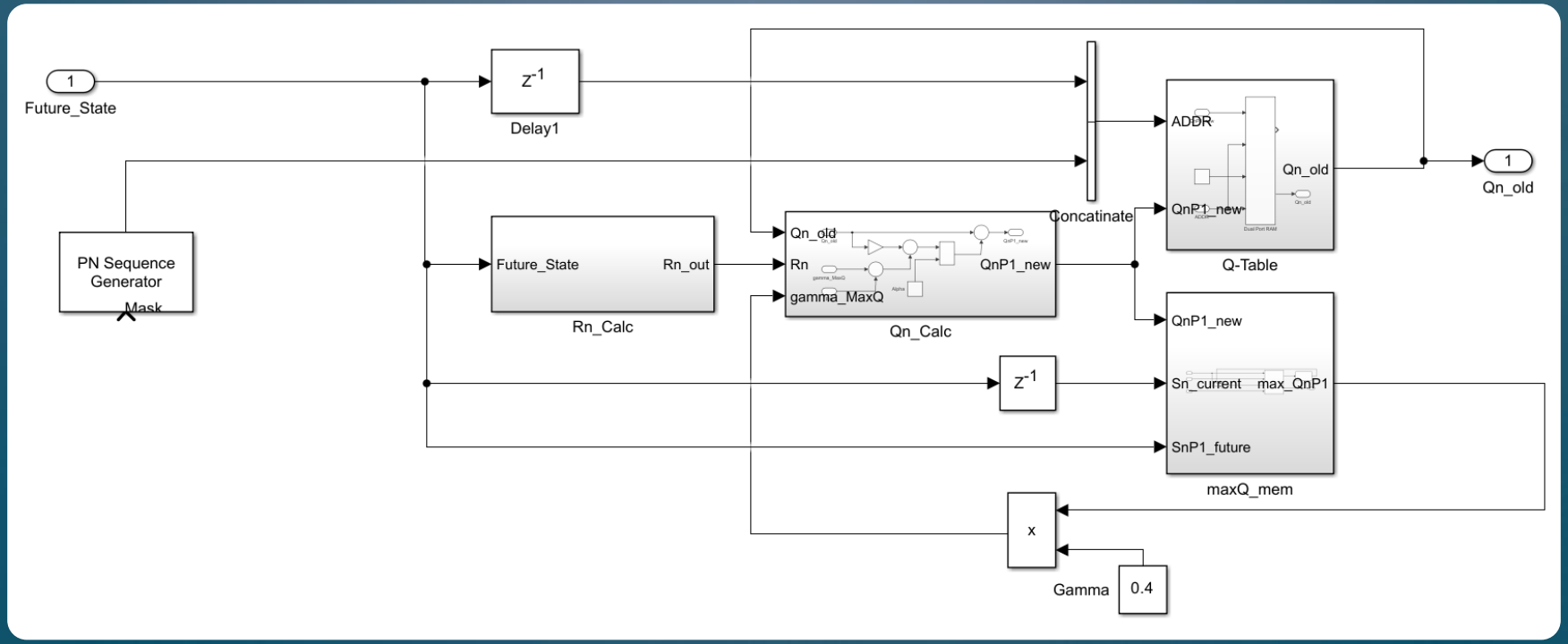
The figure shows the resources of specifications and requirements for the algorithm



The figure shows the Model-based design of model using SIMULINK

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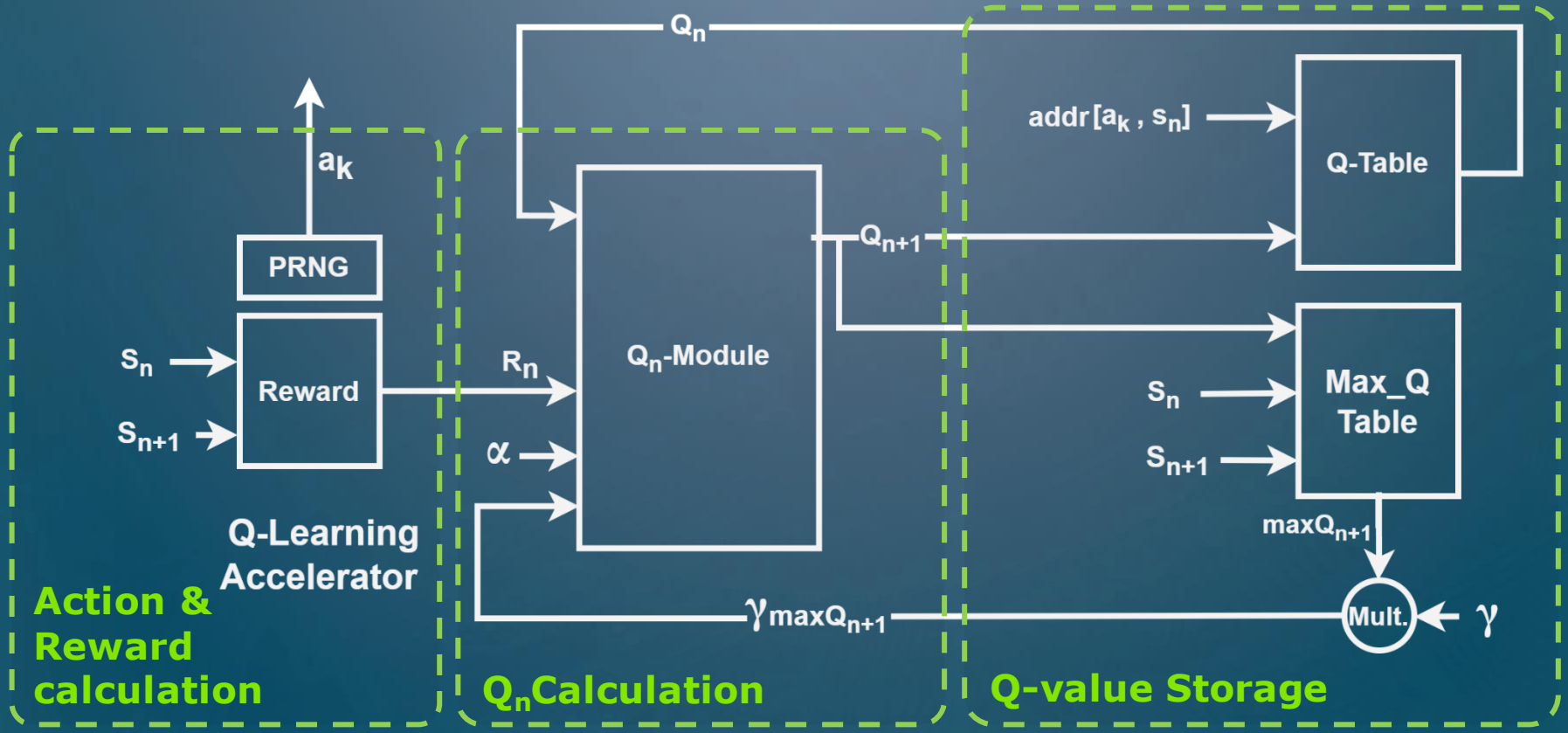

The figure shows the Serial implementation of the Q-learning technique on an FPGA.

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HIGH-LEVEL SW MODEL RESULTS

Type	Tabular RL
Algorithm	Q-Learning
Programming Language	MATLAB
Style of Programming	OOP
Actions	9
States	20
Epsilon-Greedy	Yes (0.5)

Learning Rate	0.7
Discount Factor	0.1
Features	Vanilla
	Visualization
	Parametric Model
	GUI Application

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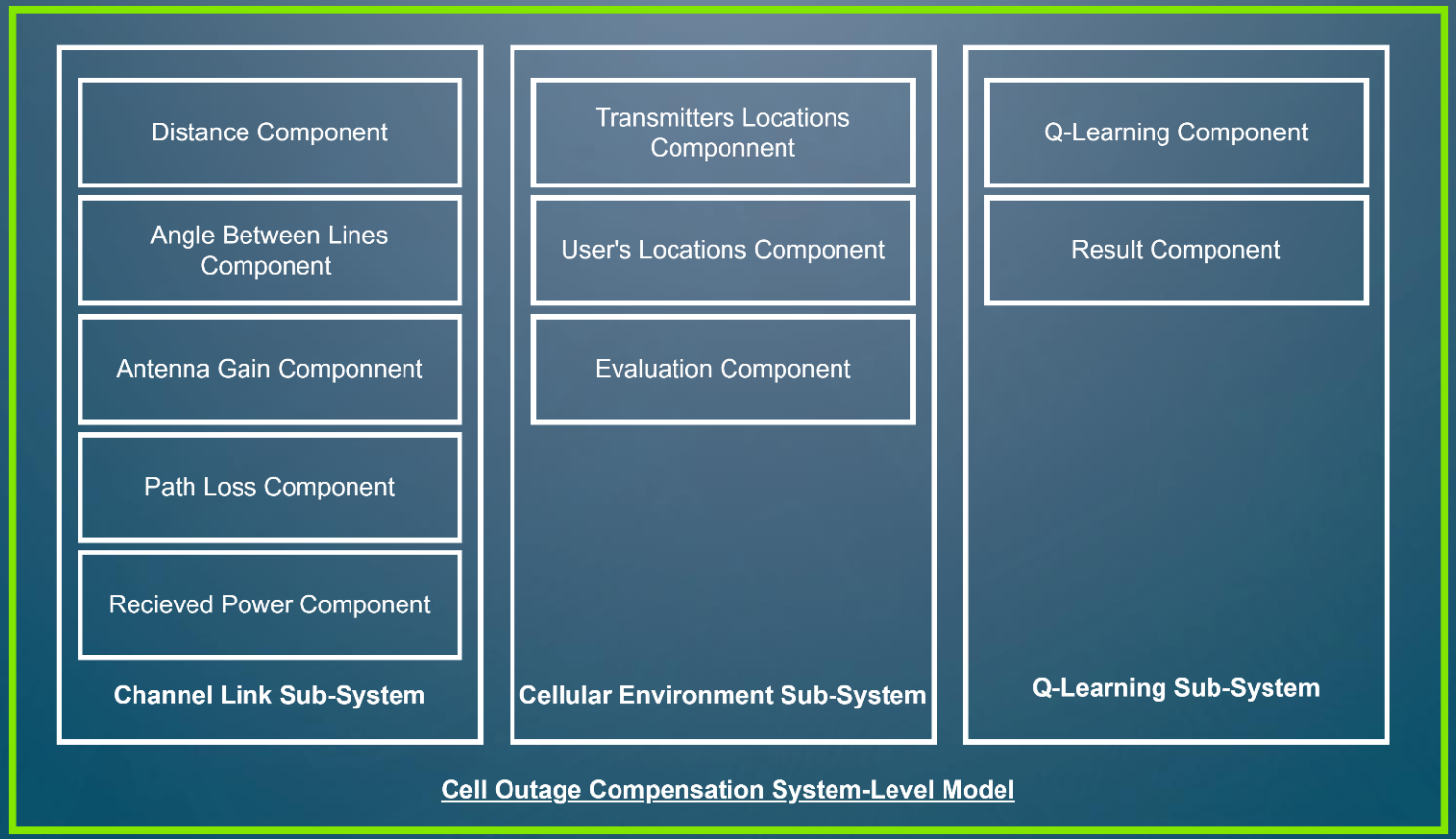

The figure shows the High-level model as layered architecture

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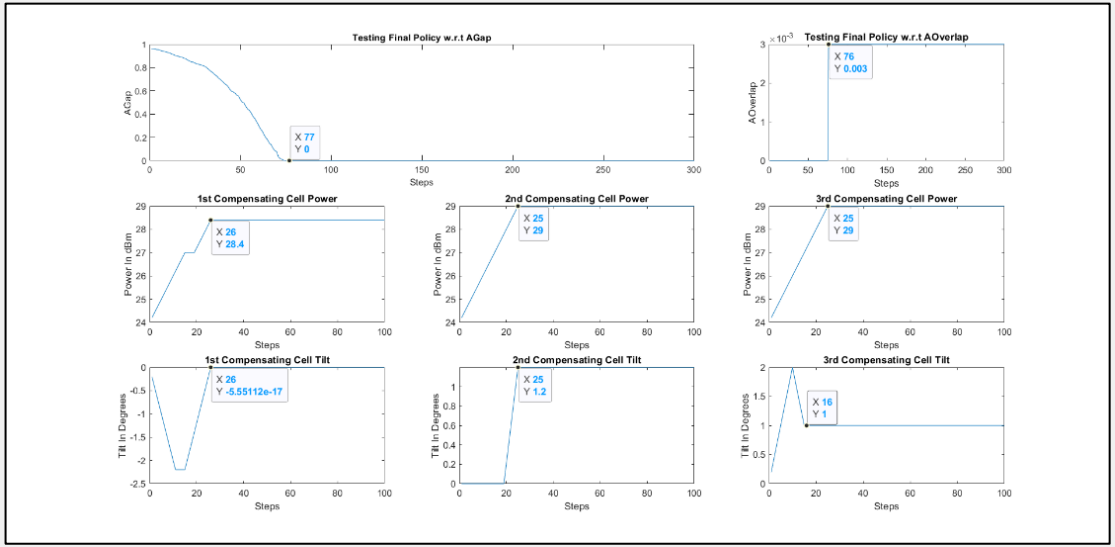
Cell Outage Compensation Model

System Model Parameters

Initial Transmitted Power	24
Intial Tilit Angle	0
Operating Frequency	4
Inter-Site Distance	2000
Number of Users in System	1000
Environment Type	Urban / Sub-Urban / Rular / Open

Run Simulation



The figure shows the High-level model for the algorithm using MATLAB – GUI for high-level Model

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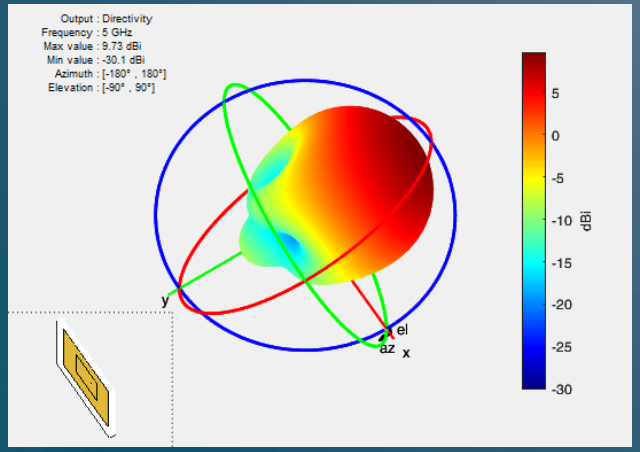

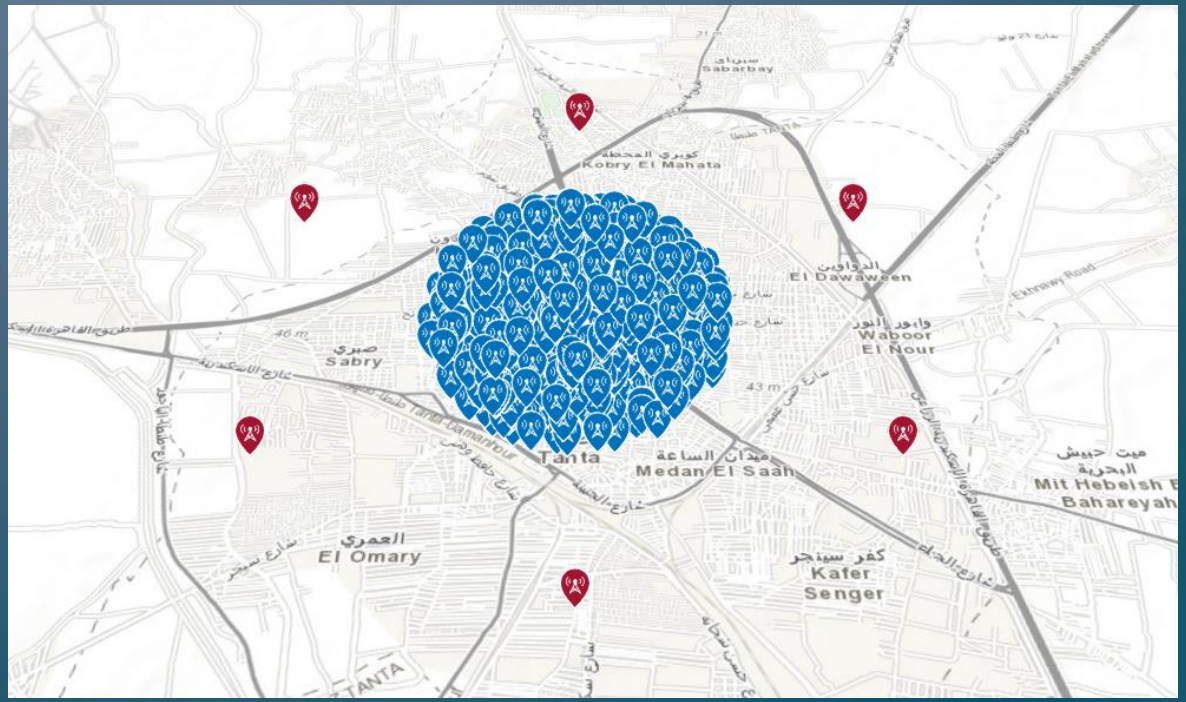

The figure shows the High-level model for the algorithm using MATLAB – Antenna Pattern, Cellular Mobile Network

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HARDWARE IMPLEMETATION RESULTS

Type	Tabular RL
Algorithm	Q-Learning
Platform	Altera Cyclone®
Reference Platform	3C16 FPGA Device
States	20
Reward Width	15 bit

Resources	**LUTs**	410 Logic Element
	FFs	124 Register
	IM	1792 Memory Bit
	DPS	Null
TP[a] [MSps]		50
TP[a] per Power [MSps/mW]		0.24
TP[a] per LUT [MSps/LUT]		0.122

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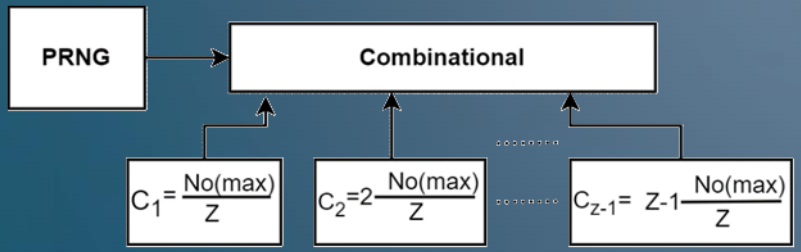
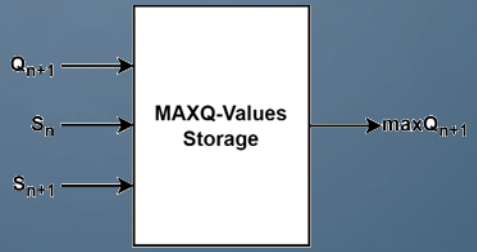
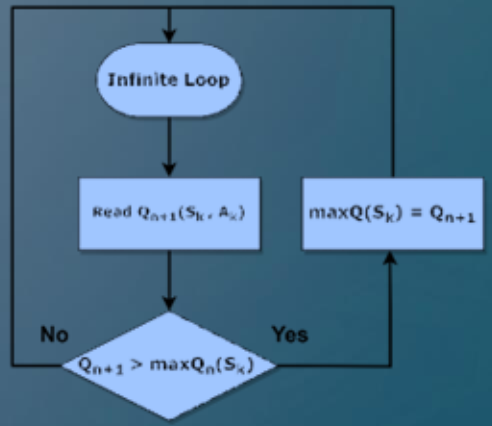
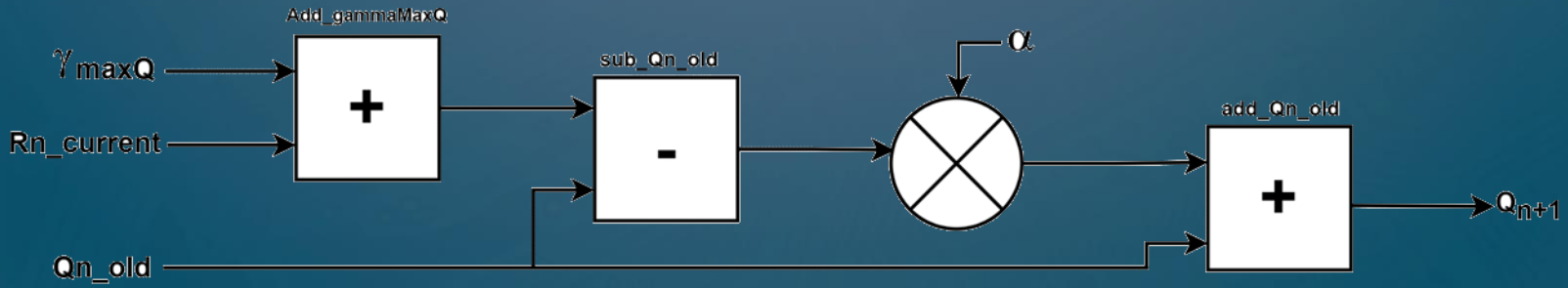






$$Qn+1(s, a) = Qn(s, a) + \alpha[r(A_{gap}, a) + \gamma \max(Q(s', a')) - Qn(s, a)]$$



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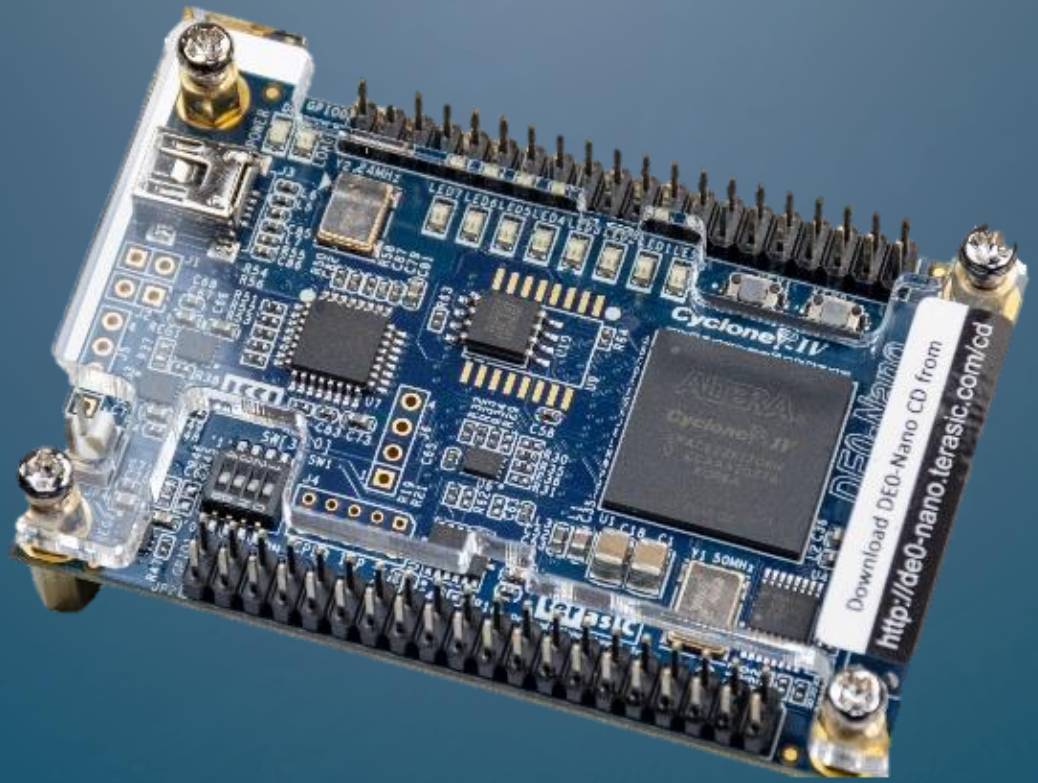

The figure shows the used FPGA.

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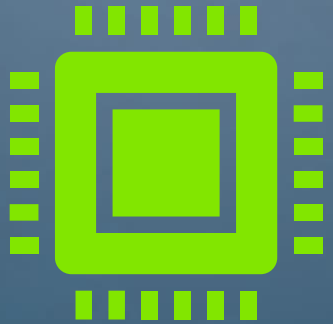
Final Product



Semi-Conductor Intellectual Property Core (IP core)

From **VALEO** to Connected Mobility Community

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Q&A