ELECTRICAL & COMPUTER ENGINEERING

Portland State UNIVERSITY

Design Review

Tilt-Timer Cube

ECE 411 - *Industry Design Processes*

Fall 2025

Prof. *Andrew Greenberg*

Authors: *Yaaqoub Rabiah, Hussein Ashkanani, Khaled A. Alkandari, & Artyom Kaydalin. (Group 13)*

Contact yrabiah@pdx.edu, hashk2@pdx.edu, khaled36@pdx.edu, & artyom@pdx.edu.

Date: November 20, 2025

Team 14 – Design Review Notes

Team Members Present: Daniel, Eyad, Manaf, Saleh, Khaled, Yaqoub

Date: November 18, 2025

1. High-Level Project Review

- Confirm power-source behavior under all operating conditions.

- Ensure bus integrity on I2C communication lines (SDA, SCL).

- Review physical constraints: board shape, battery placement, OLED fit.

2. Schematic Review – Issues & To-Dos

a) Power System

- Use 4.7 kΩ pull-ups on SDA and SCL. Without them, the bus floats low, and all I2C devices read zero.

- The fixed 3.3 V buck-boost regulator must be validated for load current.

- If the battery dies, the boost converter output drops.

b) Battery & Power Routing

- Battery symbol placement in CAD must be moved, current position interferes with the PCB footprint.

- Check that traces feeding the power stage are sized correctly for the expected current (pre-defined trace width 2.54 mm).

- Run an updated ERC report to verify unconnected power pins.

c) Grounding & Connectivity

- U2 has no ground connection.

- Verify all return-paths are consistent and not relying on long thin traces.

d) Components & Connections

-OLED footprint must be measured and confirmed to physically fit on the PCB.

-Through-hole components should follow the minimum recommended dimensions:

-18 mil drill / 10 mil annular on through-holes.

- Ensure all connectors are labeled clearly.

3. PCB Layout Review – Issues & To-Dos

a) Mechanical & Ergonomics

-PCB needs rounded edges.

- Verify battery holder placement and ensure mechanical clearance.

b) Routing & Spacing

-Maintain the pre-defined 2.54 mm trace width where high current flows.

-Check spacing around the OLED cutout area.

-Run ERC.

c) Signal Integrity

-Route SDA/SCL is short and direct. Keep away from high-current power traces.

- Ensure enough ground vias for the return path near connectors.

Team 10 – Design Review Notes

Team Members Present: Allen, Dylan, Hussain, Hussein Ashkanani , Khaled, Yaqoub

Date: November 19, 2025

1. Schematic Review – Issues & To-Dos

a) Microcontroller & Clock

- Add a series resistor if required.

- Add both load capacitors correctly sized.

b) Functionality

- The Tilt-Timer Cube has six faces, must label each orientation.

- Clarify timer shutdown behavior: Timer will stop based on interrupt logic.

Confirm behavior of buzzer: Buzzer continues until the cube is returned to the original upright position.

c) Power & Battery

- Battery holder must be cut/adjusted to fit within the enclosure.

- Check battery packaging and mounting.

2. PCB Layout / Issues & To-Dos

- Ensure proper footprint

- Verify that block-labeling is consistent for each cube face.

- Confirm programming interface location for accessibility.

Professor Andrew's Review Notes

Attendance: Hussein, Khaled, Yaqoub

Date: November 19, 2025

Issues & To-Dos

-BC-2001: Requires clearer schematic annotation.

-Pin header should be 2.54 mm pitch, verify footprint.

-Increase trace width for power lines.

- Add more vias for grounding and return-path consistency.