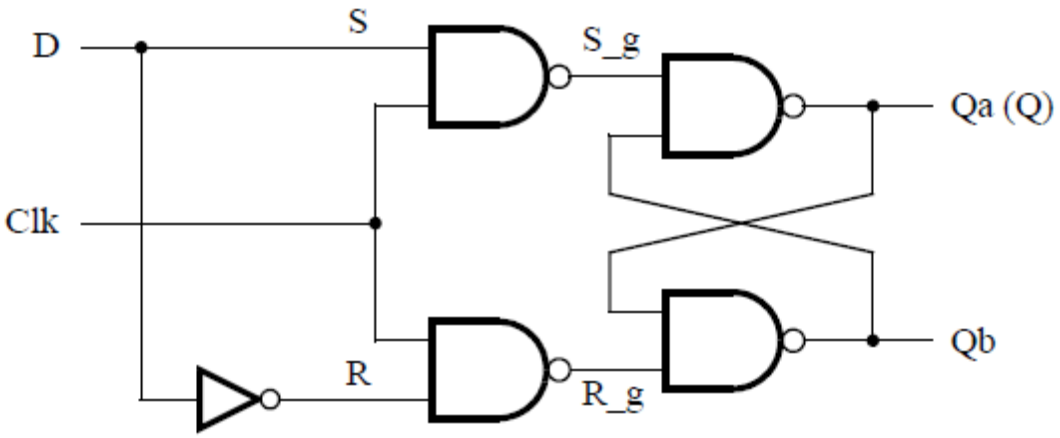
Solution: TP4

Part I:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY part1 IS
PORT ( Clk, R, S : IN STD_LOGIC;
Q          : OUT  STD_LOGIC);
END part1;

ARCHITECTURE Structural OF part1 IS
SIGNAL R_g, S_g, Qa, Qb : STD_LOGIC ;
BEGIN
R_g <= R AND Clk;
S_g <= S AND Clk;
Qa <= NOT (R_g OR Qb);
Qb <= NOT (S_g OR Qa);

Q <= Qa;
END Structural;
```

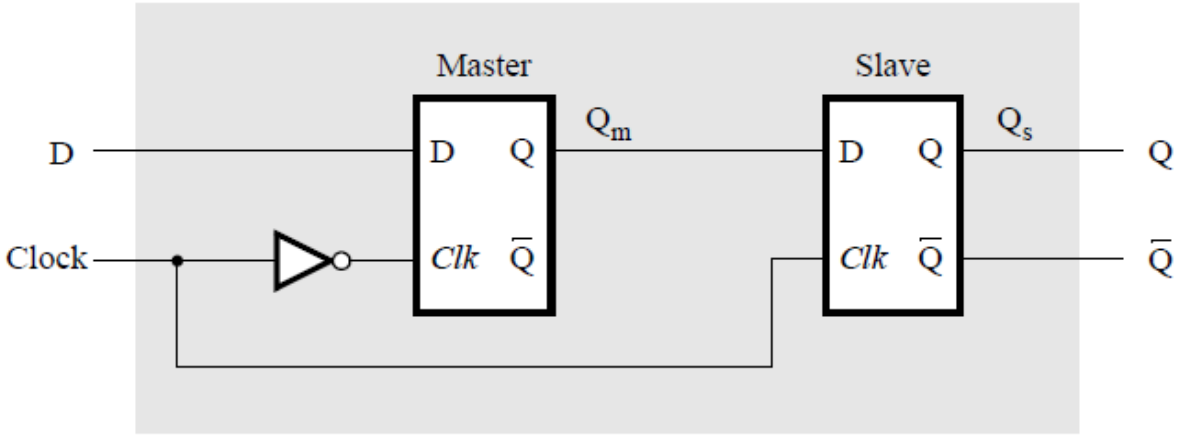
Part II:




```
LIBRARY ieee;
Use ieee.std_logic_1164.all;
ENTITY part2 is
  port( clk,Din: IN STD_LOGIC;
      Qout,Qnout: OUT STD_LOGIC);
    END part2;
ARCHITECTURE STRUC OF part2 is
  SIGNAL R,R_g,S_g,Qa,Qb : STD_LOGIC;
```

```
 BEGIN
   R<= NOT Din;
   R_g<= not (R AND clk);
   S_g<= not (Din AND clk);
   Qb<= not (R_g AND Qa);
   Qa<= not (S_g AND Qb);
   Qout<=Qa;
   Qnout<=Qb;
 end STRUC;
```

Part III:

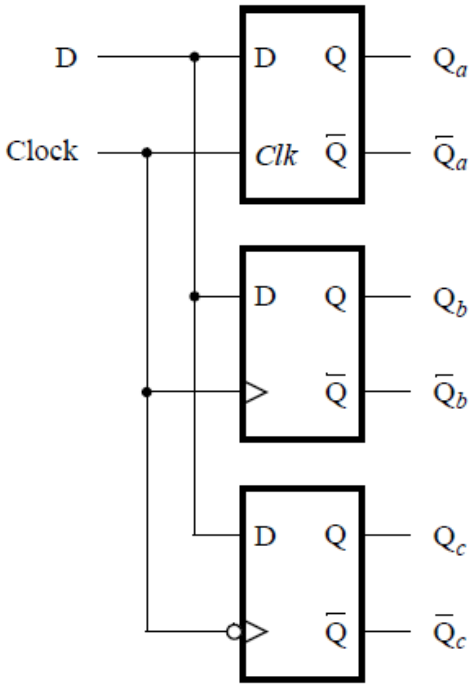


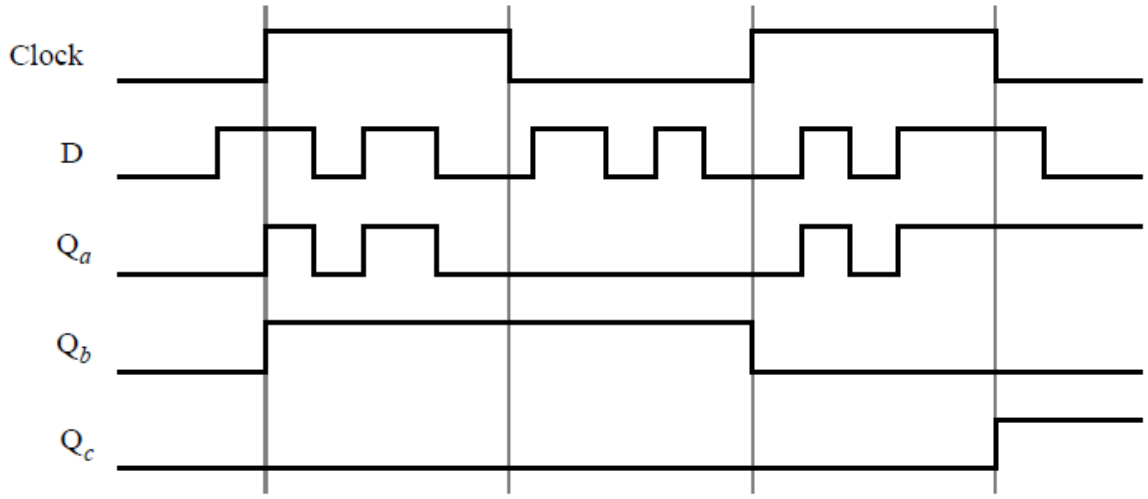

```
-- A gated D latch. desribed the hard way
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY basculed  IS
 PORT ( Clk, Din: IN STD_LOGIC;
       Qout : OUT STD_LOGIC);
  END basculed ;
ARCHITECTURE Structural OF basculed  IS
SIGNAL R,R_g, S_g, Qa, Qb : STD_LOGIC ;
--ATTRIBUTE keep : boolean;
--ATTRIBUTE keep of R_g, S_g, Qa, Qb : SIGNAL IS true;
BEGIN
R<=NOT Din;
R_g <= not(R NAND Clk);
S_g <= not (Din NAND Clk);
Qb <= NOT (R_g AND Qa);
Qa <= NOT (S_g AND Qb);
Qout <= Qa;
END Structural;
```

----------main----------

```
library ieee;
use ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;
entity lab3_3 is
port( D,Clock: in std_logic;
                                Q,QN : out std_logic);
end lab3_3;
architecture behaviore  of lab3_3 is
component basculed is
port (Clk,Din : in std_logic;
                                Qout : out std_logic);
end component;
signal Qm,C,QS: std_logic;

begin
C<=not(Clock);
G1:basculed port map (D,C,QM);
G2:basculed port map (Qm,Clock,QS);

Q<=Qs;
QN<=not Qs;

end behaviore;
```

Part IV






```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY part4 IS
PORT ( D, Clk : IN STD_LOGIC ; Qa,Qb,Qc : OUT STD_LOGIC) ;
 END part4 ;
ARCHITECTURE Behavior OF part4 IS
BEGIN
 PROCESS ( D, Clk )
 BEGIN

  IF (Clk'event and Clk='1') THEN Qb<=D;
   elsIF (Clk'event and Clk='0') THEN Qc<=D;
  END IF ;
  IF Clk = '1' THEN Qa <=D;
    END IF ;
  END PROCESS ;
   END Behavior ;
```