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LLC Converter Design Note

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1 Introduction

LLC topology has been used sparingly in high-end applications that required the very highest efficiency possible. However, with industry demanding increased efficiency in more mainstream products and organizations such as Energy Star and 80 Plus posting ever higher “recommendations” for efficiency at any load-level, LLC topology is proliferating throughout product categories and power levels. While this topology handles load variarations extremely well, it requires substantial upfront effort to configure a design to handle line variations – this must be fully considered in the resonant tank design, and a wider input range design will have some specific trade-offs. Use LLC in off-line SMPS with a pre-regulated bus (PFC) when efficiency and power density are high priorities. This design note aims to detail the operation of the LLC converter in its three different modes as well as provide guidance on how to properly design an LLC stage. A detailed example is provided with component selection and worst-case loss calculations for all semiconductor components.

2 LLC Converter Topoology

The LLC converter is part of the resonant converter family, which means regulation is not like conventional Pulse Width Modulation schemes. Running at 50% Duty cycle and fixed 180 degree phase shift, regulation is obtained through frequency modulation. All primary side MOSFETs turn on resonantly – Zero Voltage Switching – resulting in full recycling of the energy contained in the MOSFETs’ parasitic output capacitance. Furthermore, all secondary side switches turn off resonantly – Zero Current Switching – to minimize switching losses normally associated with hard switching. Resonant operation of all switching devices in the LLC converter results in minimized dynamic loss and thus increased overall efficiency; particularly at higher operating frequencies in the hundreds of kilo Hertz to Mega Hertz range.

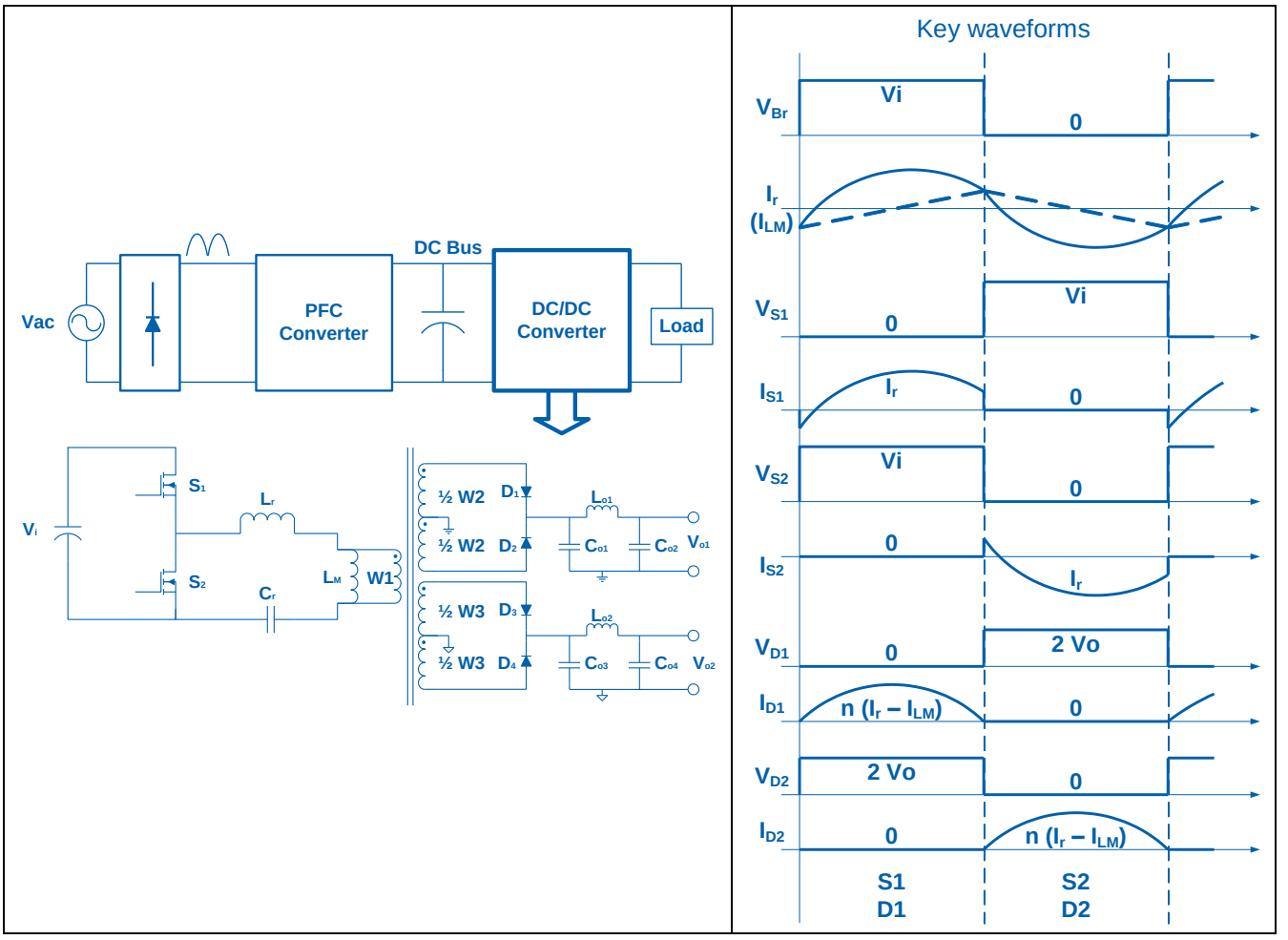

Figure 2.1: Schematic and basic waveforms for HB LLC converter operating at resonant frequency.

3 Design Equations

The following are design equations for the LLC converter, including a design example using Half Bridge front-end and two center-tapped, passively rectified outputs to clarify the use of the equations. The example uses a proposed design process to establish resonant tank component values based on certain guidelines.

Input voltage {Vi}	320 V-420 Vdc (PFC pre-regulated bus – universal ac)
Output voltage 1 {Vo1}	24 V
Maximum output current 1 {Io1,max}	6 A
Output voltage 2 {Vo2}	12 V
Maximum output current 2 {Io2,max}	5 A
Maximum power {Po,max}	204 W
Switching frequency {fs}	100 kHz, nominal at full load, 380Vdc

Table 3.1: Specifications

3.1 Converter gain

The winding ratio between the primary winding, n_{pri}, and the secondary winding, n_{sec}, gives one gain-term as in other transformer isolated SMSP:

$$G_{XFMR} = \frac{n_{sec}}{n_{pri}} \quad (1)$$

Since the resonant converter gain is expressed with respect to sinusoidal in- and out-puts, both need conversion, which results in a total gain factor of

$$G_{HB} \approx \frac{1}{2} \quad , \quad G_{FB} \approx 1 \quad (2)$$

For Half-bridge or fullbridge front-ends respectively.

The last gain-term is the one for the resonant network:

$$K(Q,m,Fx) = \frac{Fx^2(m-1)}{\sqrt{(m \cdot Fx^2 - 1)^2 + Fx^2 \cdot (Fx^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \quad (3)$$

Where

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}}$$ Quality factor (4)

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{n_{pri}^{\ 2}}{n_{sec}^{\ 2}} \cdot R_o$$ Reflected load resistance (5)

$$Fx = \frac{f_s}{f_r}$$ Normalized switching frequency (6)

$$f_r = \frac{1}{2\pi\sqrt{L_r \cdot C_r}}$$ Resonant frequency (7)

$$m = \frac{L_r + L_m}{L_r}$$ Ratio of total primary inductance to resonant inductance (8)

The resonant gain will have a general shape as shown below in Figure 3.1:

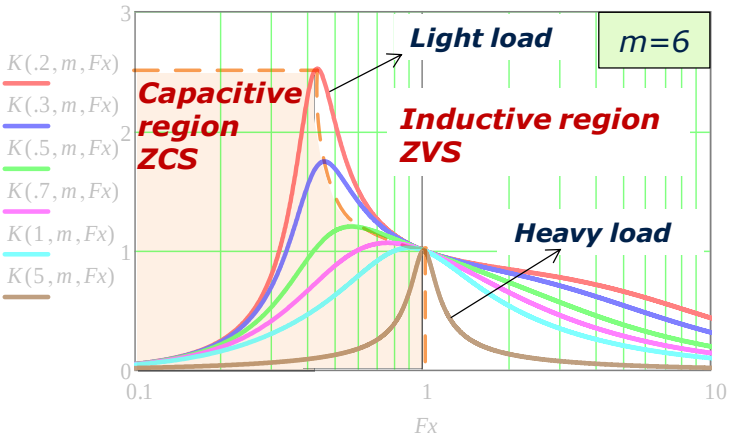

Figure 3.1: Shape of the resonant gain at different values of Q

Gain is 1 at Fx=1 and lower for Fx>1. Assuming Q<1, gain is higher for Fx<1. The minimum frequency of operation is limited to the frequency at which the gain peaks. The amplitude of the peak represents the maximum gain. R_{ac} is a function of output voltage and output current, which are given at maximum output

power. The Lr * Cr product is given by (7) {fr is selected to equal the desired switching frequency at nominal operation to obtain best efficiency at that operating point}. A larger Lr (and smaller Cr) results in a lower maximum gain via Q.

m is the only variable that contains Lm (the transformer magnetizing inductance). A larger value of Lm brings the transformer closer to ideal and improves efficiency, but makes it harder to achieve ZVS. A larger value of Lm also reduces maximum possible gain: Q and m influence each other and determine maximum gain. The ratio of maximum gain to nominal gain (a gain of 1) must be high enough to accommodate for the ratio of nominal input voltage to minimum input voltage. This cannot be made up for by the other (non-frequency dependent) gains.

3.2 Determining resonant components

Given the specifications in Table 3.1, we can see that the minimum resonant gain required is

$$G_{Vi,\min} = \frac{V_{i,nom}}{V_{i,\min}} \cdot 1.1 = 1.3 \quad \textbf{(9)}$$

When adding 10% for head room. The resonant frequency, f_r, is set equal to the desired switching frequency for best efficiency.

Picking the right – optimal – maximum Q and m values is a very involved task that requires iterations, physical experiments and complex calculations, which is not the purpose of present Design Note. Instead some guidelines will be followed. Figure 3.1 shows gain plots for several values of Q in the range from “small” (0.2) to “large” (5) for some quasi-arbitrarily chosen value of m=6. At the maximum Q (heaviest load), the minimum resonant gain (determined above in (9)) must be achievable. A value of Q_{MAX} higher than ~0.7 will probably not satisfy the requirements. Q will have its minimum value at light loads, where the gain curve becomes very shallow at higher frequencies. The converter must be able to buck the voltage enough when the input voltage is high. Subtracting 10% for tolerances, the bucking-gain is obtained:

$$G_{Vi,\max} = \frac{V_{i,nom}}{V_{i,\max}} \cdot 0.9 = 0.81 \quad \textbf{(10)}$$

We see from Figure 3.1 that Q_{max} values less than ~0.3 will result in high frequency at high input voltages – which will decrease efficiency (added switching loss). A good choice of Q_{max} is somewhere in the middle:

$$Q_{\max} = 0.5 \quad \textbf{(11)}$$

Since Q_{max} has been solidified, we must pick the highest m-value that satisfies the minimum gain requirement (remember that high m is desirable, since the transformer is more ideal). For a Q-value of 0.5, the gain is plotted for different values of m:

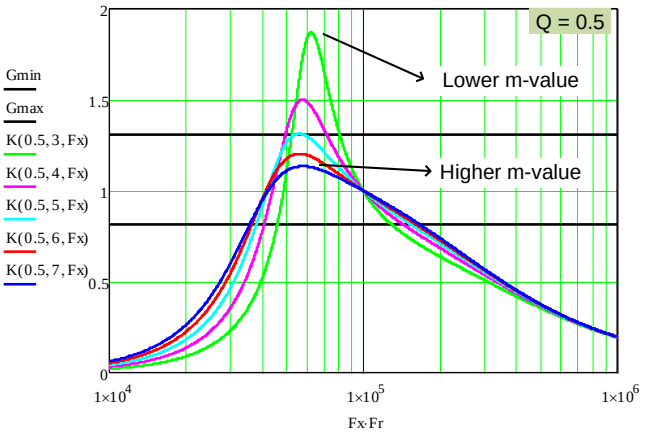

Figure 3.2: Resonant gain curves for different values of m when Q = 0.5

The maximum gain occurs at a normalized frequency that can be approximated by

$$F_{G\max} \approx \frac{1.25}{\sqrt{m}} \tag{12}$$

The highest permissible value of m can be found to be

$$m = 5 \tag{13}$$

Resulting in maximum gain of

$$K\left(0.5{,}5{,}\frac{1.25}{\sqrt{5}}\right) = 1.31 \quad @ \quad 56\,kHz \tag{14}$$

Which is confirmed graphically above in Figure 3.2, where m-values higher than 5 will result in insufficient maximum gain, but the curve for m = 5 just touches the line indicating the minimum required gain.

The frequency required at high input voltage (and full output power) can be found using $G_{Vi,max}$ from (10).

The maximum frequency for full output power is:

$$K(0.5{,}5,\, f_{\max}) = G_{Vi,\max} \quad \rightarrow \quad f_{\max} = 154\,kHz \tag{15}$$

Which is reasonable. For 50% load fs_{max} is 189kHz and 294kHz at 10% load. The actual maximum frequency is typically limited and the converter intead operates in burst-mode to achieve sufficient bucking at light loads while maintaining high efficiency.

The turns ratio for the transformer must be calculated to give the required overall gain

$$G_{HB} \cdot G_{XFMR} \cdot G_{res} = \frac{V_o}{V_i} \quad \rightarrow \quad n_1 = \frac{n_{pri}}{n_{\sec 1}} \approx 8.5, \;\; n_2 = \frac{n_{pri}}{n_{\sec 2}} \approx 17 \tag{16}$$

Accounting for a voltage-drop term of sqrt(m/(m-1)) across the secondary side leakage inductance and a secondary side diode forward drop of 0.6 V.

In order to arrive at the maximum effective reflected ac resistance, first we reflect each effective full-power output resistance through the transformer individually

$$R_{ac1} = \frac{8}{\pi^2} \cdot n_1 \cdot \frac{V_{o1}}{I_{o1}} = 234\,\Omega \quad , \quad R_{ac2} = \frac{8}{\pi^2} \cdot n_2 \cdot \frac{V_{o2}}{I_{o2}} = 562\,\Omega \tag{17}$$

Then the total reflected AC equivalent resistor at full load is the paralleled value:

$$R_{ac} = \frac{R_{ac1} \cdot R_{ac2}}{R_{ac1} + R_{ac2}} = 165\,\Omega \tag{18}$$

The three unknown variables, Lr, Lm and Cr can now be found by solving the three equations for Q, fr and m given in (4), (7) and (8) respectively:

L_r=132 µH

L_M=526 µH

C_r=19 nF

An integrated transformer can be built on a PC47 EC32 core on a split-type bobbin, which could achieve

L_r=120 µH		m=5.3
L_M=516 µH and	→	Q_{max}=0.447
C_r=22 nF (standard capacitor value)		f_r=98 kHz

These physically realizable component values and subsequent m, Q and f_r values lead to resonant gain curves plotted below for various load levels:

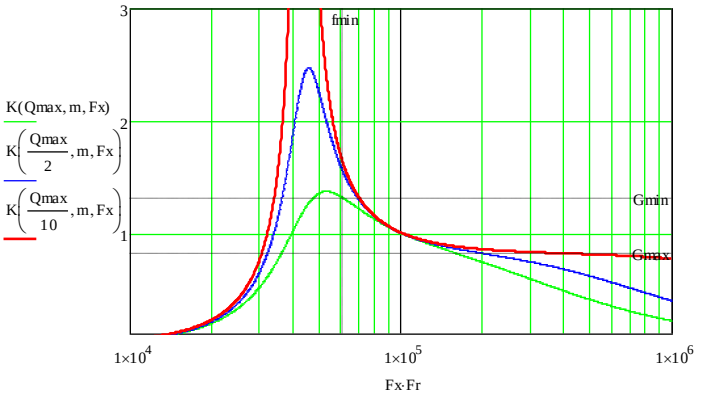

Figure 3.3: Specific resonant gain at full load (green), 50% load (blue) and 10% load (red)

The transformer design is outside the scope of this Design Note, but could be built with 34 turns on W1 (primary), 8 turns (center-tapped) for W2 (Seconday 1) and 4 turns (center-tapped) for W3 (secondary 2). This transformer construction would avoid saturation, and the windings would fit assuming appropriate wire gauge and isolation tape.

f_s can now be found for any operating condition.

3.3 Rectifier diode considerations

Worst operating condition for secondary side diodes is under full load (since RMS current is highest). We assume lowest input voltage – in order to get an operating point.

The switching frequency is first found under this condition:

$$K(Q_{\max}, m, f_{\min}) = \frac{V_i}{V_{i,\min}} \quad \rightarrow \quad f_{\min} = 71\,kHz \tag{19}$$

For Fx<1, each diode peak current can then be calculated as (not valid for Fx>1)

$$I_{D1,pk} = I_{D2,pk} = \frac{\pi}{2} \cdot I_{o1} \cdot \frac{f_r}{f_{\min}} = 13\,A \tag{20}$$

$$I_{D3,pk} = I_{D4,pk} = \frac{\pi}{2} \cdot I_{o2} \cdot \frac{f_r}{f_{\min}} = 11\,A \tag{21}$$

We must select diodes that can handle these peak currents with appropriate derating (20%).

During the half-cycle when D1 conducts, V_{o1} is forced across ½ W2 (since V_{o1} exists across C_{o1}). Since D1 conducts, D2 has all of W2 voltage across it. The opposite is true for D1:

$$V_{D1,\max} = V_{D2,\max} = V_{o1} \cdot 2 = 48\,V \tag{22}$$

$$V_{D3,\max} = V_{D4,\max} = V_{o2} \cdot 2 = 24\,V \tag{23}$$

We must select diodes with a reverse voltage rating high enough to allow for appropriate derating (20%).

The rectifying diodes will reverse recover, so low reverse recovery charge is important. For this application, Schottky diodes can be used with negligible reverse recovery characteristics.

To calculate the rectifying diode power loss, we first realize each carry half the corresponding output current on average:

$$P_{D1,con} = P_{D2,con} = \frac{I_{o1}}{2} \cdot V_{f,D1} = 1.5\,W \tag{24}$$

$$P_{D3,con} = P_{D3,con} = \frac{I_{o2}}{2} \cdot V_{f,D3} = 0.875\,W \tag{25}$$

For $V_{f,D1}$=0.5 V (reasonable value) and
$V_{f,D3}$=0.35 V (reasonable value)

For Schottky diodes – that have virtually no reverse recovery – the capacitance determines switching loss

$$P_{D1,sw} = P_{D2,sw} = \frac{1}{2} \cdot C_{T,D1} \cdot V_{D1,\max}{}^2 \cdot f_{\min} = 33\,mW \tag{26}$$

$$P_{D3,sw} = P_{D4,sw} = \frac{1}{2} \cdot C_{T,D3} \cdot V_{D3,\max}{}^2 \cdot f_{\min} = 6\,mW \tag{27}$$

For $C_{T,D1}$=400 pF (reasonable value) and
$C_{T,D3}$=300 pF (reasonable value)

Total rectifier diode loss is thus (for 60/35V rated Schottky diodes rated at least 15 A)

$$P_{D1,tot} = P_{D2,tot} = P_{D1,con} + P_{D1,sw} = 1.5\,W \tag{28}$$

$$P_{D3,tot} = P_{D3,tot} = P_{D3,con} + P_{D3,sw} = 0.9\,W \tag{29}$$

For a reasonable choice of Schottky diodes.

3.4 MOSFET considerations

In an off-line application with a pre-regulated bus, the primary side MOSFETs each see a maximum voltage equal to the bus voltage. Due to resonant operation, over- and under-shoot is negligible, so minimum breakdown voltage rating of the MOSFETs must be

$$V_{br,S1,S2} \geq V_{in,\max} \cdot 1.2 = 504\,V \quad \textbf{(30)}$$

When employing standard 20% derating.

Different families of MOSFETs are available in this voltage rating range. The diverse CoolMOS technology families of Super Junction MOSFETs offer different characteristics and optimizations, so it is important to understand the requirements the LLC topology puts on the MOSFETs. Following are some of the selection considerations:

The ideal MOSFET for the LLC converter would allow for zero dead time (maximum power transfer) and no conduction loss. R_{on} is obviously important for the latter consideration, but the former requires a little more explanation. As will be shown later, the dead time must be sufficient to cover three phases of MOSFET transition: turn-off time delay (from gate drive signal goes low until MOSFET begins to turn off), turn-off time (the time it takes for the MOSFET channel to completely turn off) and resonant transition time (the time it takes for the drain-source voltage to resonantly transition to the level of the input voltage):

- Low FOM: R_{on}*Q_g (turn-off time delay and channel turn-off time)
- Low FOM: R_{on}*Q_{oss} (resonant drain-source voltage transition time)

Since this topology is expected to operate fully in ZVS-mode (given appropriate MOSFET Q_g, Q_{oss}, selected Q_{max} and m-values – and ample pre-programmed deadtime), switching loss caused by E_{oss} can be considered negligible, and to this extent, E_{oss} is not a critical MOSFET parameter for LLC.

What does complicate matters, though, is the fact that the MOSFET body diode could potentially experience hard current commutation in abnormal conditions, if steps are not taken specifically to avoid this. Particularly Super Junction MOSFETs exhibit very snappy reverse recovery characteristics, which – if severe enough – could interact with parasitic inductances and cause avalanche breakdown and consequently catastrophic failure of the MOSFET. The CoolMOS C6/E6 family as well as the CFD and CFDII technologies address this potential issue by employing a self-snubbing scheme causing the channel to partially turn on at high dv/dt (induced by Cgd/Cgs voltage divider) in order to prevent avalanche breakdown.

The recommended CoolMOS™ MOSFET family for LLC applications is P6 provided necessary precautions have been taken to avoid hard commutation of the body diode. This family of parts offers superior price/performance ratio with low FOMs, which means MOSFET turn-off and resonant voltage transition can happen in a shorter deadtime period. The fast turn-off speed is further augmented by a slightly elevated threshold- and plateau voltage compared to other CoolMOS families.

In implementations where hard body diode commutation is a concern, the more conservative recommendation is the C6/E6 CoolMOS™ MOSFET family, which provide the extra measure of protection during hard body diode commutation.

The current in the resonant tank during operation is the sum of currents in the magnetizing inductance and the primary transformer winding. The shape of the resonant- and magnetizing currents are given below:

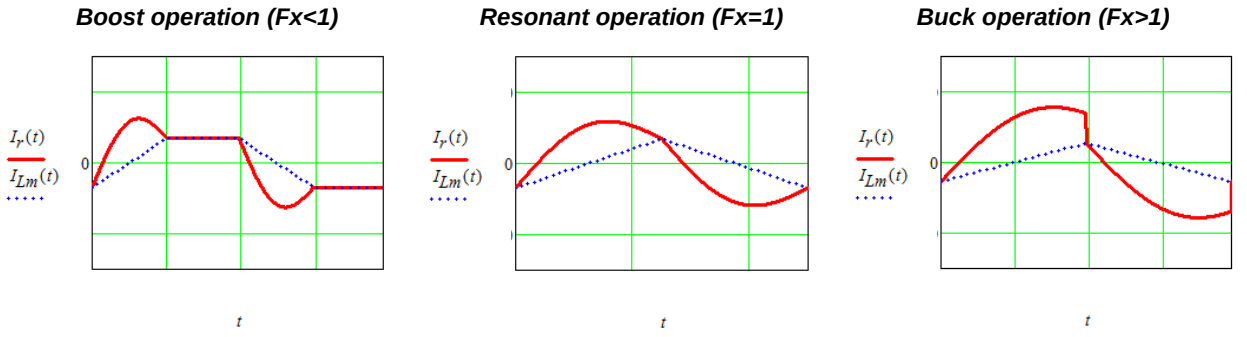

Figure 3.4: Resonant tank current and Magnetizing current general shapes in different modes

The resonant current flows through the primary MOSFETs. It has its highest peak-value in boost operating mode, when the input voltage is at a minimum. The current through the transformer primary is given by the following equation (NB: only valid for Fx≤1):

$$i_{pri}(t) = \begin{cases} \left(\frac{1}{n_1}\cdot I_{D1,pk} + \frac{1}{n_2}\cdot I_{D3,pk}\right)\cdot \sin\left(2\cdot\pi\cdot f_r\cdot t\right) & if\ \ 0 < t \le \frac{T_r}{2} \\ 0 & if\ \ \frac{T_r}{2} < t \le \frac{T_s}{2} \\ -\left(\frac{1}{n_1}\cdot I_{D1,pk} + \frac{1}{n_2}\cdot I_{D3,pk}\right)\cdot \sin\left(2\cdot\pi\cdot f_r\cdot\left(t-\frac{T_s}{2}\right)\right) & if\ \ \frac{T_s}{2} < t \le \frac{T_s}{2} + \frac{T_r}{2} \\ 0 & if\ \ \frac{T_s}{2} + \frac{T_r}{2} < t \le T_s \end{cases} \quad \textbf{(31)}$$

The magnetizing current is approximated by the following formula (NB: only valid for Fx≤1):

$$i_{Lm}(t) = \begin{cases} \frac{n_1\cdot V_{o1}}{L_m}t - \frac{n_1\cdot V_{o1}}{L_m\cdot 4\cdot f_r} & if\ \ 0 < t \le \frac{T_r}{2} \\ \frac{n_1\cdot V_{o1}}{L_m\cdot 4\cdot f_r} & if\ \ \frac{T_r}{2} < t \le \frac{T_s}{2} \\ -\frac{n_1\cdot V_{o1}}{L_m}\left(t-\frac{T_s}{2}\right) + \frac{n_1\cdot V_{o1}}{L_m\cdot 4\cdot f_r} & if\ \ \frac{T_s}{2} < t \le \frac{T_s}{2} + \frac{T_r}{2} \\ -\frac{n_1\cdot V_{o1}}{L_m\cdot 4\cdot f_r} & if\ \ \frac{T_s}{2} + \frac{T_r}{2} < t \le T_s \end{cases} \quad \textbf{(32)}$$

The total resonant current is the sum of the two as plotted below (actual values for design example):

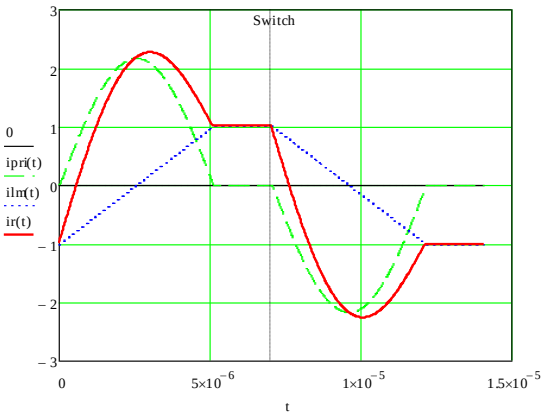

Figure 3.5: Resonant current plottet for full power at minimum input voltage

Where ipri(t) – the green dashed line – is the secondary side current reflected to the primary side
ilm(t) – the blue dotted line – is the magnetizing current and
ir(t) – the red solid line – is the sum of the two representing the total resonant tank current

The peak current can be found within the first half of the resonant period, where the derivative is 0:

$$\frac{d}{dt} i_r\left(0 < t < \frac{T_r}{2}\right) \equiv 0 \qquad \rightarrow \qquad i_{S1,pk} = i_{S2,pk} = 2.27\ A \tag{33}$$

We can select **IPA60R280E6**, which with a voltage rating of 600 V and pulsed current rating of 40 A easily satisfies the minimum requirements and is the more conservative choice with inherent self-snubbing. Alternatively the **IPA60R280P6** could be considered for higher efficiency if extra protection measures are taken. The following calculations assume selection of **IPA60R280E6**.

From t=0 to t=Switch, the high-side MOSFET conducts ir(t), for the remainder, the low-side MOSFET conducts, causing equal conduction losses of:

$$P_{S1,con} = P_{S2,con} = 0.5 \cdot i_{r,RMS}{}^2 \cdot R_{on} = 0.4\,W \tag{34}$$

Where

R_{on}=0.38 Ω (read off chart for typ value at 80°C junction temperature) and

$$i_{r,RMS} = \sqrt{f_{\min} \cdot \int_0^{\frac{1}{f_{\min}}} i_r{}^2(t)\,dt}$$ Is the RMS value of the resonant current **(35)**

The energy contained in the resonant inductances at the time of switching (for Fx≤1) is

$$E_{L,Switch} = \frac{1}{2} \cdot \left(L_m + L_r\right) \cdot I_{Lm}{}^2 = 250\ \mu J \tag{36}$$

Where

$$I_{Lm} = \frac{n_1 \cdot \left(V_{o1} - 0.5\right)}{L_m \cdot 4 \cdot f_r \cdot \sqrt{\frac{m}{m-1}}} \cong 0.89\ A \tag{37}$$

When accounting for voltage drops across the secondary side diodes and leakage inductance.

The energy required to swing both MOSFETs' output capacitances the entire input voltage can be read off of DataSheet:

$$E_{oss,tot} = 2 \cdot E_{oss,S1} \approx 7\ \mu J \quad \textbf{(38)}$$

For the chosen values of m and Q_{max} there is plenty of energy stored in the resonant tank to achieve ZVS given enough dead time.

Assuming Rg and Vdrv close to values in DataSheet, the Td(off) can be found in DS:

$$t_{d(off)} = 71\,ns\,(typ) \quad \textbf{(39)}$$

The time to turn off channel is normally associated with charging C_{gd} to the final voltage via gate current for hard-switching applications. In softswitching applications, the calculation is more complex, and typically sophisticated simulations are required to arrive at a reasonable estimate. For simplicity, we estimate similar time interval as Td(off) to turn off the channel.

Assuming constant current during DT (approximately), the time required for full resonant switching is

$$t_{res(off)} = 2 \cdot C_{o(tr)} \cdot \frac{V_i}{I_{Lm}} \approx 214\,ns \quad \textbf{(40)}$$

Total dead time required is thus

$$t_{DT,tot} = t_{d(off)} + t_{off} + t_{res(off)} \approx 356\,ns \quad \textbf{(41)}$$

With a higher value of m, I_{Lm} is lower, which means longer DT required (power transfer suffers). With a lower value of MOSFET Qg and Co(tr), m can be higher with same DT or DT can be lower; thus increasing efficiency.

With a properly designed resonant tank and correctly tuned Dead Time, the MOSFETs turn on resonantly (full ZVS), so only the turn-off loss contributes to switching loss. Turn-off loss can be approximated by:

$$P_{S1,sw} \approx 0.5 \cdot I_{Lm} \cdot V_{i,\min} \cdot t_{d(off)} \cdot f_{\min} = 0.71 W * \quad \textbf{(42)}$$

For $t_{d(off)}$=71 ns (from Data Sheet, with suggested Rg and Vdrv)

Gate drive loss is calculated by

$$P_{S1,Qg} \approx Q_g \cdot V_{drv} \cdot f_{\min} = 37\ mW \quad \textbf{(43)}$$

So the total MOSFET loss is

$$P_{S1} = P_{S2} = P_{S1,con} + P_{S1,sw} + P_{S1,Qg} = 1.2\,W \quad \textbf{(44)}$$

For the selected **IPA60R280E6**

*This approximation is only a first-order approach to give a rough idea. Interaction between channel conduction and non-linear output capacitance behavior makes ZVS turn-off loss in SJ MOSFETs so complex to calculate that simulation or practical experimentation is recommended for more accurate estimation/measurements.

3.5 Output filter considerations

The output filter need only consist of an output capacitor, since the current is smooth (does not have high harmonic content). This capacitor – Co1 or Co3 conversely – does handle a fairly large AC current (the entire current ripple found in previous chapter on rectifying diode considerations), so a type with a low ESR should be selected. This capacitor will only see the output voltage, so voltage rating is straight-forward. The capacitance can be selected from output voltage ripple requirements (since current wave shape and magnitude are known). The current into it can be determined from the sec side diode currents less output current, and the loss is thus

$$P_{Co1} = I_{Co1,RMS}^{\ 2} \cdot ESR_{Co1}\ W \quad , \quad P_{Co3} = I_{Co3,RMS}^{\ 2} \cdot ESR_{Co3}\ W \quad \textbf{(45)}$$

The secondary filter – L_{o1}, C_{o2} and L_{o2}, C_{o4} conversely – only sees minor voltage- and current ripples, and could be omitted as stated previously. The secondary filter selection could be determined by some specific requirements such as EMI. The DCR of the secondary inductors does add copper loss.

3.6 Resonant reactive elements considerations

The resonant tank has a significant AC current flowing in it as detailed in previous sections. The DC-component of the resonant current is zero, so the components must be designed/picked with AC resistance in mind. The transformer can be implemented – as in the design example presented herein – as an integrated magnetic structure. The entire resonant current flows through the physical primary winding, causing loss based on the AC resistance of the primary winding (note: DCR is not a precise measure of the effective resistance causing loss). The total copper loss can be calculated as the sum of the secondary side copper losses and the primary side loss incurred by rms currents squared multiplied by AC resistances.

$$P_{XFRM,cu} = I_{r,RMS}^{\ 2} \cdot ACR_{pri} + I_{\sec 1,RMS}^{\ 2} \cdot ACR_{\sec 1} + I_{\sec 2,RMS}^{\ 2} \cdot ACR_{\sec 2}\ W \quad \textbf{(46)}$$

The transformer also has associated core loss that depends on core material.

The ESR of the resonant capacitor directly causes similarly incurred ESR loss, and a type with very small ESR should be chosen. Alternatively several parallel capacitors could be chosen to further reduce ESR:

$$P_{Cr} = I_{r,RMS}^{\ 2} \cdot ESR_{Cr}\ W \quad \textbf{(47)}$$

The voltage rating of the resonant capacitor is important as well, since it will be charged positivily during the dead time by the same current that charges/discharges the MOSFET output capacitances. If C_r value is large compared to the $C_{oss,tot}$ then this voltage is negligible, and the voltage rating could be same as for MOSFETs:

$$C_{r,Vrate} = V_{i,\max} \cdot 1.2 = 504\,V \quad \textbf{(48)}$$

If the transformer is not a single, integrated structure, then the discrete resonant inductor has its own copper loss:

$$P_{Lr,cu} = I_{r,RMS}^{\ 2} \cdot ACR_{Lr}\ W \quad \textbf{(49)}$$

And core loss.

3.7 Controller/driver considerations

The contol scheme and controller chip implementation is a topic onto itself and will not be detailed herein. When picking a controller for the LLC resonant topology, one must carefully consider some features that are either necessary or niceties:

- Adjustable minimum frequency {requirement}
- Soft-start scheme (non-trivial) {requirement}
- Sufficient pre-programmed or programmable dead time {requirement}
- Sufficiently high, limited maximum frequency {requirement}
- OCP (Over Current Protection) {requirement}
- OVP (Over Voltage Protection) {requirement}
- Input under-voltage protection {requirement}

A reasonable choice for this design example could be **ICE1HS01G-1**, which fulfills all the requirements in a fairly small SO-8 package.

If higher performance, more freedom and more adjustability is required, the **ICE2HS01G** can be recommended, which additionally allows synchronous rectification and fully adjustable dead time.

4 References

[1] Infineon Technologies: EVALHS-200W-ICE1HS01G, 200W SMPS Evaluation Board using LLC Half Bridge Resonant Controller ICE1HS01G, Application Note V1.1 06 Dec 2010.

[2] Infineon Technologies: ANPS0031 –ICE1HS01G, Half Bridge LLC Resonant Converter Design using ICE1HS01G, Application Note V1.0 12 August 2009.

[3] Infineon Technologies: ICE2HS01G datasheet, High Performance Resonant Mode Controller, V1.1, August 2011.

[4] Infineon Technologies: Design Guide for LLC Converter with ICE2HS01G, V1.0, July 2011.

[5] Infineon Technologies: 300W LLC Evaluation Board with LLC controller ICE2HS01G, V1.1, August 2011.

Symbols used in formulas

V_i: Input voltage
$E_{oss,tot}$: Energy required to swing both MOSFETs output capacitance the entire input voltage range
F_{Gmax}: maximum gain for normalized frequency
G_{Vi},min: minimum resonant gain
G_{HB}: Half Bridge sinusoidal gain factor
G_{FB}: Full Bridge sinusoidal gain factor
R_{ac}: total AC equivalent resistance at full load reflected to the primary
V_{o1}: Output voltage
I_{o1}: Output current
$I_{r,RMS}$: RMS value of tank resonant current
$P_{o,max}$: Maximum output power
Fx: Normalized switching frequency
f_r: Resonant frequency
T: Switching time period
L_R: Resonant inductance
L_M: Magnetizing inductance
m: Ratio of total primary inductance to series resonant inductance
$I_{M.pk}$: Peak magnetizing current
N_p: Number of transformer's primary turns
N_s: Number of transformer's secondary turns
B_{max}: Peak magnetic flux
A_c: Core sectional area
P_{core}: Core loss
$P_{XFRM.cu}$: Total transformer copper loss
P_{Co1}: Output filter capacitor loss from ESR
P_{Cr}: Resonant capacitor power loss from ESR
$P_{Lr.cu}$: Resonant inductor copper loss
$P_{S1.Qg}$: Gate drive loss
$T_{res(off)}$: MOSFET switching off time
$t_{DT.tot}$: Total dead time required
$I_{S,rms}$: Primary MOSFET rms current
$P_{S,cond}$: Primary MOSFET conduction loss
$P_{S.off}$: Primary MOSFET switching off power loss
$P_{S.gate}$: Primary MOSFET gate drive loss
Q: Quality factor of resonant circuit
R_{ac}: Reflected AC load resistance
$V_{SR,stress}$: SR MOSFET max voltage stress
$R_{on.sec(100C)}$: SR MOSFET on resistance at 100^{o}C
$I_{SR,rms}$: SR MOSFET rms current
$P_{SR,cond}$: SR MOSFET conduction loss
$P_{SR,gate}$: SR MOSFET gate drive loss
$P_{SR,oss}$: SR output capacitance loss
Q_{oss}: MOSFET output capacitance charge
Q_{gs}: MOSFET gate-source charge
Q_{gd}: MOSFET gate-drain charge
Q_g: MOSFET total gate charge

R_g: MOSFET gate resistance
Vbr: Drain-source MOSFET breakdown voltage rating
V_{pl}: MOSFET gate plateau voltage
V_{th}: MOSFET gate threshold voltage
ESR: Capacitor resistance
$I_{Cin.rms}$: Input capacitor rms current
P_{Cin}: Input capacitor conduction loss