

Half-Bridge LLC Resonant Converter Design Using NCP4390/NCV4390

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INTRODUCTION

Among many resonant converters, LLC resonant converter has been the most popular topology for high power density applications. This topology has many advantages over other resonant topologies: it can regulate the output over entire load variation with a relatively small variation of switching frequency, it can achieve zero voltage switching (ZVS) for the primary side switches and zero current switching (ZCS) for the secondary side rectifiers, and the resonant inductor can be integrated into a transformer. The NCP4390 series is an advanced pulse-frequency-modulation (PFM) controller series for LLC resonant converters with synchronous rectification (SR) that offers best-in-class efficiency for isolated DC/DC converters. Compared to the conventional PFM controllers in the market, NCP4390 offers several unique features that can maximize efficiency, reliability, and performance.

1. Charge-current control: Voltage-mode control, where the error-amplifier output voltage directly controls the switching frequency, has been typically used for LLC resonant converters. However, the

compensation network design of the LLC resonant converter is relatively challenging since the frequency response of the LLC resonant converter with voltage-mode control has very complicated characteristics with four poles where the location of the poles changes with input voltage and load condition. NCP4390 employs a current-mode control technique based on the charge quantity of each switching cycle, which provides a better control-to-output transfer function of the power stage, simplifying the feedback loop design while allowing true input power limit capability and inherent line feed-forward.

2. Dual-edge-tracking synchronous-rectification (SR) control: NCP4390 uses a dual-edge-tracking method that anticipates the SR current zero-crossing instant with respect to two different time references. This technique not only minimizes the dead time during the normal operation but also provides stable SR control during any transient and mode change.

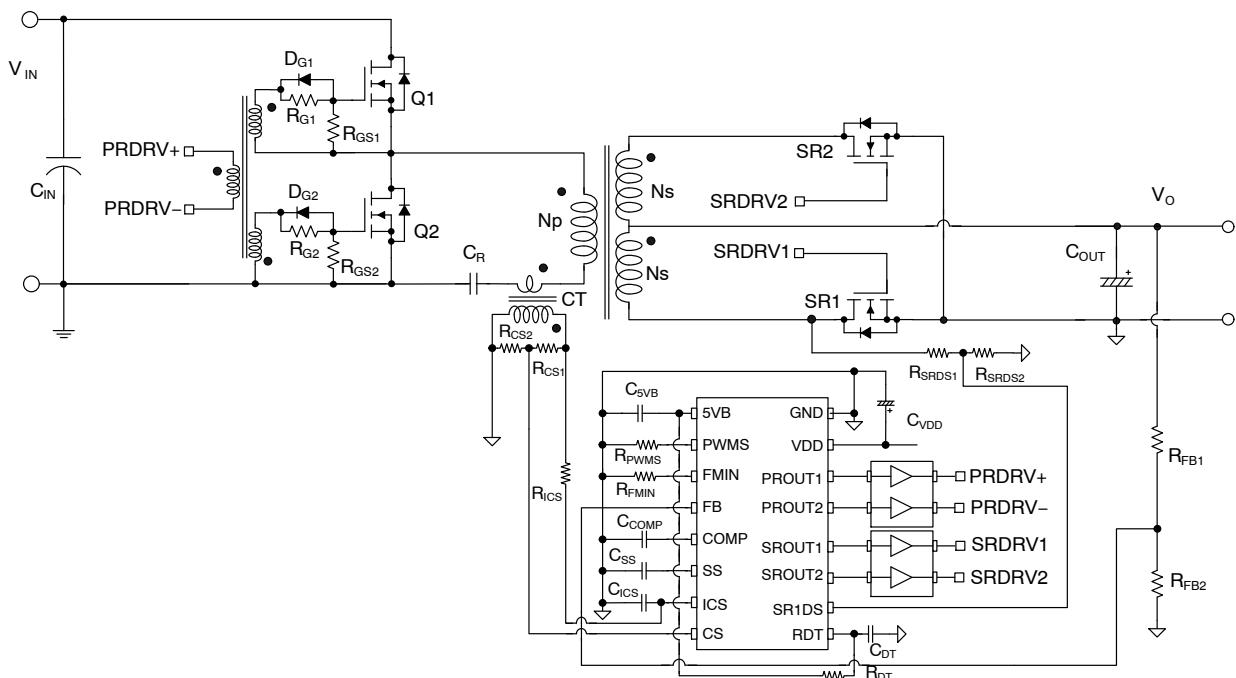


Figure 1. Schematic of Half-bridge LLC Resonant Converter

This application note presents design considerations of the half-bridge LLC resonant converter employing NCP4390. It includes an explanation of the LLC resonant converter operation principle, designing the transformer and resonant network, and selecting the components. The step-by-step design procedure explained with a design example helps design the LLC resonant converter.

LLC RESONANT CONVERTER AND FUNDAMENTAL APPROXIMATION

Figure 2 shows the simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor.

Figure 3 illustrates the typical waveforms of the LLC resonant converter. It is assumed that the operation frequency is same as the resonance frequency, determined by the resonance between L_r and C_r . Since the magnetizing inductor is relatively small, there exists considerable amount of magnetizing current (I_m), which freewheels in the primary side without involving in the power transfer. The primary-side current (I_p) is a sum of the magnetizing current and the secondary-side current (I_D) referred to the primary.

In general, the LLC resonant topology consists of three stages shown in Figure 2: a square-wave generator, a resonant network, and a rectifier network.

- The square-wave generator produces a square wave voltage, V_d , by driving switches Q_1 and Q_2 alternately with a 50% duty cycle for each switch. The controller usually introduces a short dead time between the consecutive transitions. The square-wave generator can be full-bridge or half-bridge type. The full-bridge square-wave generator produce a square wave having double amplitude from the half-bridge ones.
- The resonant network consists of a capacitor, leakage inductances, and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Essentially, only sinusoidal current passes through the resonant network even though a square wave voltage applies to the resonant network. The current (I_p) lags the voltage applied to the resonant network (that is, the fundamental component of the square wave voltage (V_d) applied to the half-bridge totem pole), which allows the MOSFETs to turn on with zero drain-to-source voltage. As shown in Figure 3, the MOSFET turns on while the voltage across the MOSFET is zero due to the current flowing through the anti-parallel diode.
- The rectifier network produces DC voltage by rectifying the alternative current with rectifier diodes. The rectifier network can be full-wave bridge-rectification or center-tapped configuration with a capacitive output filter.

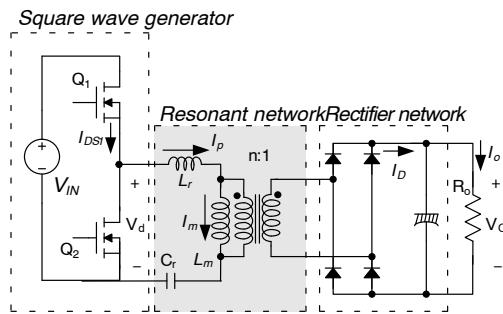


Figure 2. Schematic of Half-bridge LLC Resonant Converter

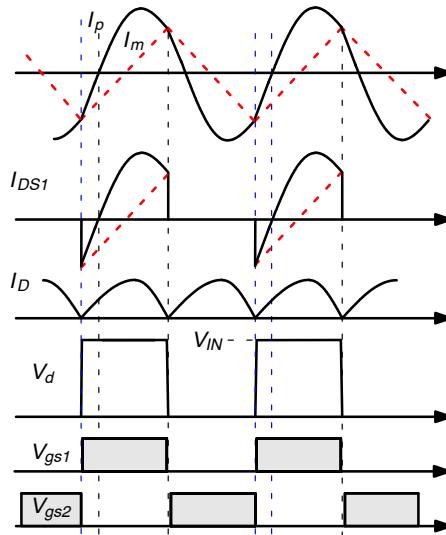


Figure 3. Typical Waveforms of Half-bridge LLC Resonant Converter

The filtering action of the resonant network allows the use of the fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the transferred power. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Figure 4 shows how to derive this equivalent load resistance. The primary-side circuit is replaced by a sinusoidal current source, I_{ac} , and a square wave voltage, V_{RI} , appears at the input to the rectifier. Since the average of $|I_{ac}|$ is the output current, I_o , I_{ac} is obtained as:

$$I_{ac} = \frac{\pi \times I_o}{2} \times \sin(\omega t) \quad (\text{eq. 1})$$

and V_{RI} is given as:

$$\begin{aligned} V_{RI} &= +V_o & \text{if } \sin(\omega t) > 0 \\ V_{RI} &= -V_o & \text{if } \sin(\omega t) < 0 \end{aligned} \quad (\text{eq. 2})$$

where V_o is the output voltage.

The fundamental component of V_{RI} is given as:

$$V_{RI}^F = \frac{4 \times V_o}{\pi} \times \sin(\omega t) \quad (\text{eq. 3})$$

Since harmonic components of V_{RI} are not involved in the power transfer, dividing V_{RI}^F by I_{ac} gives an AC equivalent load resistance:

$$R_{ac} = \frac{V_{RI}^F}{I_{ac}} = \frac{8}{\pi^2} \frac{V_o}{I_o} = \frac{8}{\pi^2} R_o \quad (\text{eq. 4})$$

Considering the transformer turns ratio ($n = N_p / N_s$), the equivalent load resistance shown in the primary side becomes:

$$R_{ac} = \frac{8n^2}{\pi^2} R_o \quad (\text{eq. 5})$$

By using the equivalent load resistance, we obtain the AC equivalent circuit as illustrated in Figure 5, where V_d^F and V_{RO}^F are the fundamental components of the driving voltage, V_d , and reflected output voltage, V_{RO} (nV_{RI}), respectively.

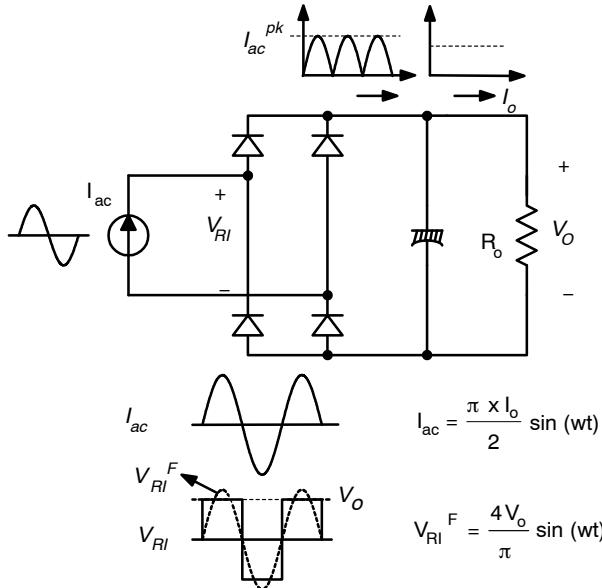


Figure 4. Derivation of Equivalent Load Resistance R_{ac}

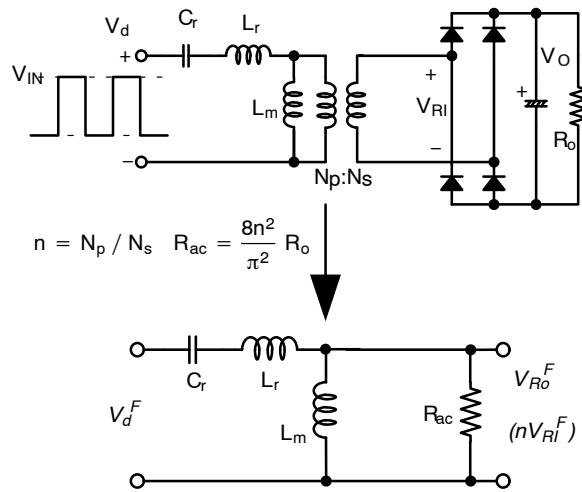


Figure 5. AC Equivalent Circuit for LLC Resonant Converter

With the equivalent load resistance obtained in equation (5), we can derive the characteristics of the half-bridge LLC resonant converter from Figure 5. A voltage gain, M , is obtained as:

$$M = \frac{V_{RO}^F}{V_d^F} = \frac{n \times V_{RI}^F}{V_d^F} = \frac{\frac{4n \times V_o}{\pi} \sin(\omega t)}{\frac{4}{\pi} \frac{V_{in}}{2} \sin(\omega t)} = \frac{2n \times V_o}{V_{in}} =$$

$$= \left| \frac{\left(\frac{\omega}{\omega_o} \right)^2 (m - 1)}{\left(\frac{\omega^2}{\omega_p^2} - 1 \right) + j \frac{\omega}{\omega_o} \left(\frac{\omega^2}{\omega_o^2} - 1 \right) (m - 1) Q} \right| \quad (\text{eq. 6})$$

where

$$L_p = L_m + L_r, R_{ac} = \frac{8n^2}{\pi^2} R_o, m = \frac{L_p}{L_r}$$

$$Q = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{ac}}, \omega_o = \frac{1}{\sqrt{L_r C_r}}, \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

As seen in equation (6), there are two resonant frequencies. One is determined by L_r and C_r , while the other is by L_p and C_r .

Equation (6) shows an unity gain at resonant frequency (ω_o), regardless of the load variation.

$$M|_{\omega=\omega_o} = \frac{(m - 1) \omega_p^2}{\omega_o^2 - \omega_p^2} = 1 \quad (\text{eq. 7})$$

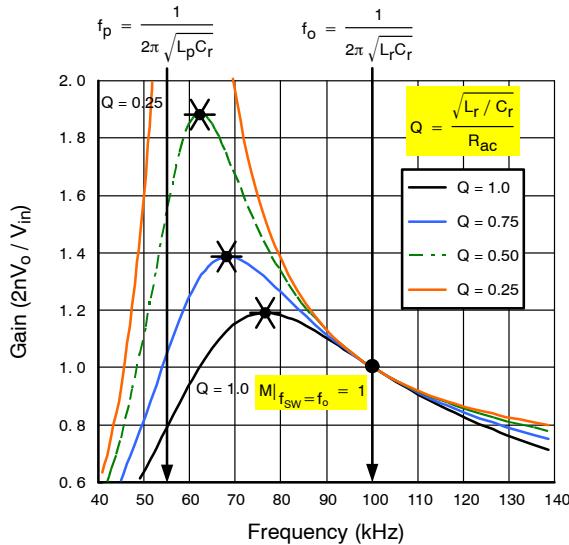


Figure 6. Typical Gain Curves of LLC Resonant Converter ($m = 3$)

Equation (6) is plotted in Figure 6 for different Q values with $m = 3$, $f_o = 100$ kHz, and $f_p = 57$ kHz. As observed in Figure 6, the LLC resonant converter shows gain characteristics that are almost independent of the load when the switching frequency is around the resonant frequency, f_o . This is a distinct advantage of the LLC resonant converter over the conventional series-resonant converter (SRC). Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation.

The operating range of the LLC resonant converter is limited by the peak gain (maximum attainable gain), which is indicated with a '*' sign in Figure 6. Note that the peak voltage gain does not occur at f_o nor f_p . The peak gain frequency where the peak gain is obtained exists between f_p and f_o . As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to f_o , and the peak gain drops; thus, the full load condition should be the worst case for the resonant network design.

CONSIDERATION FOR INTEGRATED TRANSFORMER

For practical design, it is common to implement the magnetic components (series inductor and shunt inductor) using an integrated transformer, where the leakage inductance is used as a series inductor while the magnetizing inductor is used as a shunt inductor. When building the magnetizing components in this way, the equivalent circuit in Figure 5 becomes as in Figure 7. The leakage inductance exists not only in the primary side but also in the secondary side. Not considering the leakage inductance in the secondary side results in an incorrect design.

In Figure 7, the effective series inductor (L_p) and shunt inductor ($L_p - L_r$) are obtained by assuming $n^2 L_{lks} = L_{lkp}$ and

referring the secondary side leakage inductance to the primary side as:

$$L_p = L_m + L_{lkp}$$

$$L_r = L_{lkp} + L_m \parallel (n^2 L_{lks}) = L_{lkp} + L_m \parallel L_{lkp} \quad (\text{eq. 8})$$

When handling an actual transformer, an equivalent circuit with L_p and L_r is preferred since these values can be easily measured with a given transformer. In an actual transformer, we can measure L_p and L_r in the primary side with the secondary-side winding opened and short-circuited respectively.

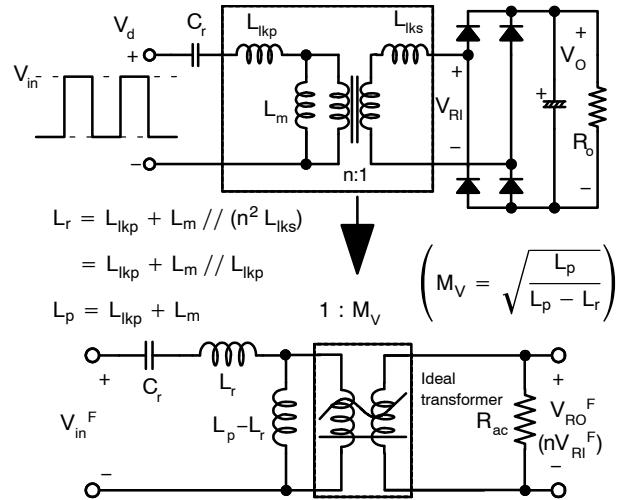


Figure 7. Modified Equivalent Circuit to Accommodate the Secondary-side Leakage Inductance

Figure 7 introduces a virtual gain, which is caused by the secondary-side leakage inductance. By adjusting the gain equation (6) using the modified equivalent circuit, a new gain equation for the integrated transformer is obtained:

$$M = \frac{2n \times V_o}{V_{in}} =$$

$$= \left| \frac{\left(\frac{\omega}{\omega_0} \right)^2 (m - 1) \times M_V}{\left(\frac{\omega^2}{\omega_p^2} - 1 \right) + j \frac{\omega}{\omega_0} \left(\frac{\omega^2}{\omega_0^2} - 1 \right) (m - 1) Q^e} \right|$$

$$= \left| \frac{\left(\frac{\omega^2}{\omega_0^2} \right) \sqrt{m(m - 1)}}{\left(\frac{\omega^2}{\omega_p^2} - 1 \right) + j \frac{\omega}{\omega_0} \left(\frac{\omega^2}{\omega_0^2} - 1 \right) (m - 1) Q^e} \right| \quad (\text{eq. 9})$$

where:

$$R_{ac}^e = \frac{8n^2}{\pi^2} \frac{R_o}{M_V^2}, \quad m = \frac{L_p}{L_r}$$

$$Q^e = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{ac}^e}, \quad \omega_0 = \frac{1}{\sqrt{L_r C_r}}, \quad \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

The gain at the resonant frequency (ω_o) is fixed regardless of the load variation, which is given as:

$$M = M_V = \sqrt{\frac{L_p}{L_p - L_r}} = \sqrt{\frac{m}{m - 1}} \text{ at } \omega = \omega_o \quad (\text{eq. 10})$$

The gain at the resonant frequency (ω_o) is unity when using individual core for series inductor, as shown in equation (7). However, when implementing the magnetic components with the integrated transformer, the gain at the resonant frequency (ω_o) is higher than unity due to the virtual gain caused by the leakage inductance in the transformer secondary side.

Figure 8 plots the gain of equation (9) for different Q^e values with $m = 3$, $f_o = 100$ kHz, and $f_p = 57$ kHz. Again, the LLC resonant converter shows gain characteristics almost independent of the load when the switching frequency is around the resonant frequency, f_o .

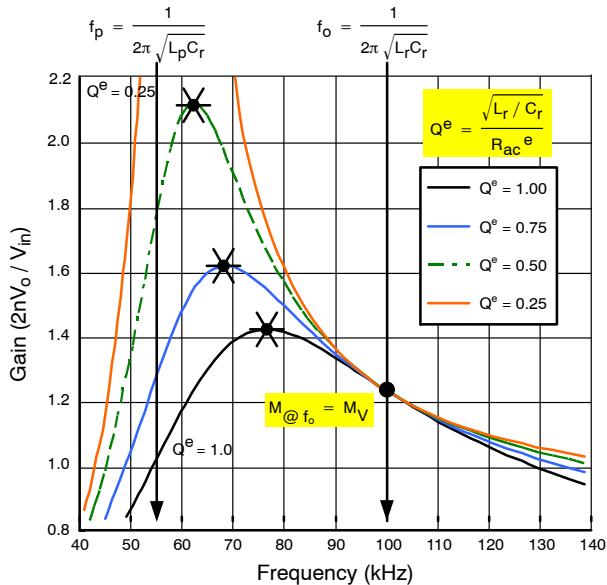


Figure 8. Typical Gain Curves of LLC Resonant Converter ($m = 3$) Using an Integrated Transformer

MAXIMUM ATTAINABLE GAIN

Even though we can obtain with the peak gain at a given condition with equation (6) or (9), it is difficult to express the peak gain in explicit form. To simplify the analysis and design, we collect the peak gains using simulation tools and depict in Figure 9 and Figure 10, which shows how the peak gain (maximum attainable gain) varies with Q for the different m values for separated and integrated resonant inductor design, respectively. It appears that we can obtain higher peak gain by reducing m or Q value. With a given resonant frequency (f_o) and Q value, decreasing m means reducing the magnetizing inductance, which results in an increased circulating current. Accordingly, there is a trade-off between the available gain range and conduction loss. Note that the integrated resonant inductor design in Figure 10 has higher gain than the separate resonant inductor design in Figure 9 due to the virtual gain M_V .

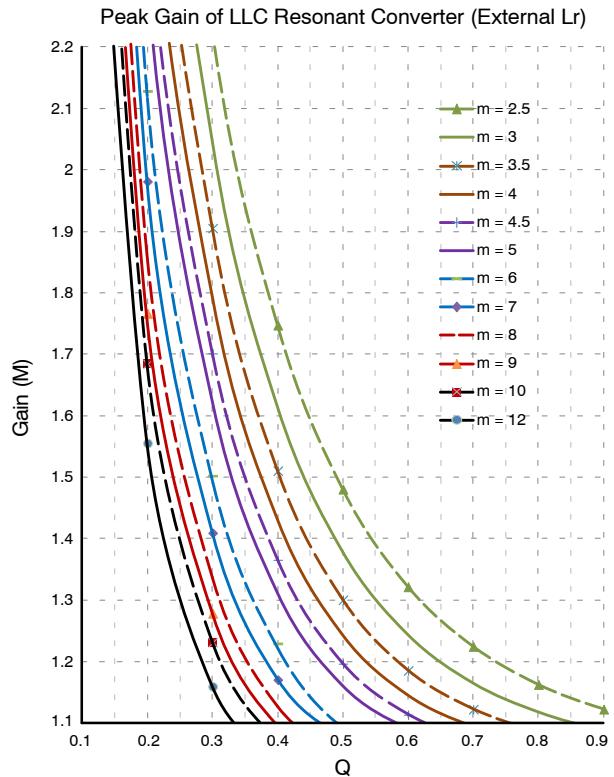


Figure 9. Peak Gain vs. Q for Different m Values (Separated Resonant Inductor)

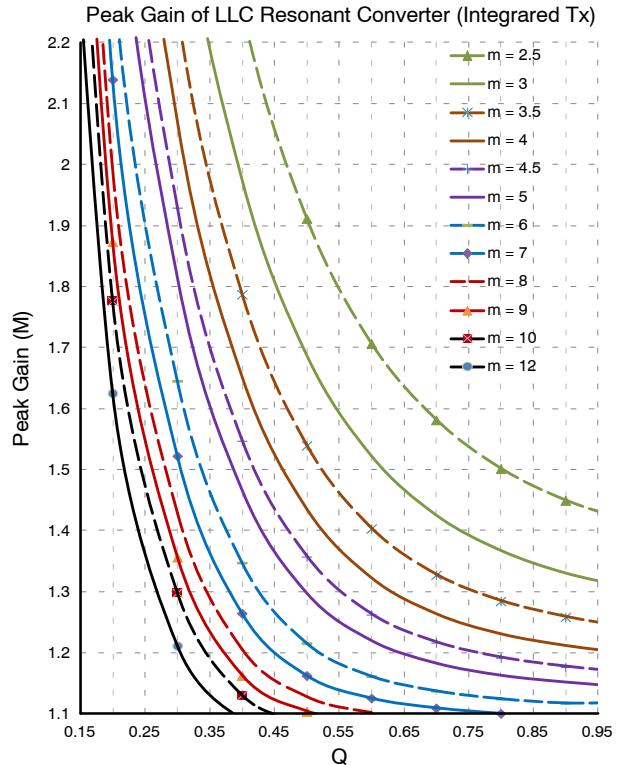


Figure 10. Peak Gain vs. Q for Different m Values (Integrated Resonant Inductor)

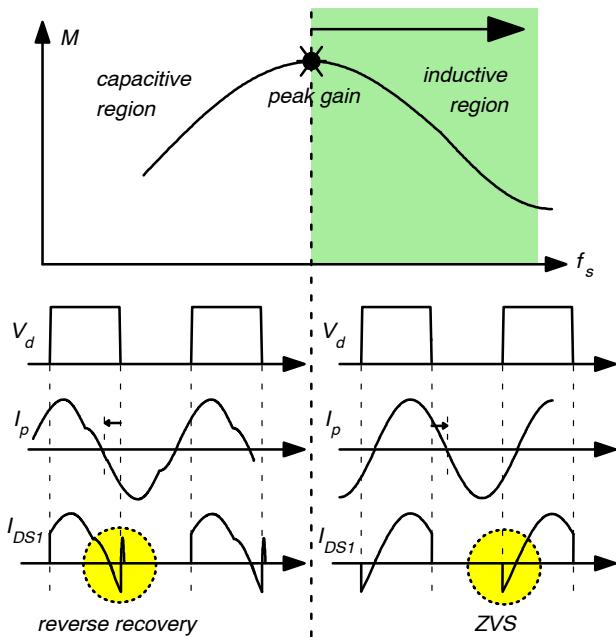


Figure 11. Operation Waveforms for Capacitive and Inductive Regions

Above the peak gain frequency, the input impedance of the resonant network is inductive, and the input current of the resonant network (I_p) lags the voltage applied to the resonant network (V_d). This fact permits the MOSFETs to turn on with zero-voltage switching (ZVS), as illustrated in Figure 11. Meanwhile, the input impedance of the resonant network becomes capacitive, and I_p leads V_d below the peak gain frequency. When operating in the capacitive region, the MOSFET body diodes generate reverse-recovery current during the switching transition, which results in severe noise. Another problem of entering into the capacitive region is that the output voltage becomes out of control since the slope of the gain reverses. So, the minimum switching frequency should be well limited above the peak gain frequency. NCP4390 also equips a non-ZVS protection by inspecting the CS signal at PROUT falling to prevent any prolonged operation in the capacitive region.

FEATURES OF NCP4390

NCP4390 employs a current-mode control technique based on charge control, simplifying the feedback loop design while allowing true input-power-limit capability. A closed-loop soft-start mechanism prevents saturation of the error amplifier and allows monotonic rising of the output voltage regardless of load condition. More, a dual-edge tracking adaptive SR control minimizes the body-diode conduction time, maximizing efficiency. Table 1 shows the pin description of NCP4390. Figure 12 shows the typical application schematic of the LLC resonant converter using NCP4390.

Table 1. PIN DESCRIPTION OF NCP4390

Pin#	Name	Pin Description
1	5VB	5V REF
2	PWMS	PWM mode entry level setting
3	FMIN	Minimum frequency setting pin
4	FB	Output voltage sensing for feedback control
5	COMP	Output of error amplifier
6	SS	Soft-start time programming pin
7	ICS	Integrated-current sensing pin for current mode control
8	CS	Instantaneous current sensing for over current protection
9	RDT	Dead time programming pin for the primary side switches and secondary side SR switches
10	SR1DS	SR1 drain-to-source voltage detection
11	SROUT2	Gate drive output for the secondary side SR MOSFET 2
12	SROUT1	Gate drive output for the secondary side SR MOSFET 1
13	PROUT2	Gate drive output 2 for the primary side switch
14	PROUT1	Gate drive output 1 for the primary side switch
15	VDD	IC Supply voltage
16	GND	Ground

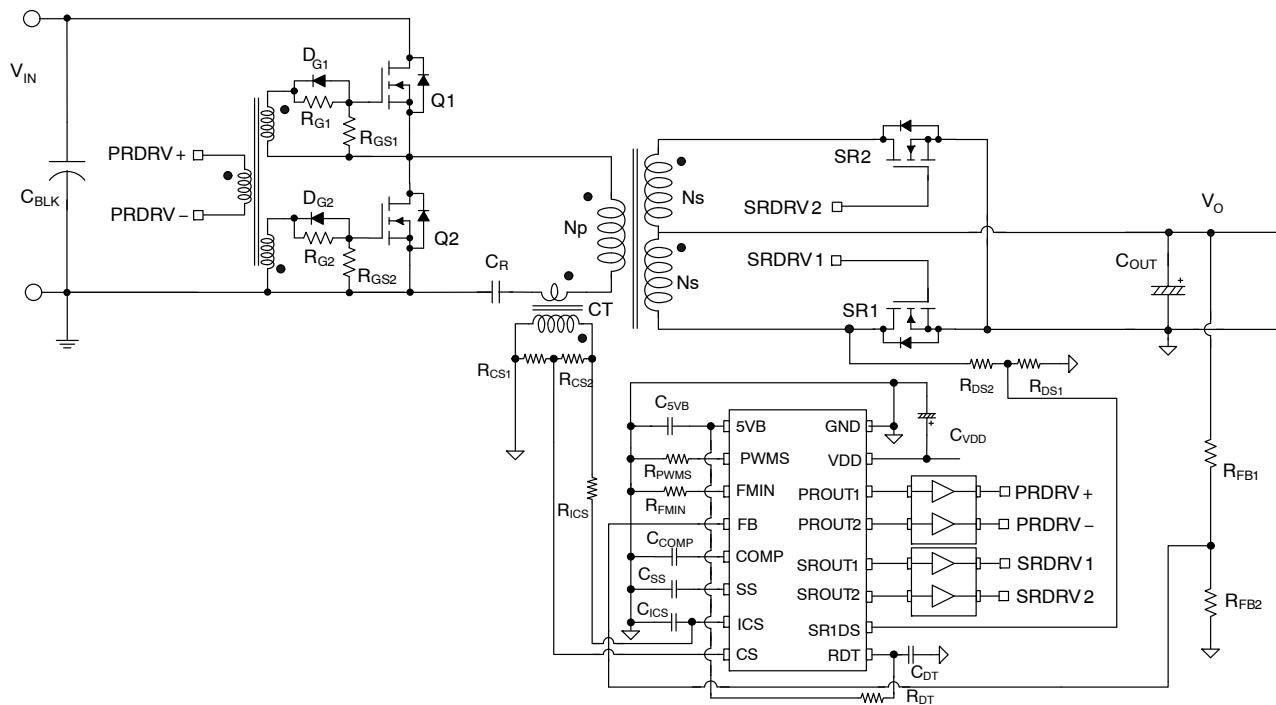


Figure 12. Schematic of Half-bridge LLC Resonant Converter

DESIGN PROCEDURE

This section presents a design procedure using the schematic in Figure 12 as a reference where the resonant inductor is implemented using leakage inductance. The design specifications are as follows:

- Nominal input voltage: 396 V_{DC} (output of PFC stage)
- Output: 24 V/12 A (288 W)
- Hold-up time requirement: 20 ms
- DC link capacitor of PFC output: 330 μ F

[STEP-1] Define the System Specifications

As a first step, define the following specification.

Estimated efficiency (E_{ff}): Estimate a power-conversion efficiency to calculate the maximum input power with given maximum output power. With the estimated efficiency, the maximum input power is:

$$P_{IN} = \frac{P_{OUT}}{E_{ff}} \quad (\text{eq. 11})$$

Input-voltage range: The maximum input voltage would be the nominal PFC output voltage.

$$V_{IN}^{max} = V_{O,PFC} \quad (\text{eq. 12})$$

Even though a PFC pre-regulator regulates the input voltage, it drops during the hold-up time. The minimum input voltage during the required hold-up time is:

$$V_{IN}^{min} = \sqrt{V_{O,PFC}^2 - \frac{2P_{IN}T_{HLD}}{C_{BLK}}} \quad (\text{eq. 13})$$

where $V_{O,PFC}$ is the nominal PFC output voltage, T_{HLD} is a hold-up time, and C_{BLK} is the DC link bulk capacitor.

(Design Example)

Assuming the efficiency is 96%,

$$P_{IN} = \frac{P_{OUT}}{E_{ff}} = \frac{288}{0.96} = 300 \text{ W}$$

$$V_{IN}^{max} = V_{O,PFC} = 369 \text{ V}$$

With 20 ms holdup time, the minimum input voltage is obtained as

$$V_{IN}^{min} = \sqrt{V_{O,PFC}^2 - \frac{2P_{IN}T_{HLD}}{C_{BLK}}} = 347 \text{ V}$$

For more margin, minimum input voltage is set to 300 V.

[STEP-2] Determine the Voltage Gain Range of the Resonant Network

Once the minimum and maximum input voltages to the LLC resonant converter are determined, we can determine the minimum and maximum gain of the LLC converter.

The minimum gain is required for the nominal input voltage. To minimize the switching frequency variation, it is typical to operate the LLC resonant converter around the resonant frequency. The voltage gain at the resonant frequency is:

$$M_V = \frac{2nV_O}{V_{IN}} \Big|_{f_{sw}=f_o} = \sqrt{\frac{m}{m-1}} \quad (\text{eq. 14})$$

During the holdup time, the PFC output voltage (input voltage of LLC resonant converter) drops, and a higher gain is required to regulate the output voltage. The maximum voltage gain is:

$$M_{\max} = \frac{V_{IN}^{\max}}{V_{IN}^{\min}} M_{\min} \quad (eq. 15)$$

We can attain a higher peak gain with a smaller m value; however, too small m value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set m around 3~7.

(Design Example)

The ratio (m) between L_p and L_r is chosen as 5.69. The minimum gain is obtained as:

$$M_{@f_0} = \sqrt{\frac{m}{m-1}} = \sqrt{\frac{5.69}{5.69-1}} = 1.10$$

The minimum gain at the maximum input voltage is selected as 1.13. Then, the maximum gain for minimum input voltage is obtained as

$$M_{\max} = \frac{V_{IN}^{\max}}{V_{IN}^{\min}} M_{\min} = \frac{396}{300} \times 1.13 = 1.49$$

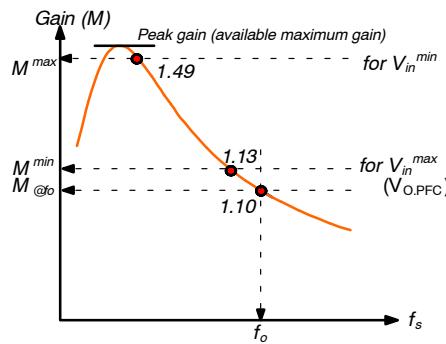


Figure 13. Maximum Gain / Minimum Gain

[STEP-3] Determine the Transformer Turns Ratio ($n = N_p / N_s$)

With the minimum gain (M_{\min}) obtained in STEP-2, we can calculate the transformer turns ratio as:

$$n = \frac{N_p}{N_s} = \frac{V_{IN}^{\max}}{2(V_o + V_F)} \times M_{\min} \quad (eq. 16)$$

where V_F is the secondary-side rectifier diode voltage drop.

(Design Example)

Since SR is used in the output rectifier, V_F is assumed to be 0 V for the SR MOSFET having low $R_{DS,ON}$. Thus, the transformer turns ratio is obtained as

$$n = \frac{N_p}{N_s} = \frac{V_{IN}^{\max}}{2(V_o + V_F)} \times M_{\min} = 9.33$$

[STEP-4] Calculate the Equivalent Load Resistance

With the transformer turns ratio obtained from equation (16), we calculate the equivalent load resistance.

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} \frac{1}{M_V^2} \quad (eq. 17)$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} \frac{1}{M_V^2} = 116 \Omega$$

[STEP-5] Design the Resonant Network

With m value chosen in STEP-2, read proper Q value from the peak gain curves in Figure 10 that allows the required maximum gain. Since the peak gain curve is generated using fundamental approximation, the actual gain at below resonance is about 10~15% higher than that of the prediction using fundamental approximation.

Once the Q value is determined, we can obtain the resonant components as follows:

$$C_r = \frac{1}{2\pi Q \times f_o \times R_{ac}} \quad (eq. 18)$$

$$L_r = \frac{1}{(2\pi f_o)^2 \times C_r} \quad (eq. 19)$$

$$L_p = m \times L_r \quad (eq. 20)$$

(Design Example)

As calculated in STEP-2, M_{\max} is 1.49. The m value has been chosen as 5.69 in STEP-2 and maximum Q is obtained as 0.37 from the peak gain curves in Figure 14.

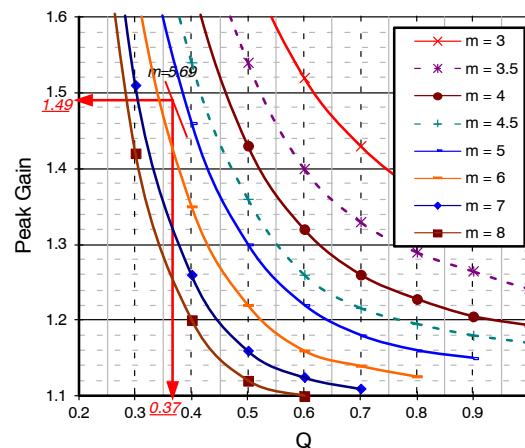


Figure 14. Resonant Network Design Using the Peak Gain (Attainable Maximum Gain)

By selecting the resonant frequency as 95 kHz, the resonant components are determined as:

$$C_r = \frac{1}{2\pi Q \times f_o \times R_{ac}} = 38.9 \text{ nF}$$

$$L_r = \frac{1}{(2\pi f_o)^2 \times C_r} = 72 \mu\text{H}$$

$$L_p = m \times L_r = 410 \mu\text{H}$$

When building the transformer, the actual parameters are adjusted as below to accommodate the standard components value as $C_r = 48 \text{ nF}$, $L_r = 58 \mu\text{H}$, $L_p = 330 \mu\text{H}$ and $f_o = 95 \text{ kHz}$.

The gain curve of final resonant network design using fundamental approximation is as below.

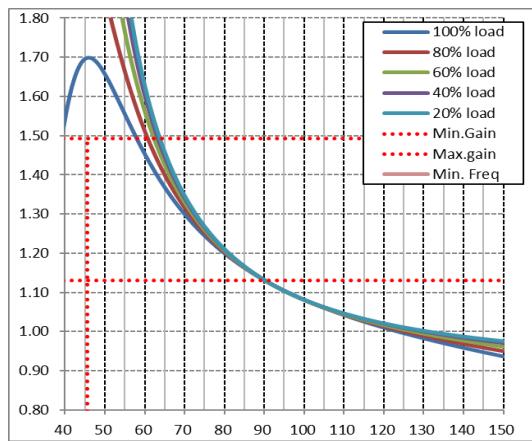


Figure 15. Gain Curve of the Design Example

Since the fundamental approximation yields lower peak gain than actual peak gain by 10~15% at below resonance operation, SIMPLIS simulation has been conducted to check the actual gain. The simulation results show that required maximum gain is obtained for 300 V input at 75 kHz. The simulation result also shows that the switching frequency at the nominal input voltage and full load condition is 105 kHz.

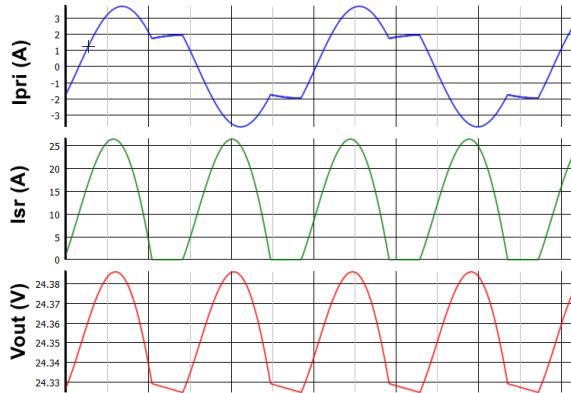


Figure 16. Simulation for $V_{in} = 300 \text{ V}$, $f_s = 69.55 \text{ kHz}$, $P_o = 288 \text{ W}$

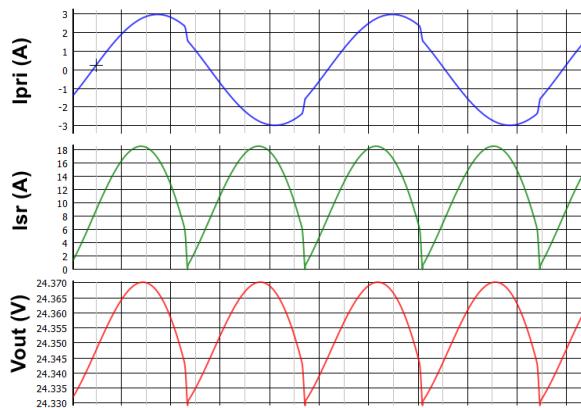


Figure 17. Simulation for $V_{in} = 396 \text{ V}$, $f_s = 105 \text{ kHz}$, $P_o = 288 \text{ W}$

[STEP-6] Design the Transformer

Figure 18 shows the magnetizing current of the transformer in the LLC resonant converter. The required minimum number of turns of the primary side winding to limit a maximum flux density B_{max} is obtained as:

$$N_p^{\min} = \frac{n(V_o + V_F)}{4f_0 \times M_V \times B_{max} \times A_e} \quad (\text{eq. 21})$$

where A_e is the cross-sectional area of the transformer core in m^2 , and B_{max} is the maximum flux density swing in Tesla, as shown in Figure 18. If there is no reference data, use $B_{max} = 0.2\text{--}0.3 \text{ T}$ to reduce the core loss. Notice that the virtual gain M_V , which is caused by the secondary-side leakage inductance (refer to Figure 7), appears in the equation.

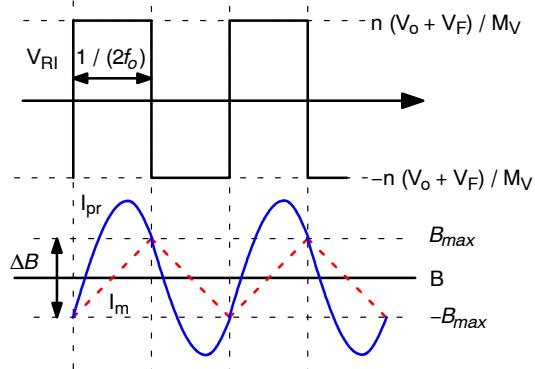


Figure 18. Flux Density Swing

Choose a proper number of turns for the secondary side resulting in a primary-side turn number higher than N_p^{\min} .

$$N_p = n \times N_S > N_p^{\min} \quad (\text{eq. 22})$$

The wire gauge of primary and secondary side winding should be determined based on the RMS currents at nominal input voltage, which are given as

$$I_{PR}^{\text{RMS}} \cong \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n} \right]^2 + \left[\frac{n(V_o + V_F)}{4\sqrt{2} f_0 M_V (L_p - L_r)} \right]^2} \quad (\text{eq. 23})$$

$$I_{SEC}^{\text{RMS}} = \frac{\pi I_o}{4} \text{ (each winding)} \quad (\text{eq. 24})$$

(Design Example)

SRV5018 core ($A_e = 189.2 \text{ mm}^2$) is selected for the transformer. B_{max} is selected as 0.1 T to reduce the core loss of the transformer. The minimum primary-side turn number of the transformer is

$$N_p^{\min} = \frac{n(V_o + V_F)}{4f_0 \times M_V \times B_{max} \times A_e} = 28.1 \text{ turns}$$

$$N_p = n \times N_S = 9.32 \times 3 = 27.96 \approx N_p^{\min}$$

N_S is chosen as 3; N_p is selected as 28.

The RMS currents of the transformer windings at nominal input voltage are obtained as

$$I_{PR}^{RMS} \cong \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n} \right]^2 + \left[\frac{n(V_o + V_F)}{4\sqrt{2} f_o M_V (L_p - L_r)} \right]^2} = 1.99 \text{ A}$$

$$I_{SEC}^{RMS} = \frac{\pi I_o}{4} = 9.42 \text{ A}$$

[STEP-7] Select the Resonant Capacitor

Figure 19 shows the primary side current (resonant capacitor current) waveforms for different operating conditions. When choosing the resonant capacitor, one should consider the current rating because a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor at nominal input voltage has been obtained in equation (23).

The maximum resonant capacitor voltage at nominal input voltage and nominal load condition is given as

$$V_{CR,NRM}^{max} \cong \frac{V_{IN}^{max}}{2} + \frac{I_o}{4f_{SW} \times n \times C_R} \quad (\text{eq. 25})$$

The voltage rating of the resonant capacitor should be determined based on the maximum voltage for each corner condition.

The maximum resonant capacitor voltage at nominal input voltage and output overcurrent condition is given as

$$V_{CR,OCP}^{max} \cong \frac{V_{IN}^{max}}{2} + \frac{I_{O,OCP}}{4f_{SW}n \times C_R} \quad (\text{eq. 26})$$

The maximum resonant capacitor voltage at minimum input voltage and nominal load condition is given as

$$V_{CR,NRM\ MIN}^{max} \cong \frac{V_{IN}^{min}}{2} + \left[\frac{I_o}{4f_{SW}n} + n \frac{(V_o + V_F)}{4M_V L_m f_o} \left(\frac{1}{2f_{SW}} - \frac{1}{2f_o} \right) \right] \frac{1}{C_R} \quad (\text{eq. 27})$$

Note that the $V_{IN}/2$ term in equation (25) – (27) should be deleted for the full-bridge LLC case.

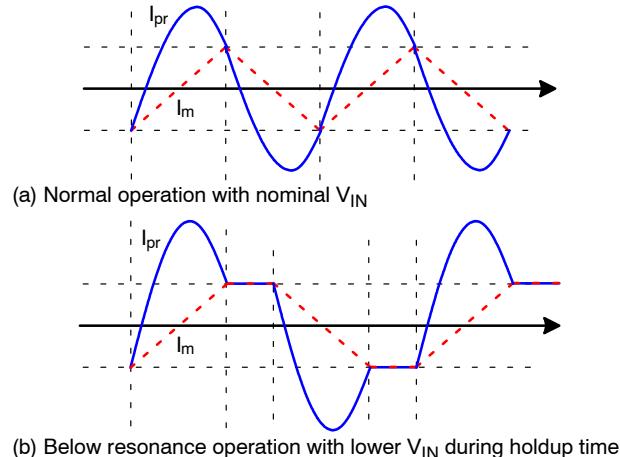


Figure 19. Primary Side Current Waveform of LLC Resonant Converter for Different Operation Modes

(Design Example)

In STEP-6, the RMS current of the resonant capacitor is calculated as

$$I_{PR}^{RMS} = 1.99 \text{ A}$$

The maximum resonant capacitor voltage at nominal input voltage and nominal load condition is obtained as

$$V_{CR,NRM}^{max} \cong \frac{V_{IN}^{max}}{2} + \frac{I_o}{4f_{SW}n \times C_R} = 261.8 \text{ V}$$

By setting the OCP level at 13 A, the maximum resonant capacitor voltage at nominal input voltage and output overcurrent condition is obtained as

$$V_{CR,OCP}^{max} \cong \frac{V_{IN}^{max}}{2} + \frac{I_{O,OCP}}{4f_{SW}n \times C_R} = 267 \text{ V}$$

By setting the minimum frequency as 65 kHz, the maximum resonant capacitor voltage at minimum input voltage and nominal load condition is given as

$$V_{CR}^{max} \cong \frac{V_{IN}^{min}}{2} + \left[\frac{I_o}{4f_{SW}n} + n \frac{(V_o + V_F)}{4M_V L_m f_o} \left(\frac{1}{2f_{SW}} - \frac{1}{2f_o} \right) \right] \frac{1}{C_R} = 361.6 \text{ V}$$

[STEP-8] Rectifier Network Design

When the center tap winding is used in the transformer secondary side, the diode voltage stress is twice of the output voltage.

$$V_D = 2(V_o + V_F) \quad (\text{eq. 28})$$

The RMS value of the current flowing through each rectifier diode is given as:

$$I_D^{RMS} = \frac{\pi}{4} I_o \quad (\text{eq. 29})$$

Meanwhile, the ripple current flowing through the output capacitor is given as:

$$I_{CO}^{RMS} = \sqrt{\left(\frac{\pi I_o}{2\sqrt{2}} \right)^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o \quad (\text{eq. 30})$$

The voltage ripple on the output capacitor is

$$\Delta V_O \cong \frac{\pi}{2} I_o \times R_C + \frac{\frac{\pi}{2} I_o}{f_{SW} C_O} \times 0.067 \quad (\text{eq. 31})$$

where R_C is the effective series resistance (ESR) of the output capacitor.

(Design Example)

The voltage stress and current stress of the rectifier diode are:

$$V_D = 2(V_o + V_F) = 48 \text{ V}$$

$$I_D^{RMS} = \frac{\pi}{4} I_o = 9.42 \text{ A}$$

The 75 V–4.5 mΩ POWERTRENCH® MOSFETs are selected for the synchronous rectifier considering the

voltage overshoot caused by the stray inductance. Conduction loss on each MOSFET is 0.47 W.

The RMS current of the output capacitor is:

$$I_{Co \text{ RMS}} = \sqrt{\left(\frac{\pi I_o}{2\sqrt{2}}\right)^2 - I_o^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o = 5.8 \text{ A}$$

Four 1200 μF capacitors are used in parallel for the output capacitor. The current rating and ESR for each capacitor is 2.77 A_{RMS} and 15 m Ω .

The output capacitor ripple is calculated as

$$\Delta V_O \approx \frac{\pi}{2} I_o \times R_C + \frac{\pi I_o}{f_{SW} C_O} \times 0.067 = 73.44 \text{ mV}$$

[STEP-9] Current Sensing Circuit Configuration

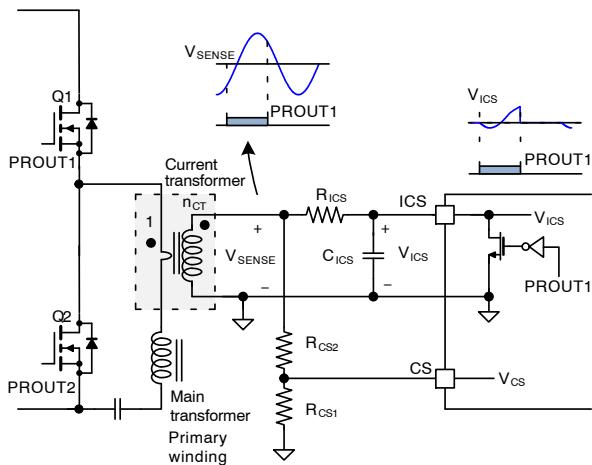


Figure 20. Typical Current Sensing Configuration

NCP4390 senses both instantaneous switch current and the integral of the switch current, as illustrated in Figure 20. Since NCP4390 is located in the secondary side, a current transformer is used for sensing the primary-side current. While the PROUT1 is LOW, an internal reset switch clamps the ICS-pin voltage at 0 V. Conversely, while PROUT1 is high, the ICS pin is not clamped, and the integral capacitor (C_{ICS}) is charged and discharged by the current flowing through R_{ICS} resistor.

Application circuit of NCP4390 does a quasi-integral using an RC filter. To obtain accurate integral, the current sensing resistor and current-transformer turn ratio should be designed such that the amplitude of V_{SENSE} is higher than V_{ICS} for most of the time. Figure 23 shows how the error of the quasi-integral circuit varies with the ratio between V_{ICS} peak voltage and V_{SENSE} at the falling edge of PROUT1 (V_{CM}). As the ratio being smaller, the more accurate the integral can be.

When the ratio between V_{ICS} peak voltage and V_{CM} is smaller than 0.5, quasi-integral with acceptable error (about 10%) is obtained. Since V_{ICS} peak voltage is below 1.2 V in normal operation, we should select R_{CS1} and R_{CS2} such that V_{CM} is higher than 2.4 V.

$$V_{CM} = \frac{n(V_O + V_F)}{M_V(L_p - L_r)} \times \frac{1}{4f_O} \times \frac{R_{CS1} + R_{CS2}}{n_{CT}} > 2.4 \text{ V} \quad (\text{eq. 32})$$

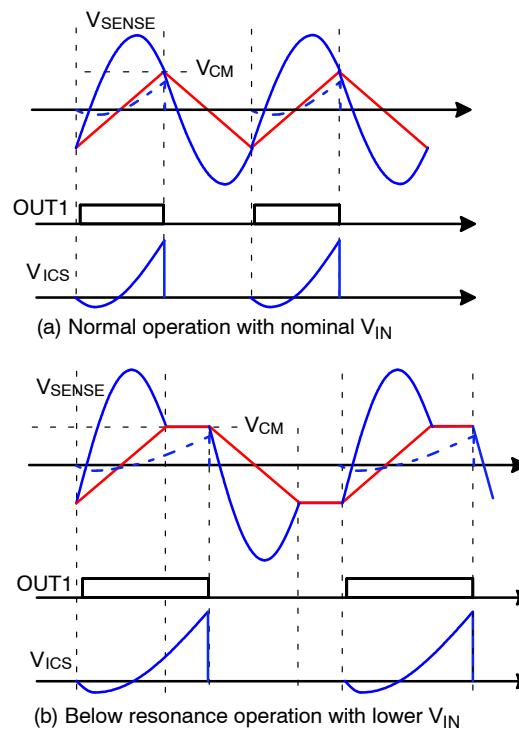


Figure 21. ICS Pin Waveforms

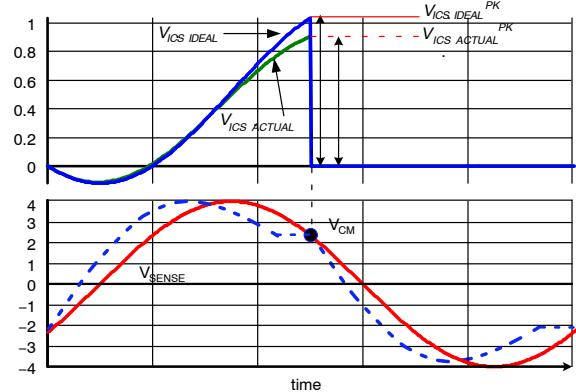


Figure 22. Definition of $V_{ICS,IDEAL}^{PK}$ and $V_{ICS,ACTUAL}^{PK}$

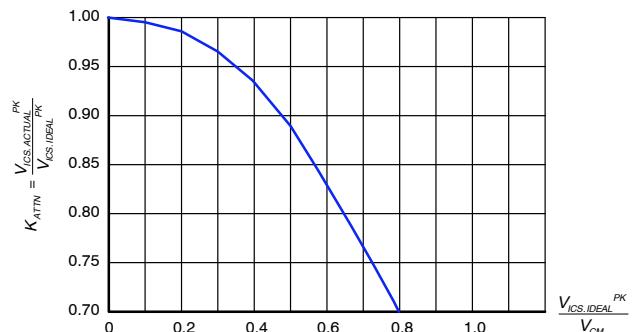


Figure 23. ICS Pin Voltage Attenuation vs. $V_{ICS,IDEAL}^{PK}/V_{CM}$

To obtain peak voltage of V_{ICS} , let's see the ideal input power of the LLC converter. With topology of half-bridge LLC and defining PROUT1 turn-on moment as $t = 0$, the input power can be described as

$$P_{IN} = f_{SW} \times V_{IN} \times \int_0^{1/2 f_{SW}} I_{PR}(t) dt \quad (\text{eq. 33})$$

Note that the right-hand side of the equal sign should be multiplied by 2 for the full-bridge LLC case.

Assuming an ideal integral, the peak voltage of ICS can be described as

$$V_{ICS\ PK} = \frac{R_{CS1} + R_{CS2}}{n_{CT} \times R_{ICS} \times C_{ICS}} \int_0^{1/2 f_{SW}} I_{PR}(t) dt \quad (\text{eq. 34})$$

Combining (33) and (34), the ICS peak voltage can be estimated as

$$V_{ICS\ PK} = \frac{R_{CS1} + R_{CS2}}{n_{CT} \times R_{ICS} \times C_{ICS}} \times \frac{P_{IN}}{f_{SW} \times V_{IN}} \quad (\text{eq. 35})$$

Considering capability of the internal discharge switch of the ICS pin, the typical value of C_{ICS} is 1 nF. For accurate integral, we recommend a 1% tolerance capacitor.

When the ratio between V_{ICS} peak voltage and V_{CM} is not smaller enough, apply the attenuation factor in Figure 23 to equations (35).

The peak value of the integral of the current sensing voltage (V_{ICS}) is proportional to the average input current of the LLC resonant converter in the switching cycle, as shown in Figure 24. Therefore, the load condition for SR enable/disable is determined as a percentage of full load condition according to the percentage of nominal power corresponding to the input current limit threshold. Typically, 120% of nominal load condition is used for the overcurrent trip point, and the SR is enabled and disabled at 15% and 7.5% of nominal load respectively. If it is 140% of the nominal load condition for the overcurrent trip point, the SR will enable and disable at 17.5% and 8.75% of the nominal load.

To obtain a higher overcurrent limit without increasing SR enable/disable points, an additional slope on V_{ICS} can be applied through a resistor R_{SLP} between ICS and 5VB pins. This technique is typically used for longer holdup time. With a given R_{SLP} , the additional slope added to ICS pin voltage is given as

$$V_{ICS,SLP} = \frac{5}{R_{SLP}C_{ICS}} \times \frac{1}{2 \times f_{SW}} \quad (\text{eq. 36})$$

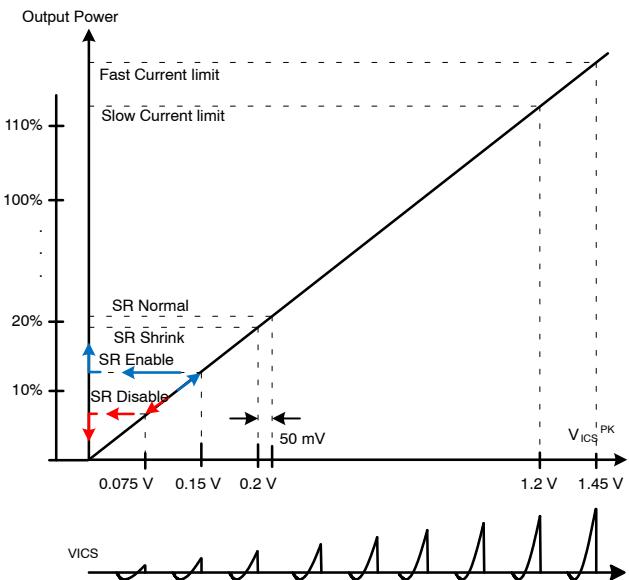


Figure 24. Load Condition and ICS Pin Voltage

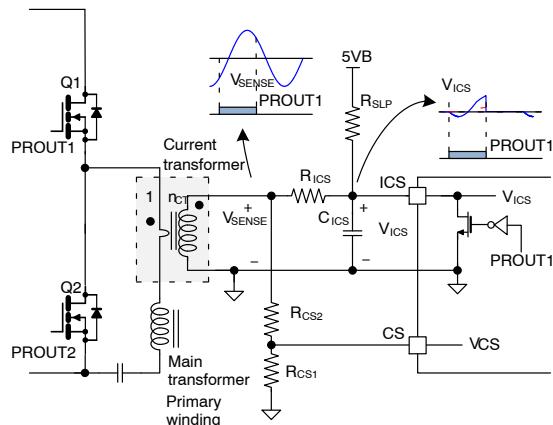


Figure 25. Current Sensing Configuration with Slope Compensation

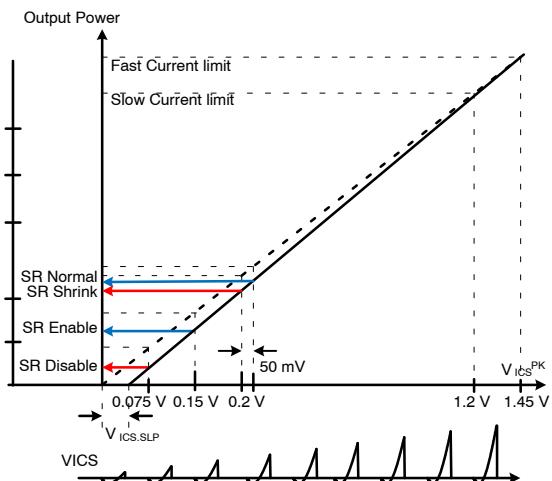


Figure 26. Load Condition and ICS Pin Voltage when Slope Compensation is Added

The peak value of primary-side current at nominal input voltage and full load is estimated as

$$I_{PR}^{PK} \cong \sqrt{2} \times I_{PR}^{RMS} \quad (\text{eq. 37})$$

The ratio between R_{CS1} and R_{CS2} is decided according to the primary-side overcurrent protection (OCP) trip point, which should be smaller than I_{PR}^{PK} .

$$I_{PR,OCP} \times \frac{R_{CS1}}{n_{CT}} = 3.5 \text{ V} \quad (\text{eq. 38})$$

(Design Example)

With a current transformer with a turns ratio of 44 (n_{CT}), the recommended minimum value of the sum of R_{CS1} and R_{CS2} is given as

$$R_{CS1} + R_{CS2} > \frac{2.4 \times M_V (L_p - L_r) \times 4f_O n_{CT}}{n (V_O + V_F)} = 54 \Omega$$

As power consumption does not go too high, it is okay to set $R_{CS1} + R_{CS2}$ higher to have ideal integral on V_{ICS} . Thus, we select sum of R_{CS1} and R_{CS2} to be 230Ω .

The peak of primary side current at nominal input voltage and full load condition is given as

$$I_{PR}^{PK} \cong \sqrt{2} \times I_{PR}^{RMS} = 2.94 \text{ A}$$

By setting the primary side OCP level at 5 A,

$$R_{CS1} = 3.5 \text{ V} \times \frac{n_{CT}}{I_{PR,OCP}} = 30.8 \Omega$$

R_{CS1} and R_{CS2} are selected as 30 and 200Ω .

This design does not apply additional slope on ICS pin.

Select 1 nF capacitor as C_{ICS} . Assuming the attenuation factor of V_{ICS} at 1.2 V is 1.0 (reading from Figure 23 at $x = 1.2 / 10.23$), the proper R_{ICS} resistor to have 13 A over-load protection ($I_{O,OLP}$) at nominal input voltage is

$$R_{ICS} = \frac{V_O \times I_{O,OLP} \times (R_{CS} + R_{CS2})}{E_{ff} \times V_{IN} \times f_{SW} \times n_{CT} \times C_{ICS} \times 1.2} = 33.1 \text{ k}\Omega$$

Select 30 k Ω as R_{ICS} .

[STEP-10] Soft-Start Capacitor

The soft-start time can be programmed using a soft-start capacitor as follows.

$$T_{SS} = \frac{C_{SS} \times 2.4 \text{ V}}{I_{SS}} \quad (\text{eq. 39})$$

Too short soft-start time forces the LLC resonant converter to draw too much current from the input voltage, resulting in overload protection during startup. Therefore, the soft-start time should be well-matched with the available rising time of the output capacitor as

$$T_{SS} = \frac{C_{SS} \times 2.4 \text{ V}}{I_{SS}} > \frac{C_{OUT} \times V_O}{I_{O,OLP} - I_O} \quad (\text{eq. 40})$$

(Design Example)

The output capacitor is $4800 \mu\text{F}$ in total. Assume maximum output current during start-up is 10 A. Then, the minimum soft-start time should be

$$\frac{C_{OUT} \times V_O}{I_{O,OLP} - I_O} = 38.4 \text{ ms}$$

By selecting 60 ms soft-start time, the soft-start capacitor is obtained as

$$C_{SS} = \frac{T_{SS} \times I_{SS}}{2.4} = 1000 \text{ nF}$$

[STEP-11] Minimum Frequency Setting

The minimum switching frequency is limited by comparing a timing-capacitor voltage (V_{CT}) with an internal 3 V reference, as shown in Figure 27. A resistor R_{FMIN} connected to the FMIN pin determines the rising slope of V_{CT} . Thus, the minimum switching frequency is

$$f_{SW,MIN} \cong 100 \text{ kHz} \times \frac{10 \text{ k}\Omega}{R_{FMIN}} \quad (\text{eq. 41})$$

A digital counter also limits the minimum switching frequency. Since a 10 bit counter with a 40 MHz clock is used in NCP4390, the minimum switching frequency cannot be lower than 39 kHz ($40 \text{ MHz} / 1024 = 39 \text{ kHz}$). Therefore, the maximum usable value for R_{FMIN} is $25.5 \text{ k}\Omega$.

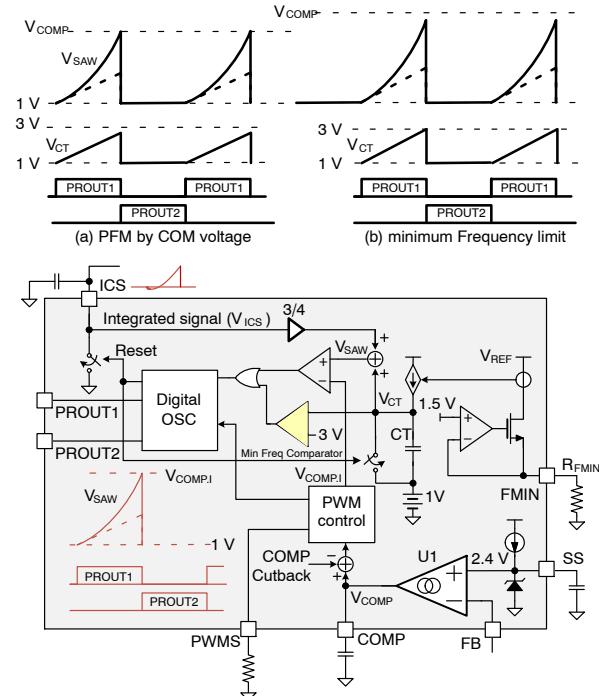


Figure 27. Minimum Switching Frequency Setting

(Design Example)

The frequency at minimum input voltage and full load condition is 69.4 kHz by SIMPLIS simulation result in [STEP-5]. Leaving some margin, 65 kHz is selected as minimum frequency. Then, the R_{FMIN} is obtained as

$$R_{FMIN} = 100 \text{ kHz} \times \frac{10 \text{ k}\Omega}{f_{SW,MIN}} = 15.4 \text{ k}\Omega$$

15 k Ω standard resistor value is selected for the final design.

If higher switching frequency is wanted during soft start, here is a little trick. Add a capacitor on FMIN pin with a series resistor to adjust a time constant, in parallel with the original R_{FMIN} . Once the V_{DD} reaches $V_{DD.ON}$ (10 V), internal bias on FMIN pin will be turned on. Due to charging the additional capacitor, current flowing out of FMIN pin becomes higher during the bias-building-up phase. It makes slope of V_{CT} signal sharper and switching frequency higher temporarily.

[STEP-12] PWM Mode Entry Level Setting

NCP4390 employs a hybrid-control mechanism where the PFM switches to pulse width modulation (PWM) mode at light load, as illustrated in Figure 28. When the error-amplifier output voltage (V_{COMP}) is below a PWM-mode threshold ($V_{COMP.PWM}$), the internal COMP signal is clamped at the threshold level, and the PFM operation switches to PWM mode.

In PWM mode, the difference between $V_{COMP.PWM}$ and V_{COMP} accompanying with V_{CT} signal determines the turning-on of PROUT1. Thus, the duty cycle decreases as V_{COMP} drops. $V_{COMP.PWM}$ also limits the switching frequency in PWM-mode and skip-mode operation.

$$f_{SW.PWM} \approx \frac{2}{V_{COMP.PWM} - 1} \times f_{MIN} \quad (\text{eq. 42})$$

The $V_{COMP.PWM}$ can be programmed through a resistor on the PWMS pin. By setting $V_{COMP.PWM}$ lower, switching frequency in PWM and skip-mode operations becomes higher. Refer to Figure 30 for the respective R_{PWMS} value for setting $V_{COMP.PWM}$.

Also, note that PWM mode disables SR operation.

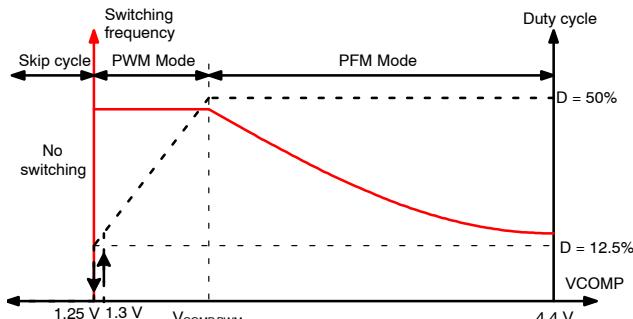


Figure 28. Mode Change with COMP Voltage

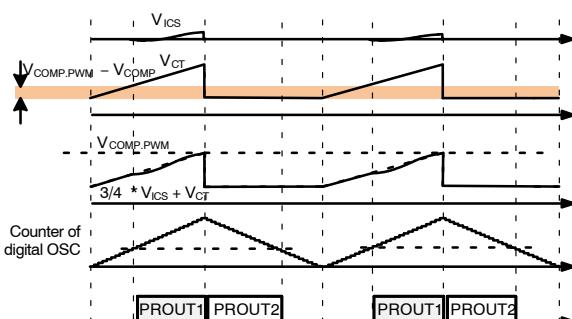


Figure 29. PWM-mode Operation ($V_{COMP} < V_{COMP.PWM}$)

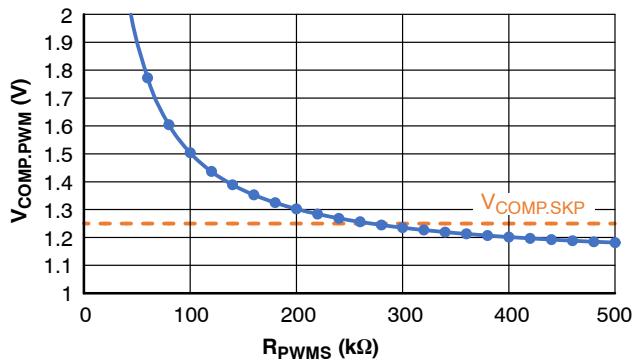


Figure 30. PWM-mode Entry-level Setting

(Design Example)

With $V_{COMP.PWM} = 1.48$ V, the switching frequency at PWM mode is given as

$$f_{SW.PWM} \approx \frac{2}{V_{COMP.PWM} - 1} \times f_{MIN} = 272 \text{ kHz}$$

R_{PWMS} is selected as 100 kΩ.

[STEP-13] Dead Time Setting

With a single pin (RDT pin), the dead times between the primary-side gate-drive signals (PROUT1 and PROUT2) and of the secondary-side SR gate-drive signal (SROUT1 and SROUT2) are programmed using a switched current source as shown in Figure 31 and Figure 32.

Once the 5 V bias on the 5VB pin enables, the RDT pin voltage is pulled up. When the RDT pin voltage reaches 1.4 V, the voltage across C_{DT} is discharged down to 1 V by an internal current source I_{DT} . Then, I_{DT} disables and the RDT resistor pulls up the RDT-pin voltage again. As highlighted in Figure 32, 1/64 of the time required (T_{SET1}) for RDT pin voltage to rise from 1 V to 3 V determines the dead time of secondary-side SR gate-drive signals.

The switched current source I_{DT} then enables again to discharge the RDT pin voltage. 1/32 of the time required (T_{SET2}) for the RDT pin voltage to drop from 3 V to 1 V determines the dead time between the primary-side gate drive signals. After the RDT voltage drops to 1 V, the current source I_{DT} disables again, allowing the RDT voltage to be charged up to 5 V.

Table 2 shows the dead times for SROUT and PROUT programmed with recommended R_{DT} and C_{DT} component values. Since the time is memorized through an internal 40 MHz clock signal, the resolution of the dead-time setting is 25 ns. The minimum and maximum dead times are therefore limited at 75 ns and 375 ns, respectively. To assure stable SR operation while taking circuit parameter tolerance into account, less than 75 ns of SR dead time is not recommended.

The required dead time for the primary-side MOSFETs can be obtained as

$$T_{D,PROUT} > \frac{V_{IN}^{max} \times 2C_{OSS}}{I_{CM}} \quad (eq. 43)$$

where C_{OSS} is an effective output capacitance of primary-side MOSFET, and I_{CM} is the peak of magnetizing current. I_{CM} can be calculated as:

$$I_{CM} = \frac{N_p}{N_s} \frac{V_O + V_F}{(L_p - L_r)} \frac{1}{4f_{SW}} \quad (eq. 44)$$

The f_{SW} in equation (44) is usually f_o in below-resonant designs. It is beyond f_o for above-resonant designs based on resonant-component design and required voltage gain M^{min} .

NCP4390 can have $f_{SW,PWM}$ PFM operation at the boundary before leaving skip-mode. When $V_{COMP,PWM}$ is set lower, switching frequency at the boundary becomes higher. This condition may lead to excessive switching loss. When that happens, consider applying the $f_{SW,PWM}$ from equation (42) as f_{SW} in equation (44), or increasing $V_{COMP,PWM}$.

If remote-on function for the LLC converter is required, it is possible to disable NCP4390's operation by pulling RDT pin down to GND.

(Design Example)

The peak of magnetizing current is obtained as

$$I_{CM} = \frac{N_p}{N_s} \frac{V_O + V_F}{(L_p - L_r)} \frac{1}{4f_o} = 1.96 A$$

Assuming FCB199N65S3 is used in the primary side, the effective output capacitance is 277 pF. Then, the minimum dead time for the primary side MOSFETs is obtained as

$$T_{D,PROUT} > \frac{V_{IN}^{max} \times 2C_{OSS}}{I_{CM}} = 112 ns$$

According to STEP-12, maximum frequency set by PWMS is 272 kHz. The peak magnetizing current and the

minimum dead time at the boundary of PWM mode can be estimated as below.

$$I_{CM,PWM,Boundary} = \frac{N_p}{N_s} \frac{V_O + V_F}{(L_p - L_r)} \frac{1}{4f_{SW,PWM}} = 0.686 A$$

$$T_{D,PROUT} > \frac{V_{IN}^{max} \times 2C_{OSS}}{I_{CM,PWM,Boundary}} = 319 ns$$

To guarantee stable ZVS operation against load variation and stray capacitance, 325 ns dead time is selected for the primary side MOSFETs.

For the secondary side SR, 250 ns dead time is selected. By choosing $C_{DT} = 470$ pF, R_{DT} is chosen as 51 kΩ.

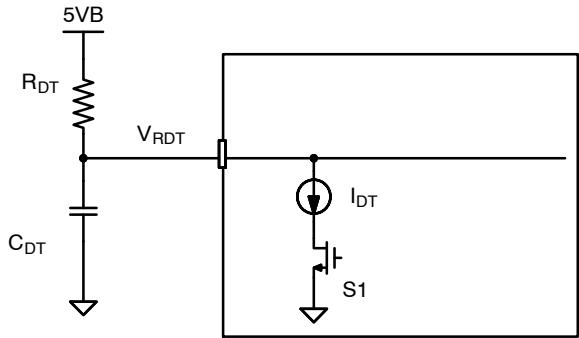


Figure 31. Internal Current Source for of RDT Pin

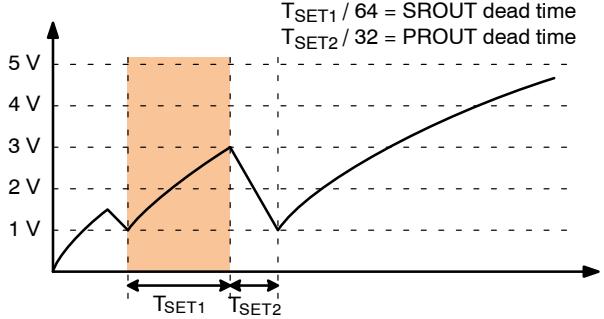


Figure 32. Multi-function Operation of RDT Pin

Table 2. DEAD TIME SETTING FOR SROUT AND SRROUT

	C _{DT} = 180 pF		C _{DT} = 220 pF		C _{DT} = 270 pF		C _{DT} = 330 pF		C _{DT} = 390 pF		C _{DT} = 470 pF		C _{DT} = 560 pF	
R _{DT}	SROUT DT (ns)	PROUT DT (ns)												
28 kΩ	75	375	75	375	75	375	100	375	125	375	150	375	175	375
30 kΩ	75	250	75	325	100	375	100	375	125	375	150	375	175	375
33 kΩ	75	200	75	250	100	300	125	375	150	375	175	375	200	375
36 kΩ	75	175	75	200	100	250	125	325	150	375	175	375	225	375
40 kΩ	75	150	100	175	125	225	150	275	175	325	200	375	250	375
44 kΩ	75	125	100	150	125	200	150	250	175	300	225	350	275	375
48 kΩ	100	125	125	150	150	175	175	225	200	275	250	325	300	375
53 kΩ	100	100	125	125	150	175	200	200	225	250	275	300	325	375
58 kΩ	125	100	150	125	175	150	200	200	250	250	300	300	350	350
64 kΩ	125	100	150	125	175	150	225	200	275	225	325	275	375	325
71 kΩ	150	100	175	125	200	150	250	175	300	225	350	250	375	325
78 kΩ	150	100	175	100	225	150	275	175	325	200	375	250	375	300
86 kΩ	175	75	200	100	250	125	300	175	375	200	375	250	375	300
94 kΩ	175	75	225	100	275	125	325	175	375	200	375	225	375	275
104 kΩ	200	75	250	100	300	125	375	150	375	200	375	225	375	275
114 kΩ	225	75	275	100	325	125	375	150	375	175	375	225	375	275
126 kΩ	250	75	300	100	375	125	375	150	375	175	375	225	375	275
138 kΩ	275	75	325	100	375	125	375	150	375	175	375	225	375	250
152 kΩ	300	75	350	100	375	125	375	150	375	175	375	225	375	250

[STEP-14] SR Drain Voltage Sensing

NCP4390 evaluates an SR conduction time for both SROUT using a single SR1DS pin. The chip compares the SR1DS voltage and its delayed replica, resulting from a 100 ns RC time-constant, as shown in Figure 33. When the SR is conducting, the SR1DS voltage clamps to either ground or the high voltage rail (2 times the output voltage divided by a voltage divider) as illustrated in Figure 34 and Figure 35. Whereas, SR1DS voltage changes fast when there is a switching transition. When both of the SR MOSFETs are turned off, the SR1DS voltage oscillates. When the SR1DS voltage changes faster than 0.25 V/100 ns on the rising edge and 0.2 V/100 ns on the falling edge, NCP4390 detects it as the switching transition of the SR conduction state. Based on the detected switching transition, NCP4390 predicts the SR current zero-crossing instant for the next switching cycle and turns off SROUT earlier according to the dead-time setting in STEP-13. NCP4390 also compensates the 100 ns detection delay caused by the

RC time constant through the internal timing detection circuit for a correct gate drive for SR.

Figure 34 and Figure 35 show the typical waveforms of SR1DS pin voltage together with other key waveforms. Since the voltage rating of SR1DS pin is 4 V, a voltage divider should be properly designed such that no excess voltage is applied to this pin.

$$R_{DS2} > \left(\frac{2V_O}{4} - 1 \right) \times R_{DS1} \quad (\text{eq. 45})$$

Additional bypass capacitor (C_{DS}) can be connected to the SR1DS pin to improve noise immunity. However, the equivalent time constant generated from the bypass capacitor and voltage divider resistors should be smaller than the internal RC time constant (100 ns) of the detection circuit for proper SR current zero-crossing detection.

$$C_{DS} < \frac{100 \text{ ns}}{(R_{DS1} || R_{DS2})} \quad (\text{eq. 46})$$

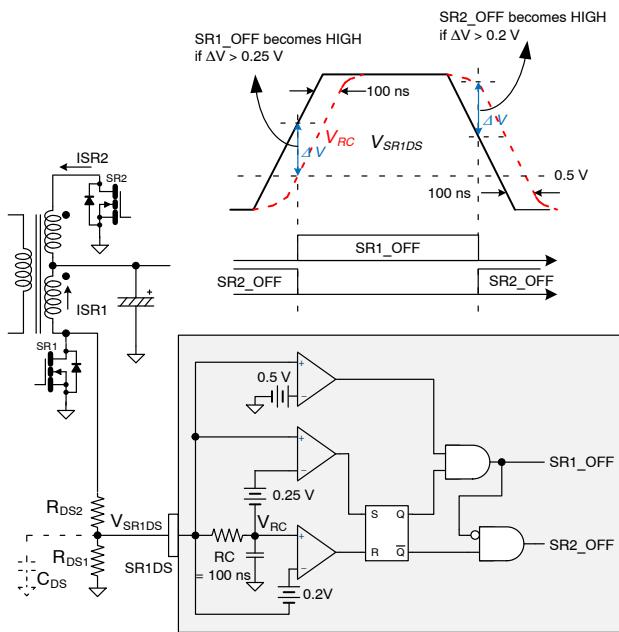


Figure 33. SR Conduction Detection with Single Pin (SR1DS Pin)

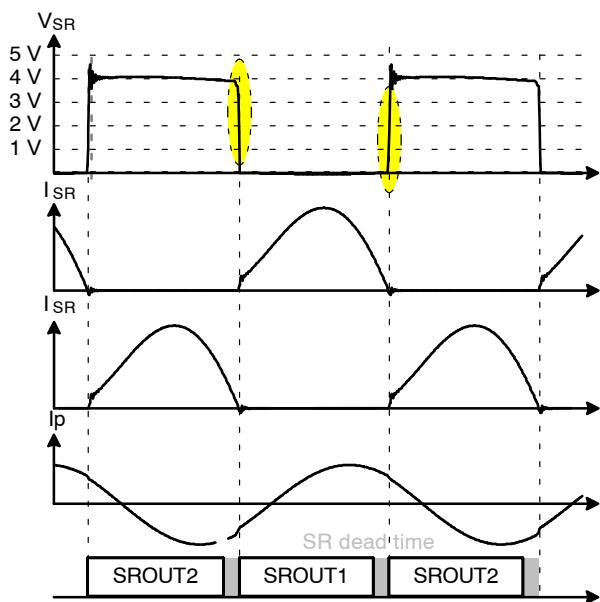


Figure 35. SR Conduction Detection Waveform at Above-resonant Operation

(Design Example)

By choosing $2.7\text{ k}\Omega$ for R_{DS1} , the minimum R_{DS2} is obtained as

$$R_{DS2} > \left(\frac{2V_O}{4} - 1\right) \times R_{DS1} = 29.7\text{ k}\Omega$$

After selecting $R_{DS2} = 30\text{ k}\Omega$, the maximum filter capacitance on C_{DS} is obtained as

$$C_{DS} < \frac{100\text{ ns}}{(R_{DS1} || R_{DS2})} = 40.37\text{ pF}$$

Thus, 20 pF is selected for C_{DS} .

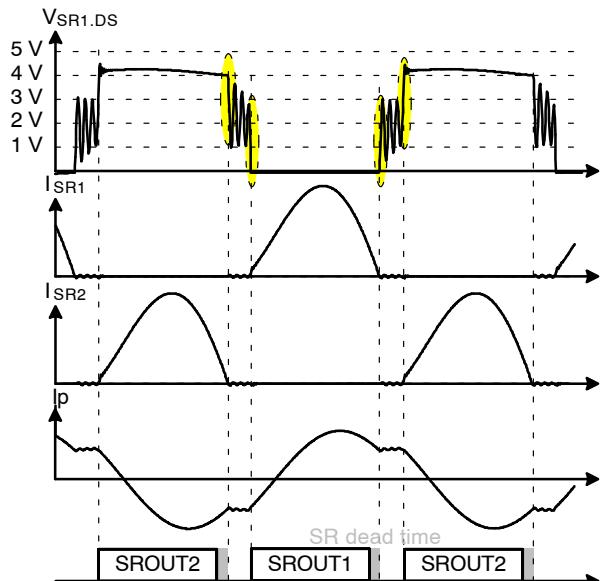


Figure 34. SR Conduction Detection Waveform at Below-resonant Operation

DESIGN SUMMARY

Figure 36 shows the final schematic of the design example. An SRV5018 core is used for the transformer and the resonant inductor is implemented using the leakage inductance.

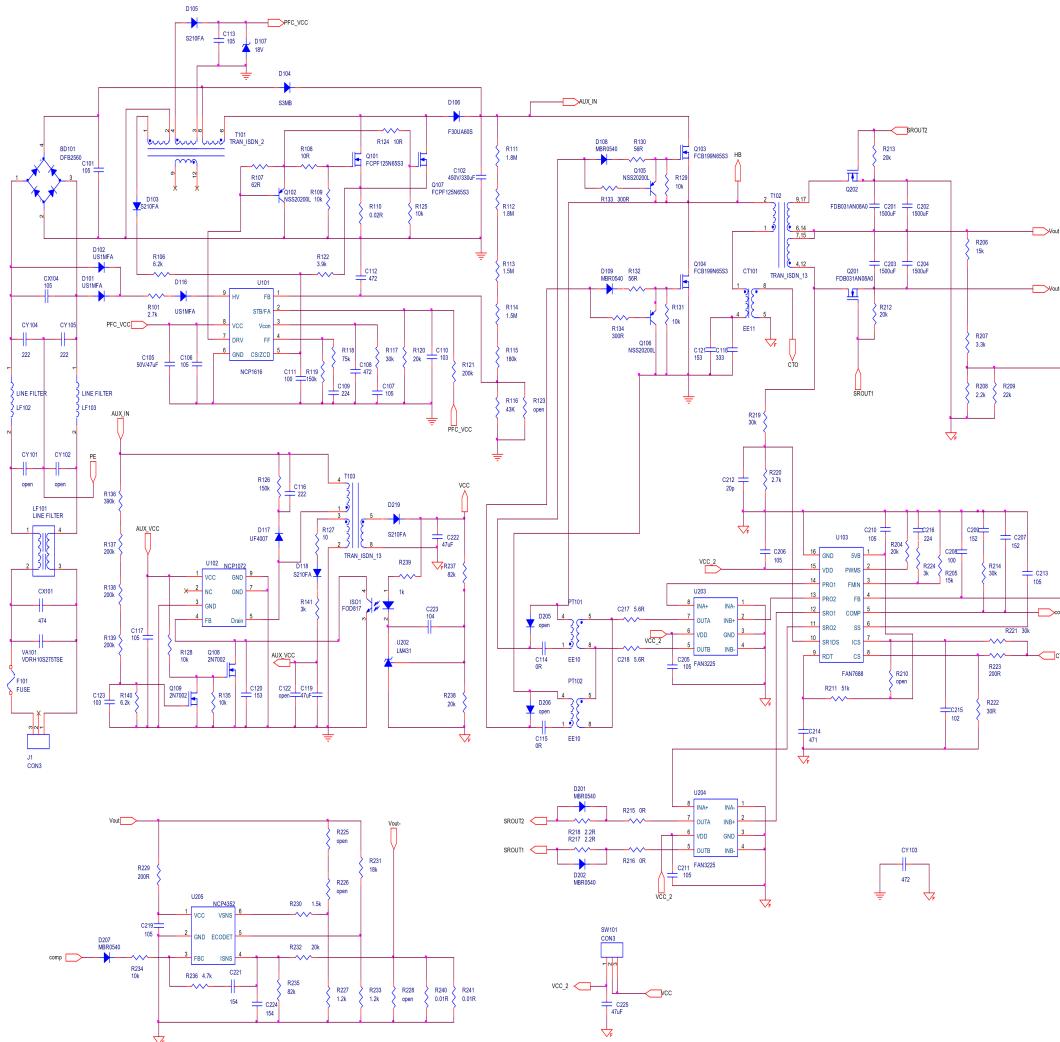


Figure 36. Final Schematic of Half-bridge LLC Resonant Converter Using NCP4390

AND90061/D

- Core & Bobbin: SRV5018 ($A_e = 189.2 \text{ mm}^2$)
- Primary Inductance : 330 mH
- Leakage Inductance: 58 μH

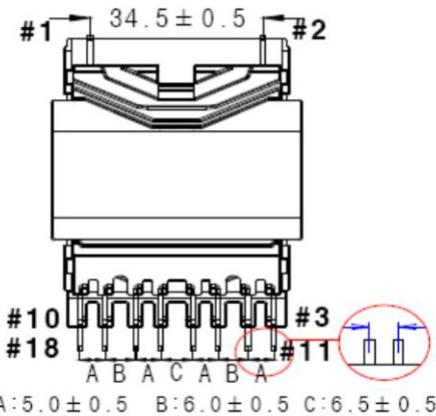


Figure 37. LLC Power Transformer (T1) in the Evaluation Board

Table 3. TRANSFORMER WINDING STRUCTURE

	Pin (Start → Finish)	Wire	Turns	Winding Method	Barrier Tape		
					TOP	BOT	Ts
N _p	1 → 2	0.1φ x 60 USTC	28	Solenoid winding	-	-	-
Insulation: Polyester Tape, t = 0.025 mm, 2 Layers							
N _s	4 → 7 12 → 15	0.10φ x 150 USTC	3	Bifilar	-	-	-
Insulation: Polyester Tape, t = 0.025 mm, 2 Layers							
N _s	6 → 9 14 → 17	0.10φ x 150 USTC	3	Bifilar	-	-	-
Insulation: Polyester Tape, t = 0.025 mm, 2 Layers							

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