
Application Note:

ESR Losses In Ceramic Capacitors

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ATC 001-923 Rev. D; 4/07

ESR LOSSES IN CERAMIC CAPACITORS

In the world of RF ceramic chip capacitors, Equivalent Series Resistance (ESR) is often considered to be the single most important parameter in selecting the product to fit the application. ESR, typically expressed in milliohms, is the summation of all losses resulting from dielectric (Rsd) and metal elements (Rsm) of the capacitor, ($ESR = Rsd + Rsm$). Assessing how these losses affect circuit performance is essential when utilizing ceramic capacitors in virtually all RF designs.

Advantage of Low Loss RF Capacitors

Selecting low loss (ultra low ESR) chip capacitors is an important consideration for virtually all RF circuit designs. Some examples of the advantages are listed below for several application types.

Extended battery life is possible when using low loss capacitors in applications such as source bypassing and drain coupling in the final power amplifier stage of a handheld portable transmitter device. Capacitors exhibiting high ESR loss would consume and waste excessive battery power due to increased I^2 ESR loss.

Increased power output and higher efficiency from RF power amplifiers are more easily attainable with low loss capacitor products. Low loss RF chip capacitors used in matching applications, for example will maximize power output and efficiency of an amplifier. This is especially true with today's RF semiconductor devices such as MMICs used in portable handheld sets. Many of these devices have exceptionally low input impedance whereby any ESR loss from the capacitor used in the input matching circuit can represent a significant percentage of the total network impedance. For example, if the device impedance is 1 ohm and the capacitor exhibits an ESR of 0.8 ohm, approximately 40 percent of the power will be dissipated by the capacitor due to ESR loss. This results in a decrease of efficiency and lower output power.

High RF power applications also require low loss capacitors. For applications requiring matching of high RF power amplifiers into a dynamic load, the need for low loss capacitors is quintessential. An example of this usage includes capacitors designed into high RF power matching applications used in conjunction with semiconductor plasma chambers. In these applications the load swings from very low impedance approaching zero ohms to nearly an open circuit. This results in large circulating currents in the network and imposes considerable stress on the capacitors. Ultra-low loss capacitors such as the ATC 100 series porcelains are ideal for these circuit applications.

Thermal management considerations, especially in high RF power applications, are directly related to component ESR. The power dissipation of a capacitor in these applications can be ascertained by assessing the $I^2 \times ESR$ loss. Low loss capacitor products in these circuits will reduce the amount of heat generated, thereby making thermal management issues more manageable. See the example under 'Power Dissipation' below.

The effective gain and efficiency of small signal level amplifiers can be increased by the use of low loss capacitors. As an example, the thermal noise (KTB) of a low noise amplifier (LNA) can be minimized by employing low loss ceramic capacitors in the design. The signal to noise ratio and overall noise temperature can easily be improved by using ultra low loss capacitors.

Designing low loss ceramic capacitors into filter networks will minimize the in-band (S21) insertion loss. Also, sharp corner frequency roll-off response and return loss characteristics are readily improved.

Ceramics capacitors utilized in MRI imaging coils must exhibit ultra low loss. These capacitors are used in conjunction with an MRI coil in a tuned circuit configuration. Since the signals being detected by an MRI scanner are extremely small, the losses of the coil circuit must be kept very low, usually in the order of a few milliohms. Excessive ESR losses will degrade the resolution of the image unless steps are taken to reduce these losses. Capacitor assemblies consisting of ATC 100 series porcelains are frequently used in these applications because of their ultra-low loss characteristics. These assemblies serve to function in a resonant circuit while remaining transparent to the overall circuit losses.

Power Dissipation in a Capacitor Due to ESR

The power dissipated in a capacitor can be calculated by multiplying the ESR by the square of the RF network current.

Power dissipation in the capacitor is therefore expressed as:

$$Pd = ESR \times (RF \text{ current})^2 \text{ or } Pd = ESR \times I^2.$$

It is interesting to note that low loss capacitors may be used in very high RF power applications hundreds of times greater than the capacitors power rating. Here is an example of how low ESR capacitors are used in this manner:

RF Power = 1000 watts
Capacitor is ATC 100E102, (1000 pF)
Frequency = 30 MHz
ESR = 0.018 ohm (18 milliohms)
Circuit Application Impedance = 50 ohms

Note: The maximum allowable power dissipation for the 100E is about 5 watts.

Solution: Calculate the RF current in this application.

Using this current, calculate the power dissipated in the capacitor.

$I = \text{square root of } (P/Z)$. (This is the current associated with this application.)

Square root of $1000/50 = 4.47$ Amps

Actual Power Dissipated in the Capacitor:

$$P = I^2 \times ESR$$

(This is the power that the capacitor will dissipate)

$$P = 4.47 \times 4.47 \times 0.018 = 0.34 \text{ watts}$$

This means that for the 1000 watts RF power application in a 50 ohm impedance, only 0.34 watt will be consumed by the capacitor due to ESR losses. Accordingly, the capacitor is only dissipating 6.8% of its maximum rating due to the ESR loss. The thermal rise of the capacitor in this application is negligible and directly attributable to its ultra-low ESR loss.

Dielectric Loss (Rsd)

Dielectric loss tangent of ceramic capacitors is dependant upon specific characteristics of the dielectric formulation, level of impurities, as well as microstructural factors such as grain size, morphology, and porosity (density).

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Each dielectric material has an associated loss factor or loss tangent. The loss tangent is numerically equal to the dissipation factor (DF) and is a measure of loss in the capacitor's dielectric at RF frequencies. The effect of this loss will cause the dielectric to heat. In extreme cases thermal breakdown may lead to catastrophic failure. The dissipation factor (DF) provides a good indication of the magnitude of the dielectric loss, and is typically measured at low frequencies e.g. 1 MHz, where this loss factor is predominant.

Metal Loss (Rsm)

Metal losses are dependent on the specific resistive characteristics of all metallic materials in the capacitor's construction, as well as the associated frequency-dependent losses of electrodes due to skin effect. This includes electrodes, terminations plus any other metals such as barrier layers, etc. The effect of Rsm will also cause heating of the capacitor. In extreme cases thermal breakdown may lead to catastrophic failure. These losses encompass ohmic losses as well as 'skin effect' losses at frequencies typically above 30 MHz for most multilayer ceramic capacitors. The following is an example of ESR loss due primarily to the metallic elements Rsm and the magnitude of loss and its relationship to frequency.

Example: Given a 100 pF capacitor with an ESR of 18 milliohms @ 30 MHz, what is the ESR of this capacitor at 120 MHz?

Solution: Take the square root of the ratio of the two frequencies:

Square root of 120/30 = square root of 4 = 2

The ESR at 120 MHz is two times higher or 36 milliohms.

The following table illustrates the contribution of dielectric and metal losses for a 22 pF ATC 180R series capacitor. All losses are tabulated at various frequencies and are added together to derive the ESR. Note that dielectric losses are predominant at the lower frequencies and diminish at higher frequencies. The converse is also true for metal losses. Other capacitor values have the same pattern with different splits between Rsd and Rsm.

Frequency (MHz)	Capacitor (pF)	Rsd (m-ohm)	Rsm (m-ohm)	ESR (m-ohm)
1	180R220	145	7	152
3	180R220	48.2	7.8	56
30	180R220	4.82	9.18	14
300	180R220	0.48	28.51	29

Table 1. Contribution of Dielectric and Metal Losses for a 22 pF ATC 180R Series Capacitor.

Catalog ESR curves typically denote ESR values for frequencies at or above 30 MHz, where the losses are predominantly due to Rsm. At these frequencies the dielectric losses are virtually transparent and do not significantly influence the overall ESR.

Relationship Between ESR, Q, DF and X_C

The following figure shows the phase relationship between capacitor voltage and current as well as dissipation factor, ESR, and magnitude of the impedance. In the ideal capacitor the current leads the voltage by 90 degrees. I_A in the diagram below denotes the actual current flow through the capacitor and forms angle δ referred to as the loss angle. Also note that the

relationship between I_A and V_C is proportional to the relationship between X_C and ESR. Refer to **Table 2** below for the relationships between all parameters depicted in **Figure 1**.

The general rule is that DF is a factor that is most useful when designing for applications operating at frequencies below 1 MHz where the main loss factor is attributable to dielectric loss (Rsd). ESR and the associated Q value are virtually always associated with metal losses (Rsm) at higher radio frequencies, i.e., above 30 MHz through microwaves.

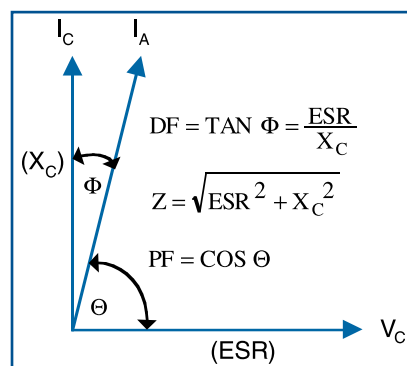


Figure 1. Phase Relationship between Capacitor Voltage and Current.

ESR =	Q =	DF =	X_C =
$X_C \times DF$	$1 / DF$	$1 / Q$	$1/2\pi \times F \times C$
$X_C \times Q$	X_C / ESR	ESR / X_C	ESR / DF
$X_C \times \tan \delta$	$1 / \tan \delta$	$\tan \delta$	$ESR \times Q$

Table 2. Relationships between all parameters.

Measuring ESR

ESR is a key parameter to consider when utilizing ceramic capacitors in RF designs. A reliable and repeatable test method must be implemented in order to establish valid capacitor ESR characterizations.

Measuring the ESR of high Q ceramic chip capacitors requires a test system with an inherent Q higher than the device under test (DUT). A high Q coaxial resonant line is most commonly utilized for these measurements. The coaxial line resonator is typically constructed from copper tubing and a solid copper rod for its center conductor. The DUT is placed in series between the center conductor and ground. See **Figure 3**.

Before performing ESR measurements the unloaded characteristics of the resonant line must be established. This is accomplished by providing RF excitation to the shorted coaxial line and ascertaining the 1/4 and 3/4 lambda bandwidth. The line is then open circuited after which the 1/2 and 1 lambda bandwidth measurements are established. This data is used to characterize the unloaded Q of the resonant line, fixture resistance and resonant frequency. The unloaded Q of the line is typically in the order of 1300 to 5000 (130 MHz to 3 GHz) with a fixture resistance rfo in the range of 5 to 7 milliohms.

The capacitor sample is placed in series with a shorting plunger located at the low impedance end of the line. The generator is tuned for a peak resonant voltage, and then re-tuned to 6 DB

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down from the peak voltage on both skirts of resonance. A loosely coupled RF millivoltmeter probe located at the high impedance end of the line will measure RF voltage at the 6 DB points.

The DUT perturbs the Q of the line changing the resonant frequency and bandwidth as compared to the unloaded line. The corresponding 6 DB down frequencies referred to as f_a and f_b are used in the calculation of the capacitor's ESR. This process is referred to as the Q perturbation method. See [Figure 2](#).

Note: Since the capacitive reactance of the test sample is in series with the line, it will shorten its electrical length depending on capacitor value. Values above 10 pF will yield reasonable measurement accuracies; however, as we approach 1 pF the measured ESR may develop substantial errors. The small capacitance values exhibiting high X_C will cause the electrical length of the line to drastically change. The reactance of the line is equal and opposite to that of the DUT at resonance.

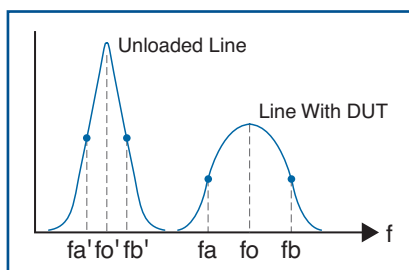


Figure 2. Bandwidth Curves for Unloaded and Loaded Line.

ESR Test System

The test system most commonly used consists of a coaxial line (Boonton Model 34A) nominally 57.7 cm in length, with a resonant frequency of 130 MHz and a characteristic impedance of 75 ohms. This impedance is chosen because it yields the highest line Q. Different line lengths may also be used for other frequency ranges.

A signal generator is connected to the low impedance end of the line and terminates in a non-inductive precision resistor. The resistor is mounted on a TNC connector and inserted into the DUT end of the line. It has an exposed loop that serves to loosely couple RF energy into the line. An RF excitation of 1 mw (0dBm)

drives the shorted line through the source loop. The generator is swept until a peak resonant voltage is displayed on the RF millivoltmeter. The source loop is physically rotated until a 3 millivolt reference voltage is achieved at the high impedance end of the line. This procedure insures that the RF excitation does not load the line. See [Figure 3](#).

An RF probe located at the high impedance end of the line is connected to a millivoltmeter to measure RF voltage at resonance. From these measurements the bandwidth and Q can be established. ESR is calculated by equating the change in bandwidth (BW) and Q, as compared to the initial unloaded shorted line condition. The BW data is put into an equation along with the initial line characterizations to calculate the ESR of the test sample. ESR measurements described here are performed in the series mode and can be achieved up to about 3 GHz.

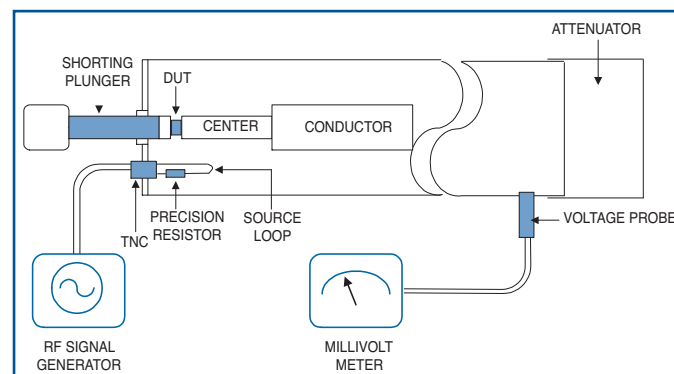


Figure 3. Coaxial Resonator with DUT.

Factors Affecting ESR Measurement

Frequency measurement data for establishing BW require a minimum of four decimal places; however, five places is desirable. Source and measurement probes must be loosely coupled to the line. The high impedance end of line should be shielded to reduce loss due to radiation to preserve Q. The shield is a cut-off attenuator offering 16 DB attenuation per radius.

Placement of the DUT in the line fixture should be consistent.

Keeping fixture contact surfaces clean is essential for good repeatability.

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ATC 001-923 Rev. D; 4/07



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