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Design Guide for QR Flyback Converter

Allan A. Saliva
Infineon Technologies North America (IFNA) Corp.

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Author: Allan A. Saliva (IFNA PMM SMD AMR PMD 2)

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1. Introduction

A Quasi-resonant Flyback is simply a DCM Flyback having a valley switching turn on. It is also known as variable frequency or valley switching Flyback and is largely used in low power SMPS application such as charger, adapter and auxiliary supply. The objective of this paper is to develop a practical, step by step and easy to follow approach in designing an off line QR Flyback power supply. This includes quick component selection guide, design knowledge and practical tips for a fast and optimized design.

2. QR Flyback Operation

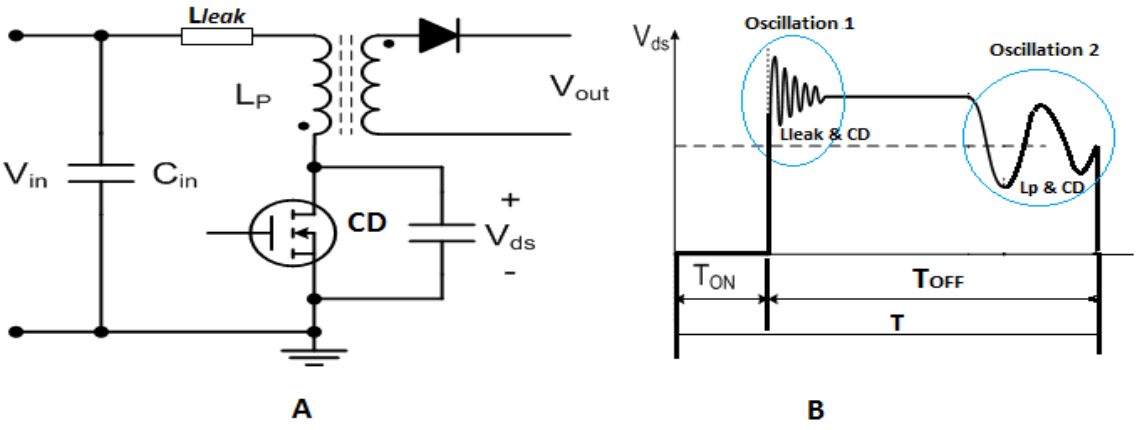


Figure 1: (A) Flyback Converter schematic (B) VDS Waveforms of a DCM Flyback

Figure 1A shows the basic Flyback converter schematic showing the primary parasitic components Lleak and CD. Lleak is the leakage inductance of the transformer while CD is the total capacitance (C_{oss} + intra-winding capacitance + stray capacitance) of the from drain node. Figure 1B shows the normal V_{DS} waveform of a DCM Flyback where two resonant oscillations can be observed. The higher frequency oscillation 1 happened during the initial turned off of the MOSFET due to the leakage inductance resonating with CD. Oscillation 2 happens when the secondary winding energy declines to zero. During this time both windings are open, thus, Lp resonates with the capacitance at the CD node.

Because of this resonance, V_{DS} will experience a minimum valley point, whose minimum value will depend on Flyback reflected voltage V_R. By making the controller to turn on at this minimum valley, we then have what is called QR or valley switching Flyback.

Depending on the QR controller, the MOSFET can be turned on at different valley of the drain-source voltage (first, second even seventh) depending on the loads. If it is always turn on at the first valley point, it is called free running quasi-resonant mode. For the free running QR, the frequency is adjusted depending on the load. Figure 2 shows the frequency vs. load relationship; the frequency is minimum at maximum load while increasing at lighter loads.

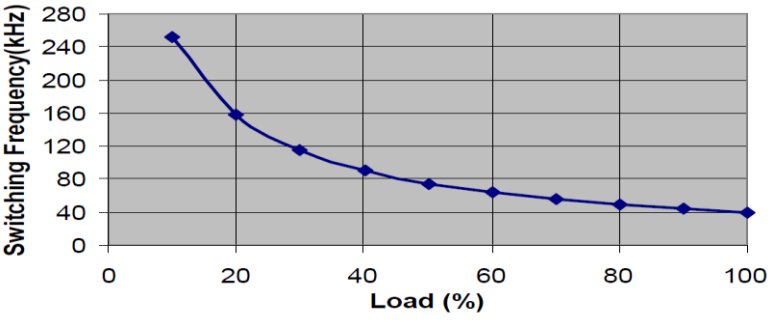


Figure 2: Free Running QR Flyback Frequency vs Pout

The switching frequency of the free running QR is given by:

$$f = \frac{1}{Ipri_{pk} \times Lpri\left(\frac{1}{Vin} + \frac{1}{VR}\right) + \pi\sqrt{Lpri \times CD}}$$ ***Equation 1***

Where: Ipripk- Primary peak current, Lpri- Primary inductance, VRp- Primary reflected voltage (Vout x Np/Ns), Vin- Input voltage and CD-Total capacitance on the drain node

In this equation it can also be seen that increasing the input voltage will also increase the switching frequency while a the it is inversely proportional to the primary inductance.

The basic QR controller uses the auxiliary winding to detect the valley point. Each time the winding voltage ZC (as shown in Figure 2) goes below to a certain threshold during the MOSFET turn off period, the MOSFET is turned on. This is usually called zero current detection ZCD because it waits for the secondary current to go down to zero before turning on the MOSFET.

Benefits of QR Flyback:

1. Lower Turn-on Loss: Since it turns on at the valley the turn on losses due to the discharging of CD is significantly reduced. This makes QR Flyback efficiency higher specially high line/lighter loads compare to a FF Flyback
2. Less Conducted EMI: Due to the ripple voltage appearing across the bulk capacitor, the switching frequency is modulated of QR Flyback is modulated at twice the mains frequency. This causes the spectrum to be spread over the wide frequency band than a single frequency values

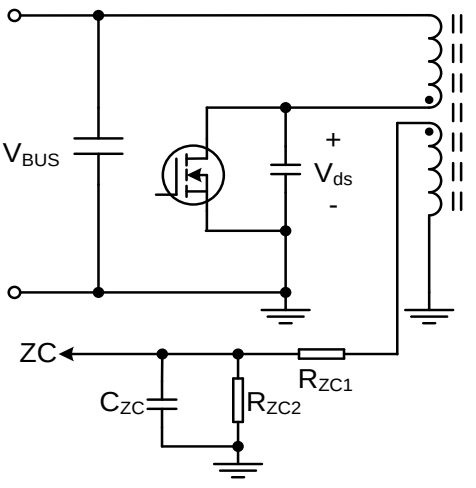


Figure 3: QR Flyback valley detection thogh ZC

Given the benefits, there are also some drawbacks. Since this is still effectively a DCM Flyback, peak and RMS current remains higher compared to CCM Flyback. This will results in higher conduction losses on the MOSFET and transformer on the primary, while requiring a larger ripple current rated capacitor at the output. Therefore it is not recommended for higher power, wide range designs exceeding 65W-100W, unless cost is a secondary factor and some other possible benefit, such as use of synchronous rectification on the secondary, is critical to system requirements.

Finally, because of the variable frequency of operation with varying line and load condition, a few different design points need to taken into consideration. The following is a sequential design guide for QR Flyback highlighting the similarities and the differences between DCM Flyback design as well as providing design tips and practical considerations.

3. QR Flyback Design Equations and Sequential Decision Requirements

STEP 1: Define and determine system requirements: Every SMPS design starts in determining the required system requirements and specifications. The following parameters need to be defined and determined.

Parameters	Descriptions
VACmax	Maximum AC input voltage
VACmin	Minimum AC input Voltage
Fsw_min	Minimum Switiching Frequency
Eff	Efficiency
Pout	Output Power (maximum)
Vout	Main Output voltage
fline	AC Line frequecny
ΔVout	Output ripple voltage
Other Requirements	

Figure 4: Input Design Parameters

An important design parameter to consider here is deciding on the minimum switching frequency. For QR Flyback the minimum frequency appears at minimum input voltage and maximum output power. The designer needs to set what would be the operating frequency at this point if operation. A higher Fsw_min would results to a smaller transformer core size with the trade off higher switching losses.

↳ Fsw_min should not be chosen lower than 20kHz to avoid operating in the audible frequency range, while the higher limit is usually below 150kHz for EMI concerns. For multiple outputs, Pout max should be the sum of each individual output.

STEP 2: Choose the right controller considering the output power requirement: A free running QR control would result in high losses with decreasing loads because of increased frequency. Some controllers place a limit on the maximum frequency, resulting in FF DCM mode at a certain point. This effectively limits the range of QR operation which will result in lower efficiency and greater EMI contribution. An ideal QR controller should be able to turn on at different valley points depending on the load, thus avoiding frequency increases at light loads while still maintaining valley switching.

Finally, other requirements, such as no load input power and average efficiency, should also be examined when choosing a suitable QR controller. Table 5 shows a selection of Infineon's QR controllers. Unlike a free running Flyback with frequency clamp, these controllers can shift QR operation on multiple valley points, thus, decreasing the frequency with decreasing loads. More information can be found in [5].

Integrated Controller and MOSFET Option	Package	MOSFET VDS	MOSFET RDSON	Pout (85V-265V)
ICE2QR4765	DIP7, DIP8,DSO16	650V	4.7 Ohm	5W-15W
ICE2QR1765	DIP7,DIP8	650V	1.7 Ohm	15W-30W
ICE2QR0665, ICE2QR1065	DIP8,DIP7	650V	0.65 hm	25W-45W
ICE2QR2280	DIP7	800V	2.2	<30W
Controller IC		**Reccomended MOSFET**		
ICE2QSO3	DIP8, SO8	IPA65R600E6 650V/0.6Ohm/TO220FP		< 60W

Table 5: Recommended QR Controller

STEP 3: Determining Input Capacitor Cin and the DC input voltage range: The capacitor Cin is also known as the DC link capacitor, depending on the input voltage and input power the rule of the thumb for choosing Cin is shown below. For wide range operation, use a DC link capacitor more than 2uF per watt of input power to get a lower ripple for the DC input voltage.

Input Voltage	Capacitance	Working Voltage
115Vac	2uF/W	~200V
230Vac	1uF/W	~400V
85Vac-265Vac	2-3uF/W	>400V

Table 6: Recommended Cin per Watt of Input Power

With the input capacitor chosen the minimum DC input voltage (DC link capacitor voltage) is obtained by:

$$VDC_{min} = \sqrt{2 \times Vac^2 - \frac{Pin_{max} \times (1 - d_{charge})}{Cin \times fline}} \qquad \textit{(Equation 2)}$$

Where: dcharge is the DC link capacitor duty ratio, which is typically around 0.2. Figure 3 shows the DC line capacitor voltage. The minimum DC input voltage occur at maximum output power and minimum AC input voltage while the maximum DCinput voltage occurs at minimum input power (no load) and maximum AC input voltage.

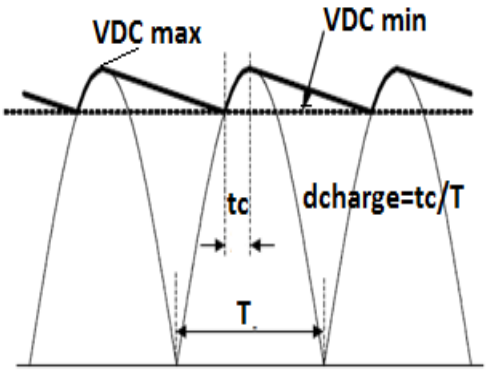


Figure 4: DC link capacitor max and min voltage

The maximum DC input voltage can be found during no load condition when the capacitor peak charge to the peak of the AC input voltage and is given by:

$$VDCmax = VACmax * \sqrt{2} \qquad \textit{(Equation 3)}$$

STEP 4: Decide on the QR Flyback Primary Reflected Voltage (VR) and MOSFET VDSmax rating:

The primary reflected voltage VR plays an important role in determining VDS valley turn on point. In FF Flyback, choosing the value of VR greatly affects many important parameters and electrical parameters of the converter (eg VDS rating of the MOSFET) . Similarly, it is true for QR but in addition, the VR value also determines the VDS valley. Figure 4 shows the typical QR Flyback where the VDS flat top is simply the sum of Vin and VR. The valley voltage in which turn on is desired is equal to the difference between Vin and VR.

This means that the higher the value of VR, the lower the valley would be and the lower the turn on loss of the MOSFET. Whenever VR is less than or equal to VIN, ZVS condition can be achieved. However as the input voltage increases ZVS can be lost, as seen on Figure 4. For wide range operation VR should be very high (~375V) to achieve ZVS over the full input voltage range. The main tradeoff here is the VDS rating requirement of the MOSFET.

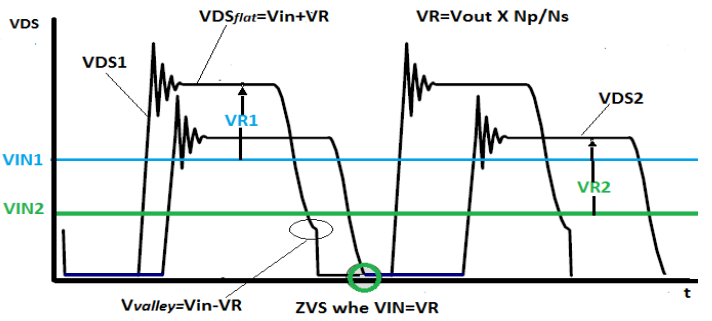


Figure 5: VDS Waveform with different Vin

Considering voltage spike due to leakage inductance, the maximum drain to source voltage is:

$$VDSmax = VDCmax + VR + Vspike$$ ***(Equation 4)***

Where: Vspike is the voltage spike caused by the leakage inductance of the Flyback transformer. For a starting point, assume Vspike is 30% of VDSmax.

The table below lists a recommended reflected voltage given a 650V or 800V rated MOSFET. As a starting point choose VR not larger than 100V for a wide range input voltage supply.

Vin	MOSFET VDS max	Recomendded Max VR *
Low line input	600V	150
Wide range AC Input: 85Vac-150Vac	650V	100V
Wide range AC Input: 85Vac-264Vac	800V	250V
Input from High voltage DC : 400VDC	800V	250V

Table 7: Recommended VR on 650 and 800V MOSFET

Choosing the reflected voltage is a compromise between the primary MOSFET and the secondary rectifier voltage stress. Setting it too high, by means of higher turns ratio, would mean higher VDS rated MOSFET to be used on the primary but lower voltage stress on the secondary rectifier. While setting it too low, by lower turn ratio, would lower VDSmax but would increase secondary rectifier stress.

STEP 5: **Calculate Primary Inductance, Lpri:** Being part of the LC tank circuit, the transformer primary inductance has a great influence on switching frequency, as seen in Equation 5. To meet the design constraint concerning the minimum operating switching frequency, the maximum primary inductance should not exceed Lpri_max .

$$Lpri = \frac{1}{\left[\left(\sqrt{2 \cdot Pin\_max \cdot Fsw\_min}\right) \cdot \left(\frac{1}{VDC_{.min}} + \frac{1}{VR}\right) + \pi \cdot Fsw\_min \cdot \sqrt{C_{.D}}\right]^2} \qquad \textit{(Equation 5)}$$

Where: CD is total capacitance at the drain node, this is approximately equal to the MOSSFET Coss, Pin_max is Pout_max/efff

↳ The maximum input power at minimum input voltage is needed for calculation of Lpri_max. Increasing inductance beyond the calculated Lprimax lowers the operating frequency at low line/maximum load below Fsw_min, which could push the transformer into saturation.

STEP 6: Calculate the primary peak current, Duty Cycle and Isecpk

$$Ipri_{pk} = \sqrt{\frac{2 \times Pin\_max}{Lpri \times Fsw\_min}} \qquad \textit{(Equation 5)}$$

$$Dmax = \frac{1}{VDC\_min} \times \sqrt{2 \times Pin\_max \times Lpri \times Fsw\_min} \qquad \textit{(Equation 6)}$$

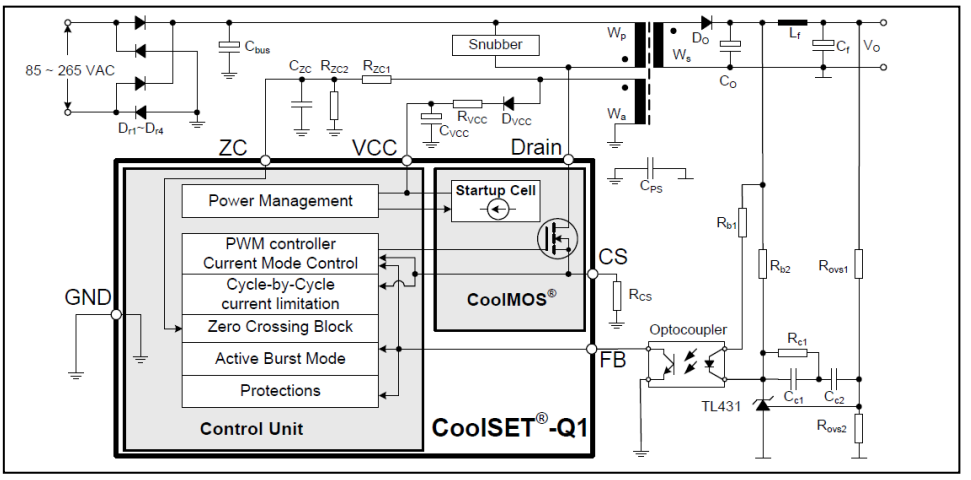
↳ **Transformer design, secondary components selection and other miscellaneous requirements are carried out just like any fixed frequency Flyback converter. Refer to the DCM Flyback design notes to complete the design steps**

4. DCM Flyback Design Example

STEP 1: System Specifications and Requirements:

Parameters	Values	
VACmax	265V	Maximum AC input voltage
VACmin	85V	Minimum AC input Voltage
fswFFF Fsw	40kHz	Switching Frequency
Eff	85%	Efficiency
Pout	25Wmax	Output Power (maximum)
Vout	12V +/- 2%	Main Output voltage
fline	60Hz	AC Line frequency
Vout ripple	120mV	Minimum ripple voltage
Other Requirements: No load Pin	<50mW	Standby input power

STEP 2: **Choosing the right controller considering Pout:** Referring to Table 3, we choose an integrated controller and MOSFET solution using ICE3BR1065J. Below is the typical Flyback application using ICE3BR1765J [4]



STEP 3: **Determining Input Capacitor Cin and the DC input voltage range:**

Maximum input power:

$$Pinmax = \frac{Pout}{n} = \frac{25W}{0.85} = 29.4W$$

Using 2uF per watt of input power, the required DC capacitor, Cin, is:

$$Cin = \frac{2uF}{W} \times 29{,}4W = 58uF \sim 68uF$$

> Use the standard capacitance value of **68uF/400V.**

With the input capacitor chosen the minimum DC input voltage (DC link capacitor voltage) is obtained by:

$$VDC_{min} = \sqrt{2 \times 85V^2 - \frac{31W \times (1-0.2)}{68uF \times 60Hz}} = \mathbf{92V} \qquad VDCmax = 265V\sqrt{2} = \mathbf{375V}$$

STEP 4: **Flyback reflected voltage (VR) and the Max VDS MOSFET voltage stress**: For a 650V MOSFET on ICE3BR0665 CoolSET, VR is chosen at 100V. Assuming 30% leakage spike the expected maximum VDS is equal to:

$$VDSmax = VDCmax + VR + 30\%Vspike$$

$$\mathrm{VDSmax} = 375\mathrm{V} + 80\mathrm{V} + 30\% \times 375V = 577V$$

STEP 5: **Calculate Primary Inductance, Lpri:**

$$\mathrm{Lpri} = \frac{1}{\left[\left(\sqrt{2 \cdot \mathrm{Pin\_max} \cdot \mathrm{Fsw\_min}}\right) \cdot \left(\frac{1}{\mathrm{VDC\_min}} + \frac{1}{\mathrm{VR}}\right) + \pi \cdot \mathrm{Fsw\_min} \cdot \sqrt{\mathrm{C\_D}}\right]^2} \quad \mathrm{Lpri} = \frac{1}{\left[\sqrt{2 \cdot 40000\mathrm{Hz} \cdot 29.4\mathrm{W}} \cdot \left(\frac{1}{92\mathrm{V}} + \frac{1}{80\mathrm{V}}\right) + 40000\mathrm{Hz} \cdot 3.14 \cdot \sqrt{100\mathrm{pF}}\right]^2}$$

$$\boldsymbol{Lpri = 726uH}$$

Where: CD is total capacitance at the drain node, assume 100pF for the CoolMOS Coss plus other parasitic capacitance on the drain node.

STEP 6: **Calculate the primary peak current, Duty Cycle and Isecpk**

$$Ipri_{pk} = \sqrt{\frac{2 \times Pin\_max}{Lpri \times Fsw\_min}} = \sqrt{\frac{2 \times 29.4W}{726uH \times 40kHz}}$$

$$\boldsymbol{Ipri_{pk} = 1.4A}$$

$$Dmax = \frac{1}{VDC\_min} \times \sqrt{2 \times Pin\_max \times Lpri \times Fsw\_min}$$

$$\boldsymbol{Dmax = 0.45}$$

↳ Transformer design, secondary components selection and other miscellaneous requirements, refer to [5]. Evaluation board and detailed descriptions on QR CoolSET are also given in [3], [5].

5. References:

[1] Product Brief, 650V SiC thinQ!™ Generation 5 diodes.
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[6] Design Guideline for Off-line DCM Flyback Converter