
Center for Advanced Power Systems
Florida State University


# Sunshine State Solar Grid Initiative (SUNGRIN)

# Model Reduction Guide

**Version 1.0**

**February 2015**

# Contents

# List of Figures



# List of Tables

# 1 Introduction

This document describes the model reduction approach and use of tools that automate the model reduction process. The need for reduced models derived from both earlier study feeders and the proposed parametric approach within the SUNGRIN high-penetration analysis project. Today's detailed power flow models of individual distribution feeder circuits may contain thousands of nodes, sections, and customer demand points. These models are the best approach toward understanding details of power flows, voltages along the feeders, and derive coordinated protection settings. The disadvantage is that large-scale studies of possible consequences of future developments require an excessive amount of computational time. The reason for the vast computational requirements derives from the need to not just perform a single or few view salient power flow computations but to explore the parameter space while using time series analysis. For example, studying the performance of a feeder circuit over a year for selected sets of planned feeder operation and distributed resource integration. Another important application of reduced models is in the area of real time simulations. Though real time simulator capabilities have vastly improved in the last decade and simulation time steps in the microsecond time range are achievable, the size of the system that can be simulated in real time is nevertheless limited. It is to be noted that the system model restrictions are more pronounced for distribution feeders than transmission systems as long(er) transmission lines allow to separate subsystems, which can be simulated on individual processors without impacting simulation result quality. Real time simulations were part of earlier phases of this project, and part of the experience gained in reduced "Rest-of-System" models found application in testing solar PV inverters at CAPS' test facility.

As the need for reduced feeder models is apparent, efforts were made to manually derive equivalent circuit models within the SUNGRIN project's earlier phases. Guided by experience and the original and detailed power flow computational models, the number of buses, sections, and customer load points were reduced. Together with available voltages, currents, and solar PV power injections, validated open use models with corresponding load and generation profiles were derived. The reduced feeder circuits were compared to the original models by assessing salient aspects such as short-circuit impedances and feeder voltage profiles. The reduced models were successfully used to study and analyze several concerns of importance in high-penetration solar PV generation situations, including impacts on protection and voltage regulation. In the last project phase, the model reduction process was formalized and converted into an automated tool. This report provides information on the model reduction concept, the tools developed, and application examples.

The objectives of this work were to develop systematic methods for converting large distribution feeder models into smaller representations for high penetration PV impact analysis. The implementation approach described herein makes use of two core components. First, the feeder circuits are modeled within the OpenDSS [1] environment and, second, MATLAB® [2] is used as the programming environment to perform the model reduction. The MATLAB environment interacts with OpenDSS through the OpenDSS provided COM-interface. This approach allows to build on a well developed and tested power flow modeling and simulation environment combined with a flexible, interpretative programming development platform that is geared toward numerical analysis. As several software vendors offer the possibility to export from their proprietary model format to OpenDSS, the reduction tool may be useful to users of other software tools as well. However, the implementation described here is not meant to handle every possible circuit configuration or feeder model component and type but to demonstrate the salient model reduction aspects. The reduction algorithm implementation has been tested with single- and multi-phase loads and feeder and transformer circuits, but the verification and validation process has been limited to two demonstration feeder circuits. One of them, "Feeder 6," is a small-scale example that allows demonstrate all possible feeder reduction steps and the resultant feeder structure and data can be easily verified at the time. The second, "Ckt 7," is a larger feeder that demonstrates the scalability of the process but requires a large number of individual steps.

The approach employed generally consists of identifying key distribution feeder buses that are to be kept in the reduced model. A mean of defining what constitutes key buses is provided and, once the reduction process is started, a function automatically scans the feeder and classifies buses. Buses that do not match key requirements are put into the candidate bus category that are to be removed. Once a candidate bus is identified, a set of actions is derived and executed to remove the bus from the model. The iterative process of identifying and removing buses is repeated until no more candidate buses can be found. At the end of

the reduction process, the reduced feeder is saved as a new OpenDSS model. In case a profile data file was provided, an updated profile file is also automatically created that maps the original feeder load demands to the new load representations.

The reduction approach is described in further detail in Section 2, and examples of applying and validating the methods are given in Section 3. General observations based on the example studies, along with concluding remarks, are given in Section 4. The developed MATLAB functions are described in Appendix 5.

# 2 Approach

## 2.1 Equivalent reduced models

The automated model reduction approach was based on the key objectives used in earlier phases (see [3] and [4]). The objectives were to both retain salient feeder structure and operating characteristics. To achieve these objectives, the following steps were followed.

- Identify key elements and buses in the system. These buses were to be kept in the final model. To retain the feeder structure, a list of key locations was established including substation, breakers and reclosers, voltage regulators, capacitor banks, large-scale solar PV sites, and medium-voltage feeder branches with significant load demand.
- After the key feeder locations were identified, corresponding feeder sections could be assigned and the equivalent impedances between the key buses computed. Short-circuit currents were determined for selected test points and compared to the results obtained using the original model.
- Design load demand data, i.e., utility installed customer transformer ratings, were aggregated into demands at the nearest retained key bus locations and scaled based on available feeder current and power flow measurements.

This process has been followed in deriving the open use models and the associated validation is documented in the respective feeder model documentation.

Several circuit reduction techniques have been developed, and an approach geared towards application in distribution system is given in [5]. This method computes lumped load representations for feeder sections with a large number equal loads, assuming a constant current load model and uniform load distribution. The resultant representation is a lumped load at the feeder section's midpoint. In a second step and based on achieving the same voltage drop, it is recognized that half of the lumped load may be connected at the end of the feeder section. Examining the feeders section representations' corresponding power losses, a difference is recognized and an alternate representation derived, which yields a feeder section with the lumped load connected one third down the line, but yields the same power loss term as the initial midpoint representation. In conclusion, the same model cannot correctly represent voltage drops and power losses at the same time. The feasibility of a model that does achieve both goals is shown with the derivation of an additional lumped load representation that splits the one equivalent lumped load into two parts of $1/3$ and $2/3$ of the initial load, connected at $1/4$ the distance and the end of the section. Though this final model is useful for converting the distributed load of a section into an equivalent representation, it is not directly applicable to the feeder circuit reduction process.

A variation of the lumped load model approach that does support model reduction was demonstrated and discussed in [6]. It is again based on using a constant current model to represent loads but allows to split a load into two parts and connects these parts to the two neighboring buses. The load fractions are derived with the constraints of reproducing the same voltage drops and the same power consumption, i.e., sum of load and line losses. Once the load is split and moved to the neighboring buses, the initial bus can be removed from the feeder model and the two line sections combined into a single section. This bus and section reduction process is feasible as long as the two line sections are compatible, i.e., the number of phases is equal and the resulting load parts can be correctly connected at the neighboring buses, i.e., preserving phase relationships.

The following proof of equivalency with respect to voltage drop and power is taken from [6] but considers all quantities involved to be complex numbers (denoted with a bar, e.g., $\bar{a} = a_{re} + j\, a_{im}$). The quantities involved are: $\bar{Z}_1$, $\bar{Z}_2$, and $\bar{Z} = \bar{Z}_1 + \bar{Z}_2$ are the individual section and total impedances; $\bar{V}_1$, $\bar{V}_2$, and $\bar{V}_3$ are the bus voltages; and $\bar{I}_1$, $\bar{I}_2$, and $\bar{I}_3$ are the load currents at the respective buses. The complex conjugate is denoted by $^*$. The voltage drop condition yields one of the load ratios that relate the original load of Bus 2 to the new loads at the neighboring buses as follows.

$$\begin{aligned} \bar{V}_1 - \bar{V}_3 &= \bar{Z}_1\bar{I}_2 + (\bar{Z}_1 + \bar{Z}_2)\bar{I}_3 \\ &= \bar{Z}_1\bar{I}_2\tfrac{\bar{Z}_1+\bar{Z}_2}{\bar{Z}_1+\bar{Z}_2} + (\bar{Z}_1 + \bar{Z}_2)\bar{I}_3 \\ &= (\bar{Z}_1 + \bar{Z}_2)\left(\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2 + \bar{I}_3\right) \\ &= \bar{Z}\left(\bar{I}_{2,2} + \bar{I}_3\right) \end{aligned} \tag{2.1}$$

Therefore, setting the new load $\bar{I}_{2,2}$ equal to $\frac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2$ and connecting it in addition to Load 3 at Bus 3 ensures that the same voltage drop is achieved. Using a second equivalent load that is to be connected to Bus 1 with the constraint of that the total currents into the models have to be equal, i.e.,

$$\bar{I}_1 + \bar{I}_2 + \bar{I}_3 = \bar{I}_1 + \bar{I}_3 + \bar{I}_{2,1} + \bar{I}_{2,2} \tag{2.2}$$

the second load can be derived as follows.

$$\begin{aligned} \bar{I}_{2,1} &= \bar{I}_2 - \bar{I}_{2,2} \\ &= \bar{I}_2 - \left(\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\right) \\ &= \tfrac{\bar{Z}_2}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2 \end{aligned} \tag{2.3}$$

Therefore, setting the new load $\bar{I}_{2,1}$ equal to $\frac{\bar{Z}_2}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2$ and connecting it to Bus 1 ensures the same total current flow and, consequently, the same power consumption. The correctness with respect to power can be shown with the following. The power consumption of the original circuit, $\bar{S}_O$, is

$$\begin{aligned} \bar{S}_O &= \bar{V}_1\bar{I}_1^* + \bar{Z}_1(\bar{I}_2 + \bar{I}_3)(\bar{I}_2 + \bar{I}_3)^* + \bar{V}_2\bar{I}_2^* + \bar{Z}_2\bar{I}_3\bar{I}_3^* + \bar{V}_3\bar{I}_3^* = \\ &= \bar{V}_1\bar{I}_1^* + \bar{V}_2\bar{I}_2^* + \bar{V}_3\bar{I}_3^* + (\bar{Z}_1 + \bar{Z}_2)\bar{I}_3\bar{I}_3^* + \bar{Z}_1(\bar{I}_2\bar{I}_2^* + \bar{I}_2^*\bar{I}_3 + \bar{I}_2\bar{I}_3^*). \end{aligned} \tag{2.4}$$

The power consumption of the equivalent circuit, $\bar{S}_E$, is

$$\begin{aligned} \bar{S}_E &= \bar{V}_1\bar{I}_1^* + \bar{V}_3\bar{I}_3^* + \bar{V}_1\left(\tfrac{\bar{Z}_2}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\right)^* + \bar{V}_3\left(\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\right)^* + \\ &+ (\bar{Z}_1 + \bar{Z}_2)\left(\bar{I}_3 + \tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\right)\left(\bar{I}_3 + \tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\right)^* \\ &= \bar{V}_1\bar{I}_1^* + \bar{V}_3\bar{I}_3^* + \bar{V}_1\tfrac{\bar{Z}_2^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2^* + \bar{V}_3\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2^* + \\ &+ (\bar{Z}_1 + \bar{Z}_2)\left(\bar{I}_3\bar{I}_3^* + \tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\bar{I}_3^* + \bar{I}_3\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2^* + \tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2\bar{I}_2^*\right) \end{aligned} \tag{2.5}$$

Reordering the last expression and using $\bar{V}_1 = \bar{V}_2 + \bar{Z}_1(\bar{I}_2 + \bar{I}_3)$ and $\bar{V}_3 = \bar{V}_2 - \bar{Z}_2\bar{I}_3$ in the terms for the equivalent load contributions yields

$$\begin{aligned} \bar{S}_E &= \bar{V}_1\bar{I}_1^* + \bar{V}_3\bar{I}_3^* + (\bar{Z}_1 + \bar{Z}_2)\bar{I}_3\bar{I}_3^* + \\ &+ \left(\bar{V}_2 + \bar{Z}_1(\bar{I}_2 + \bar{I}_3)\right)\tfrac{\bar{Z}_2^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2^* + \left(\bar{V}_2 - \bar{Z}_2\bar{I}_3\right)\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2^* \\ &+ (\bar{Z}_1 + \bar{Z}_2)\left(\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\bar{I}_2\bar{I}_3^* + \tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2^*\bar{I}_3 + \tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\bar{I}_2\bar{I}_2^*\right) \\ &= \bar{V}_1\bar{I}_1^* + \bar{V}_3\bar{I}_3^* + (\bar{Z}_1 + \bar{Z}_2)\bar{I}_3\bar{I}_3^* + \bar{V}_2\bar{I}_2^*\left(\tfrac{\bar{Z}_2^*}{\bar{Z}_1^*+\bar{Z}_2^*} + \tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\right) + \\ &+ \bar{Z}_1\left(\bar{I}_2\bar{I}_2^*\tfrac{\bar{Z}_2^*}{\bar{Z}_1^*+\bar{Z}_2^*} + \bar{I}_2^*\bar{I}_3\tfrac{\bar{Z}_2^*}{\bar{Z}_1^*+\bar{Z}_2^*} + \bar{I}_2\bar{I}_3^*\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2} + \bar{I}_2^*\bar{I}_3\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*} + \bar{I}_2\bar{I}_2^*\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\right) + \\ &+ \bar{Z}_2\left(\bar{I}_2\bar{I}_3^*\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2} + \bar{I}_2^*\bar{I}_3\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*} + \bar{I}_2\bar{I}_2^*\tfrac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\right) - \\ &- \bar{Z}_2\left(\bar{I}_2^*\bar{I}_3\tfrac{\bar{Z}_1^*}{\bar{Z}_1^*+\bar{Z}_2^*}\right) \end{aligned} \tag{2.6}$$

The last expression can be simplified and rewritten to align with the current terms of $S_O$:

$$\begin{aligned}\bar{S}_E &= \bar{V}_1\bar{I}_1^* + \bar{V}_3\bar{I}_3^* + (\bar{Z}_1+\bar{Z}_2)\bar{I}_3\bar{I}_3^* + \bar{V}_2\bar{I}_2^* + \\ &+ \bar{I}_2\bar{I}_2^*\left[\frac{\bar{Z}_1\bar{Z}_2^*}{\bar{Z}^*} + \frac{\bar{Z}_1\bar{Z}_1\bar{Z}_1^*}{\bar{Z}\bar{Z}^*} + \frac{\bar{Z}_2\bar{Z}_1\bar{Z}_1^*}{\bar{Z}\bar{Z}^*}\right] + \\ &+ \bar{I}_2\bar{I}_3^*\left[\frac{\bar{Z}_1\bar{Z}_1}{\bar{Z}} + \frac{\bar{Z}_2\bar{Z}_1}{\bar{Z}}\right] + \\ &+ \bar{I}_2^*\bar{I}_3\left[\frac{\bar{Z}_1\bar{Z}_2^*}{\bar{Z}^*} + \frac{\bar{Z}_1\bar{Z}_1^*}{\bar{Z}^*}\right]\end{aligned} \tag{2.7}$$

All terms within square brackets simplify to $\bar{Z}_1$ and the final expression is

$$\bar{S}_E = \bar{V}_1\bar{I}_1^* + \bar{V}_2\bar{I}_2^* + \bar{V}_3\bar{I}_3^* + (\bar{Z}_1+\bar{Z}_2)\bar{I}_3\bar{I}_3^* + \bar{Z}_1\left(\bar{I}_2\bar{I}_2^* + \bar{I}_2\bar{I}_3^* + \bar{I}_2^*\bar{I}_3\right), \tag{2.8}$$

proofing that the total power flows of the original and equivalent models are the same. A graphical representation of the process of splitting and moving a load to neighboring buses is shown in Figure 2.1.

As used in the derivation, a line section impedances are used to compute the load ratios. In the algorithm implemented, these line section impedances are based on the positive sequence components. Also, the scaling as implemented for 3-phase loads assumes balanced conditions.


(a) Original feeder circuit

(b) Equivalent feeder circuit

Figure 2.1: Splitting and moving a load to neighboring buses

## 2.2 Model Reduction Steps

With the above demonstrated feasibility of splitting and moving a load to neighboring buses without impacting voltage profiles and power flows, two key steps of reducing a model have been identified. These steps can be applied to any load bus that is deemed a candidate bus for reduction, i.e., not a key bus to be retained. While reducing a feeder circuit model, the following process and model reduction steps are applied.

- **Build a list of key buses:** Key buses are to be retained in the reduced model. Typical choices for key buses includes the substation, transformer and voltage regulator buses, capacitor bank locations, feeder branching nodes, distributed resource locations, and components that are deemed significant. The following provides a list of specific choices available in configuring the key bus selection process.
  - Buses explicitly identified by the user (an array of names to be passed to the function);
  - Buses with names matching a regular expression, can be used in conjunction with naming conventions to easily select portions of a feeder that are of interest to be retained;
  - A capacitor bank kVAR rating threshold, such that buses containing a capacitor bank with a rating exceeding the specified threshold are automatically retained;
  - An option to automatically retain buses including a tap changing transformer;

  - A generator kVA rating threshold, such that buses including a generation unit with a rating exceeding the specified threshold are automatically retained;
  - A load kVA rating threshold, such that all buses including loading with a rating exceeding the specified threshold are automatically retained;
  - An option to retain all three-phase buses;
  - A threshold voltage rating, such that all buses with a voltage rating above the threshold would be retained, can be used, for example, to select all of the buses of a main trunk to be retained; and
  - A per unit voltage deviation threshold, such that all buses within the solved model having voltages that differ from nominal by more than this threshold value would be retained in the reduced model.

- **Split loads:** As described above, in case a candidate bus with loads is identified, the loads can be split using the ratios derived above. The resulting load components are connected to the two neighboring buses and the initial loads removed. The load ratios are used in a separate step to update profile data accordingly. Note, this step can also be applied to loads connected through a transformer. In this case the transformer and all connected elements on the secondary side are scaled accordingly. The steps' implementation handles single-phase, phase-phase, and 3-phase connected loads accordingly, and the possibility of different phase-ordering at the neighboring buses is considered as well.

- **Move elements:** in case a candidate bus at a leaf-end of a feeder model has been identified, the connected elements (loads) can be moved to the bus "before," i.e., one bus closer to the substation in case of a radial feeder, and the leaf-end bus be removed from the circuit. The resulting current flows will be same and only the bus voltage information for the removed bus will be lost. As mentioned in the step above, the different load types and possibility of different phasing is considered when connecting the loads to the new bus.

- **Remove bus:** Any candidate bus without any load can be removed from the feeder circuit by combining the two adjacent line sections into one. Certain restrictions apply: the two adjacent line sections need to be compatible with respect to number of phases.

- **Move line:** One end of a line can be moved (i.e., reconnected) at another bus by considering the line impedance of the section the line is moved across. The reconnected line section's impedance is combined with the impedance of the section it is moved across. Three additional considerations and steps may be necessary:

  - **Compensate for moved line:** The demand along the moved line section caused a voltage drop across the line section it was moved across. Therefore, an equivalent load-generation pair needs to be added to ensure the same voltage at the original connection point. Step: add moved line's power flow as equivalent load to the initial connection point. Add the same amount as generation to the new connection point (or through a negative load).
  - **Compensate for other connected lines:** The flows of the remaining line sections caused a voltage drop. Again, an equivalent load-generation pair needs to be added to ensure the same voltage at the other end of the moved line. Step: add the sum of the other sections' power flows as equivalent load to the end of the moved line section. Add the same amount as generation to the new connection point. Note, the added load-generation pair needs to be scaled as the moved line section impedance increased. The original power flow would cause a larger voltage drop and a scaling ratio of $\frac{\bar{Z}_1}{\bar{Z}_1+\bar{Z}_2}$, where $\bar{Z}_1$ is the impedance of the section the line is moved across and $\bar{Z}_2$ is the impedance of the moved section, has to be used.
  - **Compensate for local load:** In case loads were connected at the original point of connection, an equivalent load-generation pair needs to be added to ensure the same voltage at the end of the moved line section. Step: add the sum of the local load as equivalent load to the end of the

moved line section. Add the same amount as generation to the new connection point. As in the step above, this load-generation pairs needs to be scaled to account for the larger line impedance.

Again, the step's implementation considers different load type and possibility of different bus phasing when reconnecting.

- **Combine loads:** The step of splitting and moving a load to neighboring buses may result in a large number of loads in the reduced feeder model. In case of compatible loads, i.e., phasing, connection types, and voltage rating, a single equivalent load can be computed. The profile data entries are updated accordingly, i.e., the original entries are mapped to the new equivalent load.

As stated above, the reduction process finds equivalent circuit under the assumption of constant current loads. The constant current as used during the power computations is given by a loads active and reactive power demand and its nominal voltage. As the nominal voltage is a constant scaling factor, the implemented algorithm handles and updates the power components directly rather than the currents. The same applies to the updates made to associated profile data.

Though the algorithm can handle all the situations of interest with respect to the SUNGRIN feeder reduction requirements, restrictions of the implemented model reduction algorithm apply:

- Combining line sections only succeeds in case of compatible line sections, i.e., number of phases. Also, only sequence based line information is handled.
- Only loads are currently handled but not generators, i.e., already connected distributed resources are not mapped to neighboring buses. It is assumed that the distributed generation will be connected at identified key buses after deploying model reduction.
- Load ratios are determined by using the positive sequence information only. Shunt line impedances are not considered.
- Three phase loads are assumed to be balanced.
- As outlined above, the "move line" step is involved due to the need to trace all downstream connected components to properly match power flows. This process step is computationally expensive and only been implemented by an approximate approach. The approximation is due to the use of the currents at the bus as computed in the power flow solution instead of the individual load ratings. Consequently, the resulting reduced model is only valid for the current load demand as not enough information is available to properly update the associated profile data. Also, the additional compensating load-generation pairs are only considering 3-phase connections at this point. It is noted that an algorithm could be implemented that determines the contributing downstream loads, and uses this information in computing the updated profile data. Note that the main reason for this simplified implementation is limited need for this step as branching points are kept or removed through a different set of reduction steps. Nevertheless, the current implementation allows to demonstrate the underlying concept.

One additional note: The implementations of the fundamental reduction steps keep track of both the actions taken and the actions it would take to reverse (undo) steps. Therefore, alternate algorithm implementations may be feasible that probes individual reduction steps and follows the best path forward, possibly back-tracking earlier steps in case a better choice of steps has been found.

## 2.3 Model Reduction Process

The basic model reduction steps need to be applied in a logical and automated process that scales from small demonstration models to actual large-scale feeder models. The following describes the two approaches implemented, which themselves may be combined to arrive at the final reduced model.

### 2.3.1 Topology Walking

The topology walking algorithm is based on the following iterative concept.

- **Build key and candidate bus lists:** Initially, all buses are candidates for removal. Based on the user selected choices, iterate over all buses and determine is the bus should be moved to the key bus list and making it part of the reduced model. The available list of choices includes substation, transformers, voltage regulators, capacitor bank locations, loads larger than a certain rating, branching points, bus voltage level.
- **Build topology tree:** Iterate over the feeder model from substation (root) to the feeder end points (leaves) and build the associated feeder structure tree.
- **Topology walk:** For every leave found, walk bus-by-bus back to the root. For each bus visited, determine if the bus belongs to the set of key buses or the set of candidate buses. If the bus is a key bus then move to the next bus upstream. If the bus is newly identified as a key bus, add it to the key bus list and move to the next bus upstream. If the bus is a candidate bus then evaluate which steps should be followed to remove the bus from the feeder model. Possible intermittent steps may be to move connected loads, split connected loads, move a line section, and remove the bus. Once the bus is removed, eliminate it from the candidate list and move to the next bus upstream. The algorithm exits if no candidate bus is left or all the leave-root paths have been followed.
- **Apply model reduction steps:** Once the list of actions (steps) has been generated, all actions are executed in order. Some actions may fail due to additional consistency checks such as phasing of sections to be combined. If an action does not succeed then the associated bus is kept as part of the model, the current action is terminated, and the next action applied. As a last step, individual, compatible loads at buses are combined into one.
- **Update profile data:** If a profile data file was specified, an update profile file is automatically generated that maps the initial load data to the newly connected loads. As the ratios of loads that are split and moved to neighboring buses are complex factors, both active and reactive power (or magnitude and angle) need to be updated.
- **Save reduced feeder model:** The reduced circuit model is exported as a set of OpenDSS files. These files, together with the updated profile data, can be used to setup high-penetration studies and evaluate salient feeder conditions using a time series approach and/or perform parametric studies.

A graphical representation of the model reduction process based on topology walking is shown in Figure 2.2. It is noted that the automated procedure of the topology walking currently requires a radial feeder structure though loops may be recognized and broken with additional logic.

### 2.3.2 Least Voltage Sensitivity

The Least Voltage Sensitivity algorithm is based on the following iterative concept. Based on an equivalent voltage drop index, selection of significant loads and line sections are made. The index that serves this role considers the local load and adjacent line impedances. Both, the loading and impedances are expressed in per unit values for a chosen base power and voltage rating. If a bus contains a total load of $S_{load}$ and the adjacent line impedances are $Z_1$ and $Z_2$, corresponding to two connected lines, the voltage drop indices associated with this bus are given by

$$VI = \max(|S_{load}Z_1|, |S_{load}Z_2|) \tag{2.9}$$

This index is computed for every bus with two adjacent lines, and the bus with the smallest index is removed. In this way, all buses with zero loading will be selected for removal before any buses containing loads. Similarly, buses with low impedance branches (lines, transformers, etc.) relative to the loading on the bus will be selected early in the process.

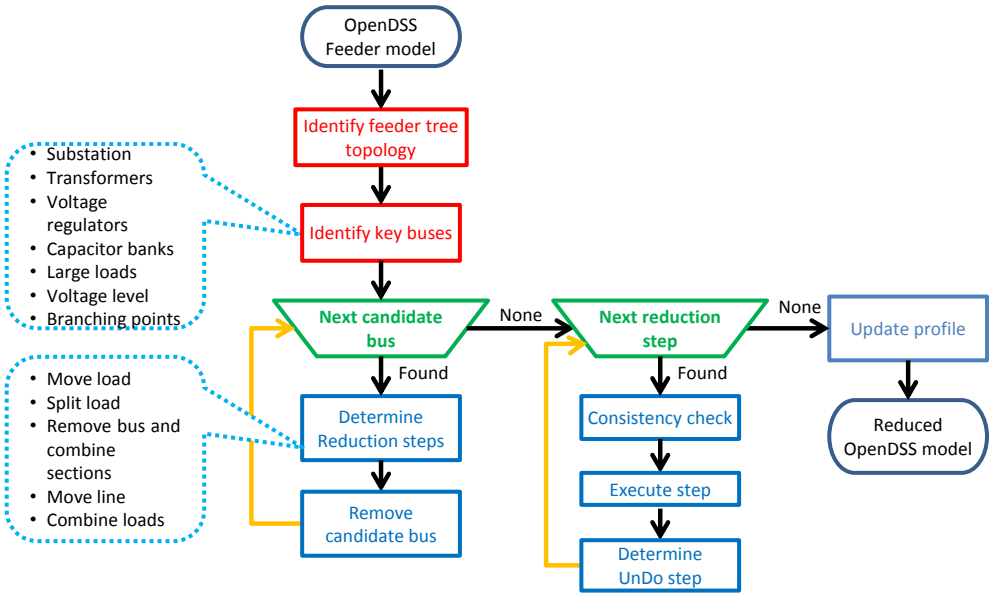



Figure 2.2: Model reduction algorithm based on topology walking

In a given iteration, once the candidate bus has been selected, the base reduction functions introduced above are used to make the necessary changes to the OpenDSS model to effect the bus removal. If a bus is connected to only one branch, the load on the bus is simply moved to the connected bus, and the branch is removed. If a bus is connected to two branches, the split-and-move approach as described above is used. The resulting algorithm is depicted in Figure 2.3.

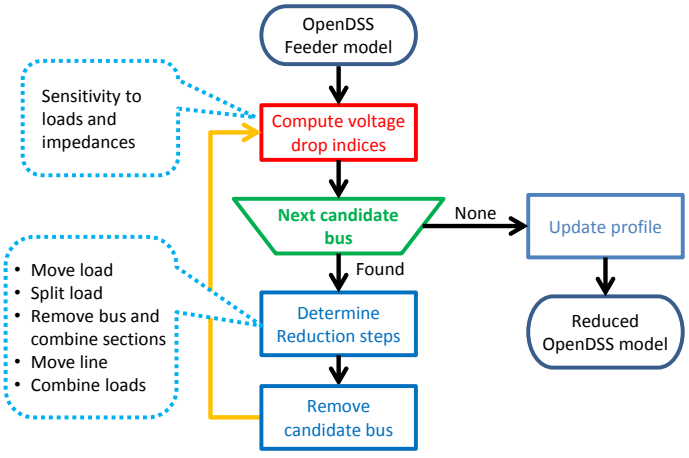



Figure 2.3: Model reduction algorithm based on voltage drop index

# 3 Examples

## 3.1 Feeder 6

The example chosen to demonstrate the model reduction procedure and algorithms is taken from [6]. The example feeder is referred to herein as "Feeder 6," and a simplified circuit diagram is shown in Figure 3.1. The diagram also gives the substation voltage, the positive sequence impedance data, and active and reactive load demands. All elements are assumed to be 3-phase and symmetric/balanced, and loads are represented by constant current loads using OpenDSS model type 5. The power flow computation results for the bus voltages and feeder section currents are shown as well. In the following different reduced feeder models are determined and compared.

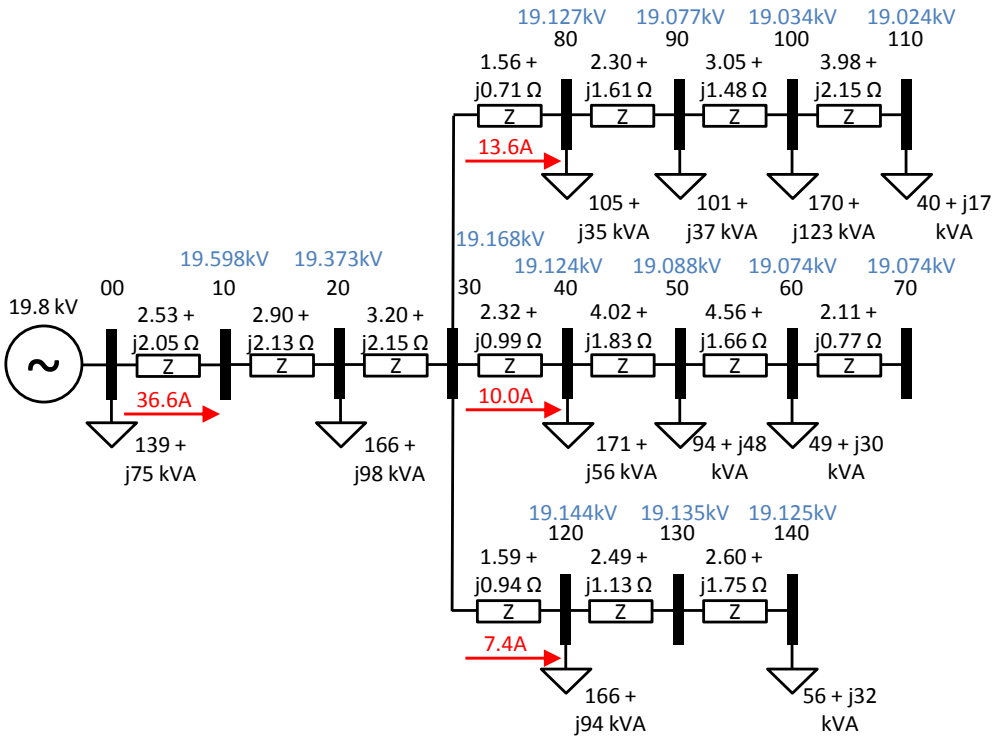



Figure 3.1: Feeder 6: Circuit diagram

As a first reduction application example, the feeder is reduced following the steps given in [6] to arrive at a model with only four buses remaining. The reduction steps taken include the custom steps of moving the connection points of two of the branches one section closer to the substation. Note that as no automated procedure can be implemented do detect the need for these two steps, all steps were manually generated and ordered. The possibility to manually implement the reduction process allowed testing the code implemented. But just as important, the developed program scripts can also be reused by other users. The program scripts available can be used as a starting point to configure reduction steps and to apply reduction steps to other feeder models. Figure 3.2 depicts the reduced feeder model and the power flow results. The list of steps taken is given in Table 3.1. Note that the order of the twenty steps is not unique, and several steps can be exchanged while nevertheless still arriving at the same reduced model. Also, the steps and parameters as used here serve an example for the reduction steps automatically generated by the reduction algorithms once a decision of how to handle a bus has been made.

An example for applying the topology walking algorithm is as follows. The algorithm accepts a list of

Table 3.1: Feeder 6: Reduction Steps for 4-bus Model

| No. | Step | Parameters | Comment |
|---|---|---|---|
| 1 | Move elements | Bus 110 | Dangling end, move connected load up |
| 2 | Remove bus | Bus 110 | Nothing connected, can be removed |
| 3 | Remove bus | [Bus 10, Bus 130] | Nothing connected, can be removed, combines adjacent lines |
| 4 | Move line | Bus 30, [Bus 20, Bus 80] | Reconnect line 30-80 at Bus 20, updates line impedance and adds load-generation pairs as necessary |
| 5 | Move line | Bus 30, [Bus 20, Bus 120] | Reconnect line 30-120 at Bus 20 |
| 6 | Move elements | [Bus 140, Bus 120],[Bus 120, Bus20] | Moves loads from Bus 140 to 120 and 120 to 20 |
| 7 | Remove bus | [Bus 140, Bus 120] | Nothing connected, can be removed |
| 8 | Split bus | Bus 80, [Bus 20, Bus 90] | Split load at bus 80 and move parts to Buses 20 and 90 |
| 9 | Remove bus | Bus 80 | Nothing connected, can be removed, combines adjacent lines |
| 10 | Split bus | Bus 90, [Bus 20, Bus 100] | As above: Split load and move parts to neighboring buses |
| 11 | Remove bus | Bus 90, [Bus 20, Bus 100] | Nothing connected, can be removed, combines adjacent lines |
| 12 | Split bus | Bus 60, [Bus 50, Bus 70] | As above: Split load and move parts to neighboring buses |
| 13 | Remove bus | Bus 60 | Nothing connected, can be removed, combines adjacent lines |
| 14 | Split bus | Bus 50, [Bus 40, Bus 70] | As above: Split load and move parts to neighboring buses |
| 15 | Remove bus | Bus 50 | Nothing connected, can be removed, combines adjacent lines |
| 16 | Split bus | Bus 40, [Bus 30, Bus 70] | As above: Split load and move parts to neighboring buses |
| 17 | Remove bus | Bus 40 | Nothing connected, can be removed, combines adjacent lines |
| 18 | Split bus | Bus 30, [Bus 20, Bus 70] | As above: Split load and move parts to neighboring buses |
| 19 | Remove bus | Bus 30 | Nothing connected, can be removed, combines adjacent lines |
| 20 | Combine loads | | Replaces individual loads by one equivalent, performed for all buses |

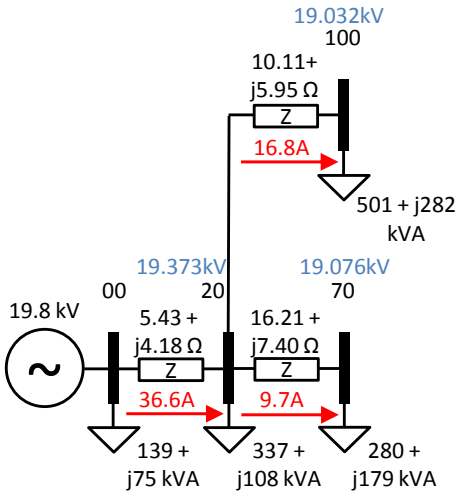



Figure 3.2: Reduced Feeder 6: 4-bus version

key buses and parameters as input, and the following has been specified: keep buses 00, 20, 70, and 100, and keep branching points. The algorithm automatically identifies a list of actions to take, followed by applying the actions one at a time. The resulting feeder model is shown in Figure 3.3.

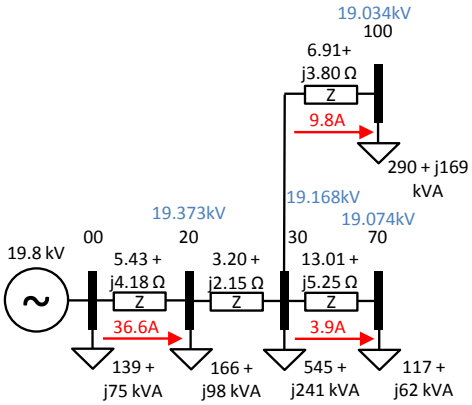



Figure 3.3: Reduced Feeder 6: Result for topology walking algorithm after adding Bus 20 to the list of key buses and preserving branching points

As can be noticed by comparing the previous power flow results with respect to the line section currents, the reduction process yields models that does not allow to directly compare current flows (though these can be recovered by considering portions of the reconnected loads.) As an example to demonstrate that current could be preserved if desired is the following. Again using the topology walking algorithm but adding the first buses after the branching point (Buses 40, 80, and 120) to the list of key buses yields the result as depicted in Figure 3.4. As described above, one of the core reduction steps is to split a load into two parts and connect the load parts at the neighboring buses. This step requires the associated load profile data to be updated accordingly. While the reduction algorithm perform the reduction steps, it keeps track of the ratios computed for the new load parts. Therefore, once the reduction process ended, these ratios can be used to map the original load profile data to the loads in the reduced circuit. This load update process may

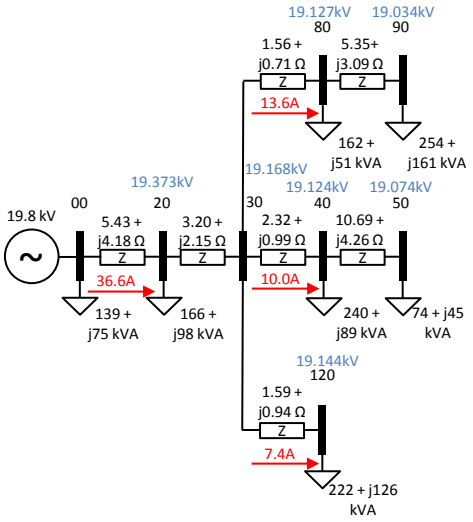
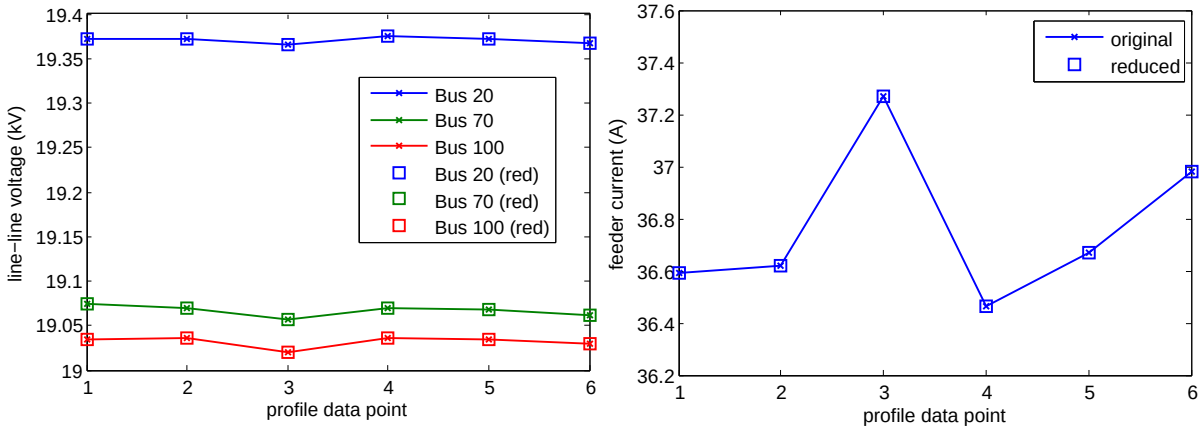



Figure 3.4: Reduced Feeder 6: Result for topology walking algorithm and preserving section current flows

mean that several of the originally individual loads get mapped into a single equivalent load. To demonstrate that the resulting feeder model and associated profile data match the original circuit, the following example is given. The load demand data as shown in Figure 3.1 is the first row of data in the original load profile, see Table 3.2. The additional rows have been generated by randomly modifying the data entries in the row above by factors between 0.9 and 1.1. Also, the load demand entries for the reduced circuit and computed during the reduction process have been rounded differently (to 0.1 kW and kvar) to indicate modified data. The power flow results for the key bus voltages and feeder current are shown Figure 3.5. The results for the two feeder circuit are basically indistinguishable.




(a) Comparing selected bus voltages

(b) Comparing feeder current

Figure 3.5: Feeder 6: Comparing selected bus voltages and feeder current of original and reduced model (topology walking)

Table 3.2: Feeder 6: Profile Data

(a) Load demand data for original circuit

| Data point | Load 00 (kW) | Load 00 (kvar) | Load 20 (kW) | Load 20 (kvar) | Load 40 (kW) | Load 40 (kvar) | Load 50 (kW) | Load 50 (kvar) | Load 60 (kW) | Load 60 (kvar) | Load 80 (kW) | Load 80 (kvar) | Load 90 (kW) | Load 90 (kvar) | Load 100 (kW) | Load 100 (kvar) | Load 110 (kW) | Load 110 (kvar) | Load 120 (kW) | Load 120 (kvar) | Load 140 (kW) | Load 140 (kvar) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 139 | 75 | 166 | 98 | 171 | 56 | 94 | 48 | 49 | 30 | 105 | 35 | 101 | 37 | 170 | 123 | 40 | 17 | 166 | 94 | 56 | 32 |
| 2 | 128 | 73 | 179 | 107 | 171 | 59 | 102 | 49 | 47 | 29 | 99 | 37 | 111 | 41 | 165 | 114 | 42 | 19 | 156 | 102 | 54 | 30 |
| 3 | 121 | 71 | 188 | 103 | 162 | 62 | 103 | 47 | 48 | 27 | 101 | 40 | 110 | 42 | 178 | 112 | 45 | 17 | 140 | 110 | 55 | 28 |
| 4 | 128 | 78 | 179 | 94 | 162 | 57 | 106 | 51 | 51 | 25 | 111 | 42 | 114 | 40 | 175 | 112 | 45 | 17 | 140 | 117 | 60 | 27 |
| 5 | 135 | 80 | 197 | 96 | 156 | 52 | 113 | 50 | 52 | 24 | 116 | 41 | 105 | 41 | 185 | 120 | 43 | 17 | 135 | 117 | 63 | 27 |
| 6 | 134 | 86 | 203 | 93 | 168 | 50 | 111 | 55 | 52 | 26 | 109 | 38 | 113 | 39 | 185 | 124 | 40 | 17 | 125 | 106 | 62 | 26 |

(b) Load demand data for reduced circuit

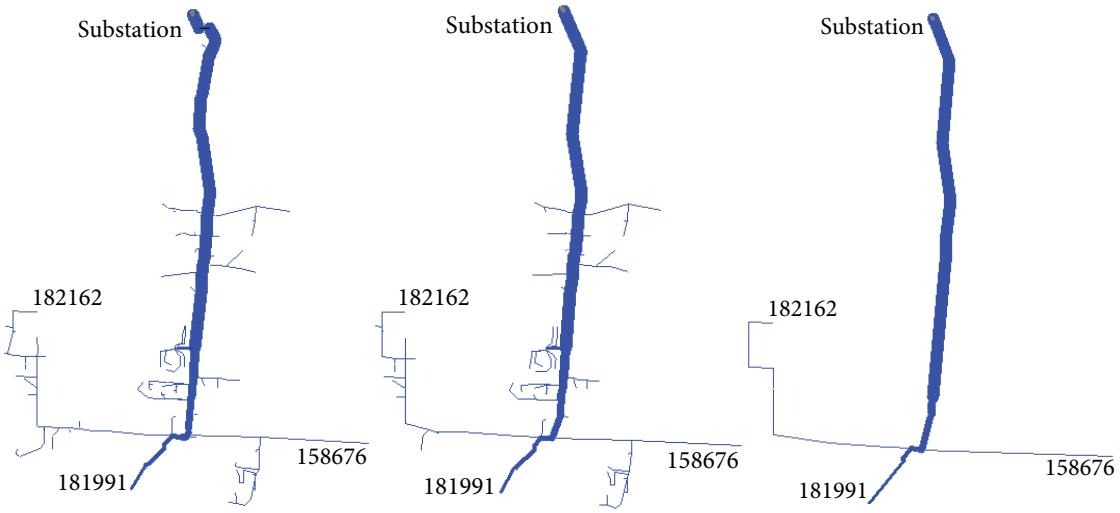
| Data point | Load 00 (kW) | Load 00 (kvar) | Load 20 (kW) | Load 20 (kvar) | Load 30 (kW) | Load 30 (kvar) | Load 70 (kW) | Load 70 (kvar) | Load 100 (kW) | Load 100 (kvar) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 139 | 75 | 166 | 98 | 544.7 | 241.3 | 117.2 | 61.5 | 290.2 | 169.2 |
| 2 | 150 | 79 | 163 | 107 | 549.2 | 238.9 | 123.3 | 61.2 | 280.5 | 168.9 |
| 3 | 156 | 80 | 163 | 99 | 563.1 | 225.0 | 128.6 | 58.8 | 294.3 | 177.2 |
| 4 | 147 | 74 | 158 | 94 | 552.5 | 229.0 | 126.1 | 61.2 | 279.4 | 179.9 |
| 5 | 142 | 78 | 167 | 100 | 543.4 | 240.7 | 124.2 | 65.5 | 285.3 | 165.7 |
| 6 | 148 | 84 | 177 | 97 | 543.8 | 251.1 | 122.8 | 69.9 | 276.3 | 177.0 |

## 3.2 Circuit 7

While the examples in the previous section are meant to document fundamental steps in model reduction and show simple examples, the case discussed here was used to test the concept on a larger system. The reduction steps and tree walking algorithm are applied to one of the OpenDSS example feeders, "Ckt. 7," referred herein as Circuit 7. Circuit 7 original feeder structure is shown in Figure 3.6(a), and the locations of the three key buses (181991, 158676, and 182162) used are indicated. The feeder's corresponding OpenDSS model summary lists 1255 buses, 2232 devices, and 2452 nodes. Note that only 290 buses are used to draw the circuit structure in the original model, i.e., these are the buses with existing x-y-coordinate information available.

The feeder is basically treated as grey box and only a few key buses are manually identified in the original model and used as key buses in the reduction algorithm. In the first reduction algorithm application, choices are to not move branching points and keep capacitor banks and transformers. In addition to the key buses indicated in the figure, the buses at the substation feeding Circuit 7 are specified (SourceBus, Ckt7, and 318412). After model reduction 317 buses, 487 devices, and 636 nodes remain, and 187 buses represent the reduced model in Figure 3.6(b). With respect to buses, a 75% reduction was achieved. By comparing the two feeders, it can be seen that the number of buses can be significantly reduced without losing valuable features in the structure. Note, the coloring and line thickness reflects the power flow as drawn by OpenDSS.

Several power flow computation results were compared to ensure the validity of the reduced model. The following provides a summary of results when modeling all loads as constant current loads, i.e., model=8 and zipv=(0 1 0 0 1 0 0) with minimum voltage of Vmin = 0.85 pu. The selected items of interest are the key bus voltages and feeder current, and their values are listed in Table 3.3. To further check on results of the reduced models, the bus distances of the original and reduced model were compared, see Figure 3.7(a). As all buses are on the expected (blue) line, indicating correct distance values, it is concluded that the code of reducing a bus and combining line sections is properly implemented. Figure 3.7(b) compares all node voltages but no significant difference is visible as the markers of the two circuits are on top of each other. A note on the voltages shown in the figure: the nodes appear ordered to some extend starting at the substation, and the initially distinct three phase voltages become more interleaved on the transformer secondaries and load points.



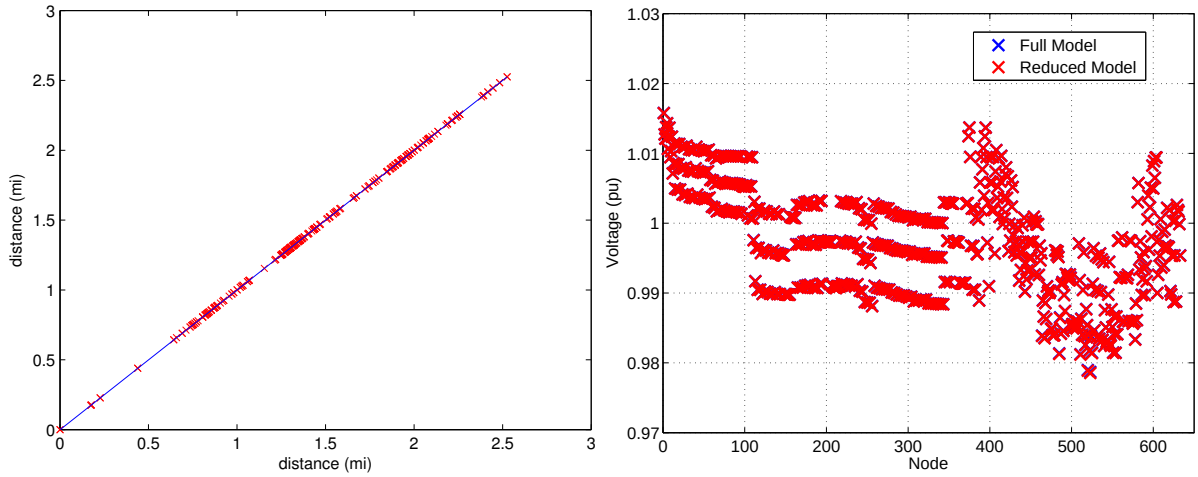

(a) Circuit 7 (1255 buses) (b) Circuit 7 (reduced, 317 buses) (c) Circuit 7 (reduced, 32 buses)

Figure 3.6: Circuit 7: Feeder structure

Further circuit reduction is feasible and shown as a second example here. By specifying the key buses as

Table 3.3: Circuit 7: Comparing original and reduced models (magnitude and angle)

| Quanity | Phase | Original | 317 bus | 32 bus |
|---|---|---|---|---|
| Voltage at Ckt7 | 1-2 | 12.660 ∠-4.7 | 12.659 ∠-4.7 | 12.667 ∠-4.7 |
| (kV) | 2-3 | 12.621 ∠-124.8 | 12.620 ∠-124.8 | 12.628 ∠-124.8 |
| | 3-1 | 12.613 ∠115.4 | 12.612 ∠115.4 | 12.620 ∠115.4 |
| Current at feeder head | 1 | 207.320 ∠159.9 | 207.300 ∠-159.8 | 206.970 ∠160.2 |
| (A) | 2 | 215.200 ∠38.6 | 215.190 ∠-38.6 | 214.860 ∠38.9 |
| | 3 | 207.360 ∠-82.7 | 207.360 ∠-82.7 | 206.980 ∠-82.3 |
| Voltage Bus 182162 | 1-2 | 12.434 ∠-6.0 | 12.433 ∠-6.0 | 12.457 ∠-6.1 |
| (kV) | 2-3 | 12.402 ∠-126.3 | 12.402 ∠-126.3 | 12.426 ∠-126.4 |
| | 3-1 | 12.369 ∠114.0 | 12.368 ∠114.0 | 12.391 ∠113.9 |
| Voltage Bus 181991 | 1-2 | 12.428 ∠-6.0 | 12.427 ∠-6.0 | 12.450 ∠-6.1 |
| (kV) | 2-3 | 12.399 ∠-126.3 | 12.399 ∠-126.3 | 12.423 ∠-126.3 |
| | 3-1 | 12.364 ∠114.0 | 12.363 ∠114.0 | 12.386 ∠113.0 |
| Voltage Bus 158676 | 1-2 | 12.455 ∠-6.0 | 12.455 ∠-6.0 | 12.477 ∠-6.1 |
| (kV) | 2-3 | 12.427 ∠-126.3 | 12.426 ∠-126.3 | 12.449 ∠-126.3 |
| | 3-1 | 12.392 ∠114.0 | 12.391 ∠114.0 | 12.414 ∠113.9 |

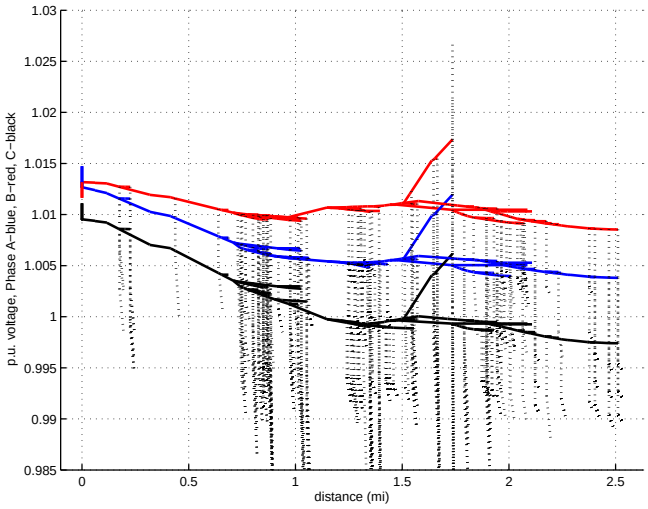



(a) Comparing bus distances: reduced (red marker) vs. original (blue line)

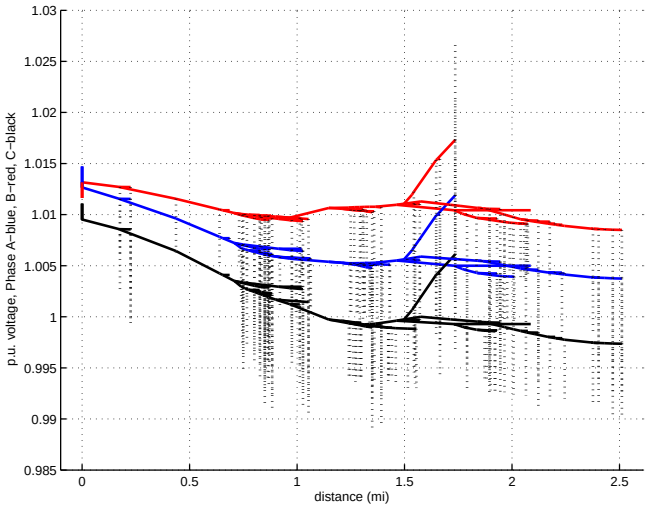
(b) Comparing node voltage magnitudes

Figure 3.7: Circuit 7: Validating reduced model against original

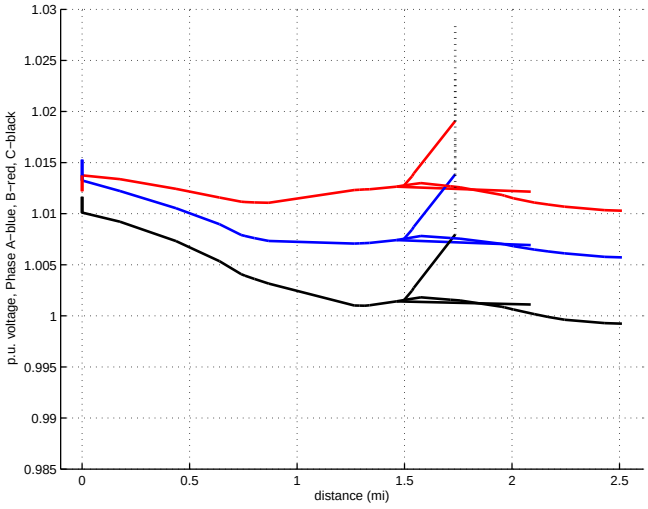
listed above, including capacitor banks but excluding transformer buses, the circuit is reduced to 32 buses, 122 devices, and 96 nodes. With respect to buses, the outcome reflects a 97.5% reduction. The resulting feeder structure is shown in Figure 3.6c, and the numerical results for the corresponding voltages and current are listed in Table 3.3. The maximum difference in bus voltages is 24 V and, based on a nominal voltage of 12.47 kV, this difference is less than 0.2%. The magnitude difference in currents is less than 0.38 A (Phase C), or 0.2% with respect to the original feeder current of 207.36 A.




(a) original circuit




(b) 317 Bus




(c) 32 Bus

Figure 3.8: Circuit 7: Feeder voltage profiles for original and reduced circuits

The three models were further used to investigate the voltage profiles after interconnecting a 4.5 MW solar PV plant. Bus 181991 was chosen as the point of common coupling, and the plant size was derived from the line feeding the bus, i.e., 230 A at 12.47 kV. The local load is about 350 kW. The corresponding voltage profiles are shown in Figure 3.8. All three profile plots are scaled with the same settings, i.e., the y-axis setting of the 317 bus circuit have been applied to the other two. As chosen in the model reduction setup, the 317 bus feeder differs from the original by eliminating the final line sections that feed customers, and the associated voltage drops are missing in this model. The 32 bus version eliminates all the load transformers but keeps the PV plant interconnection transformer.

The two model reductions required the following number of actions and steps. First, the algorithm generated a list of actions to be taken, e.g., "move elements." Second, each action was implementing by executing individual steps, e.g., all loads at a bus are moved to a neighboring bus. For both reduction processes, the corresponding action and step counts are listed in Table 3.4.

Table 3.4: Circuit 7: Number of reduction actions and steps

| **Model** | **Actions** | **Steps** |
|---|---|---|
| 317 Bus | 1877 | 3032 |
| 32 Bus | 2447 | 29861 |

# 4 Conclusion

The availability of reduced distribution feeder circuits models has been of important for several reasons. As full-scale models may include several thousand buses,line sections, and loads, parametric time series studies become quickly infeasible. This restriction applied even though today's power flow solvers are able to handle such systems and may solve for a single solution within seconds. Reduced models allow to focus on salient feeder and operation aspects without compromising the results from a quantitative and qualitative view.

This report describes the model reduction approach and salient implementation aspects of both individual reduction steps and algorithms. The algorithms allow to automate the reduction process and are based on the core concept of identifying key buses to keep and candidate buses to remove. Once a candidate bus is identified, steps to remove it from the model are taken. Several customizable parameter choices are provided to allow tailor the reduction process to a specific feeder. The MATLAB functions developed provide the required functionality to setup and execute the model reduction process, interacting with OpenDSS through the COM-interface. As demonstrated in the examples, the reduction process has been successfully tested and the validity of results confirmed. Based on the constant current load model, power flow results for the reduced feeder circuits compare well to the original circuits.

# 5 Model Reduction Functions

As described above, five base reduction steps are necessary to achieve model reduction. Besides this core reduction functions several additional are required to setup the feeder model and execute the reduction process. The functions specifically developed to implement the model reduction process are listed in Table 5.1. The core function are indicated by their short description in the "Reduction step" column, and others are facilitating functions.

The function have been written in the MATLAB environment and interact with the OpenDSS feeder model through the COM-interface. The set of functions allow to use OpenDSS models as a starting point for model reduction, and depending on the algorithm chosen additional parameters can be set to configure the reduction process. Additional information is available in the functions documentation, MATLAB help for each of the functions, and browsable function documentation.

Table 5.1: Model reduction functions

| No. | Reduction Step | Function Name | Description |
|---|---|---|---|
| 1 | | sg_DispatchReduction.m | Main entry point for reduction process |
| 2 | | sg_FeederReductionSetup.m | Feeder case setup |
| 3 | | sg_findAdjacentBuses.m | Determine adjacent buses and lines at a bus |
| 4 | | sg_GetTopologyTree.m | Build topology tree |
| 5 | | sg_getObjectProperties.m | Determine an OpenDSS object's properties |
| 6 | | sg_IDkeyBuses.m | Determine initial key and candidate bus lists |
| 7 | | sg_modelResultsComparisonReduction.m | Compute data for comparison of models |
| 8 | Combine Loads | sg_openDssCombineLoads.m | Combines individual loads into aggregated loads |
| 9 | | sg_openDssGetGenInfo.m | Extract feeder information on generators |
| 10 | | sg_openDssGetLineInfo.m | Extract feeder information on lines |
| 11 | | sg_openDssGetLoadInfo.m | Extract feeder information on loads |
| 12 | | sg_openDssGetTransformerInfo.m | Extract feeder information on transformers |
| 13 | Move Elements | sg_openDssMoveElements.m | Move elements from a specified bus to another |
| 14 | Move line | sg_openDssMoveLine.m | Reconnect a line at a different bus |
| 15 | Remove bus | sg_openDssRemoveBus.m | Eliminate bus from the circuit, combines lines if necessary |
| 16 | Split bus | sg_openDssSplitBus.m | Split a load into part and reconnect at neighboring buses |
| 17 | | sg_ProfileUpdate.m | Compute profile data for reduced circuit |
| 18 | | sg_Reduction_Metric.m | Entry point for model reduction based on alternate metrics |
| 19 | | sg_Reduction_Topology.m | Entry point for topology reduction algorithm |
| 20 | | sg_voltageDropMetric.m | Computes voltage drop as index for reduction process |

# References


[1] Electric Power Research Institute, Inc. (EPRI). OpenDSS. `https://sourceforge.net/projects/electricdss/`, 2013.

[2] The MathWorks Inc. Matlab. `http://www.mathworks.com/`, 2015.

[3] Harsha Ravindra, M.O. Faruque, Karl Schoder, Rick Meeker, Michael Steurer, and Peter McLaren. Modeling and validation of a utility feeder for study of voltage regulation in the presence of high PV penetration. Proceedings of the IEEE PES T&D Conference and Exposition, 2014.

[4] Harsha Ravindra. Investigation of dynamic interactions of PV inverters and traditional devices in regulation of voltage on distribution feeders with high penetration levels of solar PV. Master's thesis, Florida State University, 2013.

[5] W.H. Kersting. *Distribution System Modeling and Analysis, Third Edition.* Taylor & Francis, 2012.

[6] Matthew J. Reno, Robert J. Broderick, and Santiago Grijalva. Formulating a simplified equivalent representation of distribution circuits for PV impact studies. *Sandia National Laboratories SAND2013-2831*, 2013.