Electric Networks: Computer Aided Analysis and Simulation
Prof. Kai Strunz, Faculty of Electrical Engineering and Computer Science, TU Berlin

Problem Sheet 7 January 2021

Given is the following pattern of an admittance matrix:

$$\boldsymbol{Y} = \begin{pmatrix} \times & 0 & \times & \times & \times \\ 0 & \times & \times & \times & \times \\ \times & \times & \times & 0 & 0 \\ \times & \times & 0 & \times & 0 \\ \times & \times & 0 & 0 & \times \end{pmatrix}$$

a) Draw topological graph.

b) Determine the factorized matrix $\boldsymbol{Q}$ and mark the fill-in elements.

c) Determine the factorization path graph for all nodes.

d) Assume that between nodes 1 and 4 a diode is connected. Which rows and columns have to be refactorized when the status changes?

e) Renumber the nodes of the topological graph with the aim to reduce the number of fill-in elements.

f) Determine new $\boldsymbol{Y}$ and $\boldsymbol{Q}$.

g) Determine the new factorization path graph for all nodes.

h) When the diode changes status now, which rows and columns of the new $\boldsymbol{Q}$ have to be updated?