CDA3103

Project 1: Digital Clock

Spring 2019

Due : March 3, 2019

General Info

- **Topic:** **A digital clock (Time and Date)**
  - If you are interested to work on a special topic, please send your topic to the lecturer. If it was approved, you can work on your own topic.
- **Deadline:** **March 3, 2018**
- **Early Submission:** **Feb 24, 2018 (5 points bonus)**
- **Total Points:** **100 points (25 bonus points)**
- It should be completed **individually**.

Objectives

- To practice how to design and implement combinational and sequential digital systems.

- To design, implement and simulate a digital clock capable of displaying seconds, minutes and 12 or 24 hours timing, with a date indicator that display days ,months and years.

Marks Breakdown

Element	Points
Second counter circuit section	10
Minute counter circuit section	10
Hours counter circuit section	10
Days counter Circuit section	15
Months counter circuit section	10
Years counter circuit section	15
AM/PM	5
Cascading the blocks	15
Report	10
Bonus: Stop watch	5
Bonus: Adjustable Clock	10
Bonus: Creativity in design, implementation	Max 5
Bonus: Early submission	5
Total	100 + 25 (bonus)

Introduction

A digital clock is a type of clock that displays the time digitally. It uses digital counters that count second, minute and hours. Each sixty seconds make a minute and each sixty minutes an hour. After twenty four hours the clock resets and starts from initial condition. The functional unit of a digital clock is a counter that represents a second, minute or hour block.

A counter may be defined as a register i.e. a group of flip-flops that goes through a predetermined sequence of states upon the application of input pulses. The logic gates in a counter are connected in such a way as to produce a prescribed sequence of binary states in the register.

DESIGN PROCEDURES

- For easier design, the general circuit of the digital clock is divided into seven sub sections namely;
  1. Second counter circuit section
  2. Minute counter circuit section.
  3. Hours counter circuit section.
  4. Days counter Circuit section.
  5. Months counter circuit section.
  6. Years counter circuit section.
  7. Initialization control Unit. (Optional: The rest of the circuit that normally will be used for initialization will be in this section or you can include them in the previous sections.)
  8. Stopwatch section (Bonus : 5 points)
  9. Adding extra inputs for adjusting the time and date to a certain time and date (Bonus : 10 points)

DESIGN PROCEDURES (cont.)

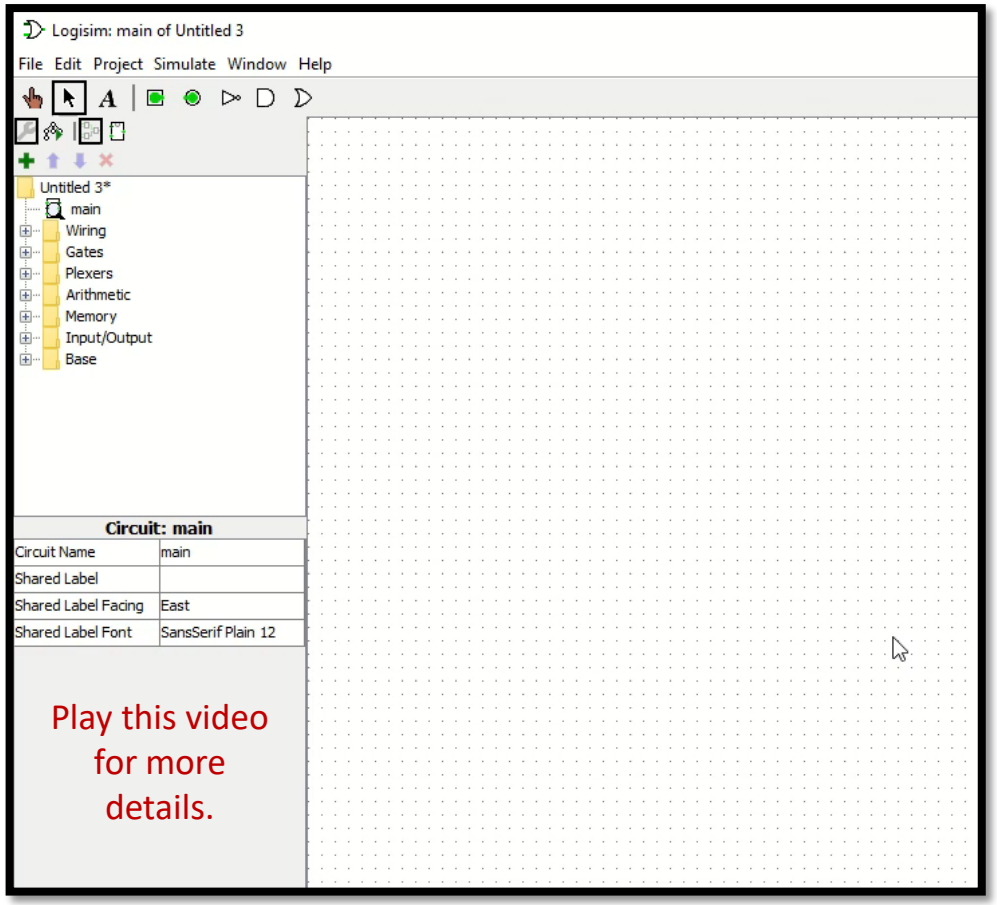
1. **Design and implement the second's circuit subcircuit.**

   - The second's circuit is designed by cascaded arrangement of a divide-by-60 counter that will count from 00 to 59 and then recycle back to 00 for 60 seconds when a clock pulse is applied to their clock inputs.

- **Then Add the subcircuit to the library of LOGISIM.**
  - See the clip on the next slide.
  - In this clip, an 8-bit build-in counter of Logisim has been used. It is maximum value is set to 60 (decimal) or 3C (hex), But you should build your own counter using 1-bit D Flip-Flops with the same behavior, input and outputs.
  - The final layout of your design should be similar to this clip.
    - 1 input: CLK
    - 2 outputs: Sec, and Carry.

DESIGN PROCEDURES (Cont.)

1. **Design and implement the second's circuit subcircuit.**
   - Add the subcircuit to the library of LOGISIM.
     - The final layout of your design should be similar to this clip.
       - 1 input: CLK
       - 2 outputs: Sec, and Carry.



DESIGN PROCEDURES (Cont.)

2. **Design and implement the minute's circuit subcircuit.**
   - The minute's circuits is designed by cascaded arrangement of a divide-by-60 counter that will count from 00 to 59 and then recycle back to 00 for 60 minutes count when a clock pulse is applied to their clock inputs.
   - The output of the second's circuit is fed into the input of the minute's circuit so that for every 60 seconds the minutes counter will advance through its states from 00 to 59.

- Then Add the subcircuit to the library of LOGISIM.

DESIGN PROCEDURES (Cont.)

3. **Design and implement the Hours circuit subcircuit.**

   - Similarly, the Hours circuit section is formed by divide–by-10 and a truncated sequence divide-by-10 counter connected through the output of the minute's section such that for every 60 minutes the counter would advance through its states from 01-12 hours or 01-24 hours timing depending on the users choice of selection from an input to affect the choice.

- **Then Add the subcircuit to the library of LOGISIM.**

DESIGN PROCEDURES (Cont.)

4. **Design and implement the day's circuit subcircuit.**

   - For the day's circuit section two divide-by-10 counters with truncated sequence are used to keep track of the days in every month. The input of the day's circuit section is connected to the output of the hour's circuit section through a single decade counter that will control the timing between 12 and 24 hours. If the user choice is 24 hours timing, the days circuit section is expected to advance through all its states for every 24 hours while if the choice is 12 hours the single decade count is expected to allow the days count to advance through its state if and only if it cycles twice to complete a 24 hours count.

- **Then Add the subcircuit to the library of LOGISIM.**

DESIGN PROCEDURES (Cont.)

5. **Design and implement the month circuit subcircuit.**

   - The month circuit section consist of a divide-by-10 and a truncate sequence divide-by-10 counter display 01 to 12 to indicate January to December whenever days circuit complete its cycle of days; at the same time control the number of days required for each month.

   - This is accomplished by coupling the month circuit section back to the days circuit section such that whenever the clock is on April, June, September and November the days count should be 30, 28 for February alone and 31 day for the rest of the months.

- **Then Add the subcircuit to the library of LOGISIM.**

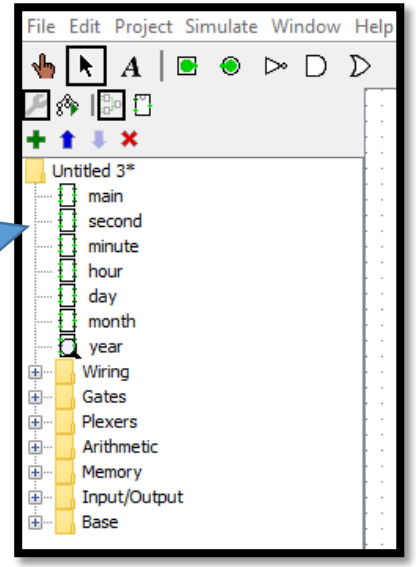
DESIGN PROCEDURES (Cont.)

6. **Design and implement the month circuit subcircuit.**

   - The year circuit section is design with four divide-by-10 synchronous decade counters that advance through there state by a HIGH logic level produce on the clock pulse that recycle the days circuit block from 31stdays in the month of December (12) to 1stday of January (01). However the Gregorian calendar has only 365 days in a normal year, and 366 days in a leap year, hence a system is also design in the years circuit block to add a day to February (that is 29 days) every 4 years and every 400 years.

- **Then Add the subcircuit to the library of LOGISIM.**

The new subcircuits added in the library of LOGISIM



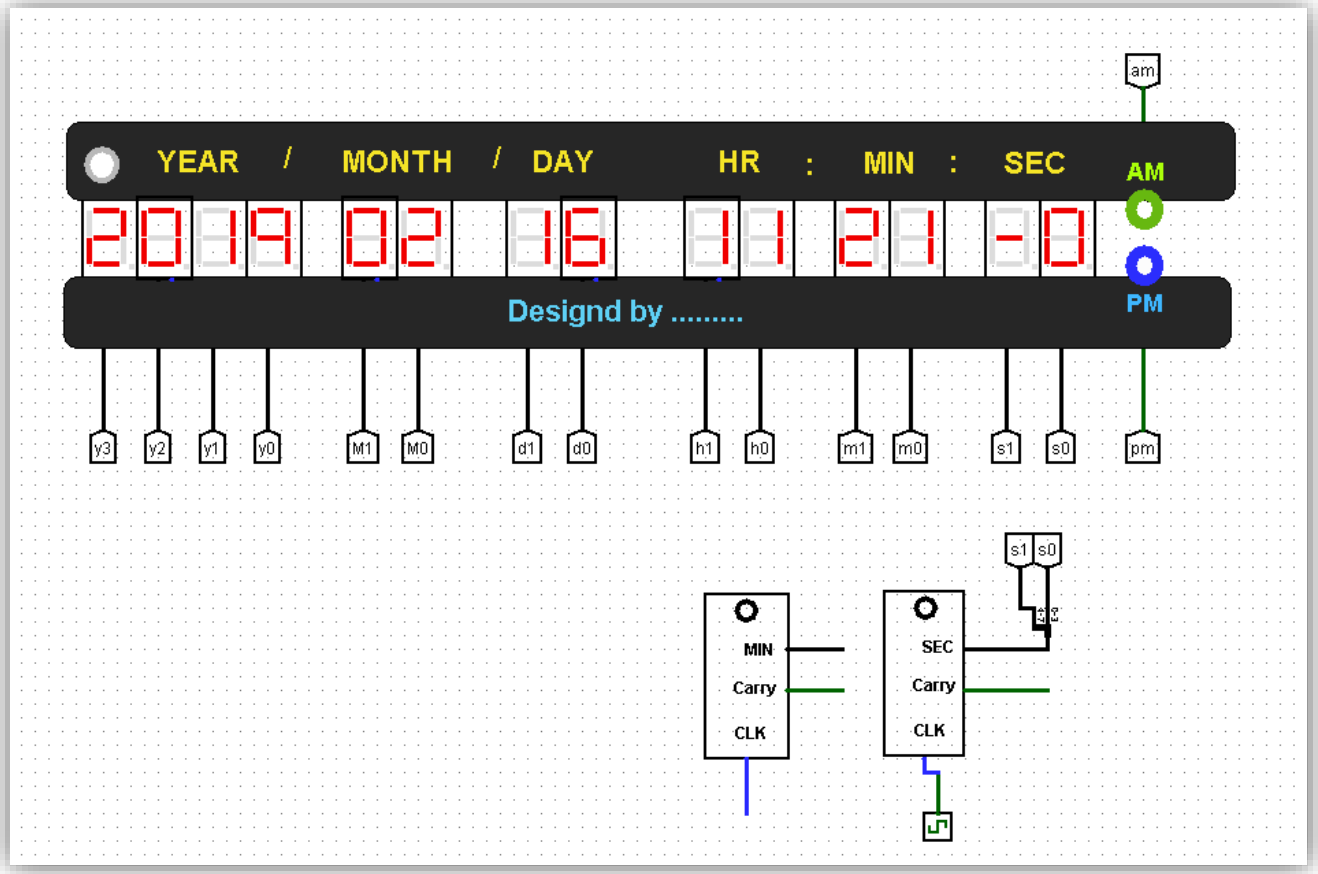
DEMO

- There is a template for the display. You can use it and connect your design to this display or you can use your own configuration.
- In this template some inputs are fixed and a digital system using build-in counters and comparators for seconds have been designed. The display should be connected to your own design and the extra elements should be removed.
- **Play** the clip below. In this clip, the frequency is changed to help you to see the changes in a faster speed, but the frequency should be 1 HZ.

Play this video for more details.

DEMO (Cont.)

- The layout of the subcircuits could be like the subcircuits below. The final design should be completed by
  - adding the other required subcircuits,
  - digital circuit for controlling the subcircuits, and
  - Connecting them to the display.



SUBMISSION

1. A . circ file named Yourname_DigitalClock.circ
2. A report (Yourname_DigitalClock.doc or Yourname_DigitalClock.pdf) explaining the process of designing. Your report should have enough details such as truth table, state table, state diagram, block diagram or everything that you used for the design and implementation.

Recommended Recourses

- The Text (Digital Design by M. Morris Mano)
- Logisim Help
- Design, Implementation and Simulation of 12/24 Hours Digital Clock

- YouTube Resources:
  - Link1
  - Link2

- Please see me or TAs if you need any question or help.