VIETNAM NATIONAL UNIVERSITY

HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

ANALOG MIXED SIGNAL IC DESIGN

Implementing a low-voltage through a Bandgap Reference by applying OTA Miller's methodology in TSMC 65nm Technology

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ABSTRACT

A basic element that is necessary for many analog and digital circuit designs is the bandgap reference block. The reference block's most crucial function is to produce a direct current or constant-value voltage that is least susceptible to variations in the circuit brought on by noise, shifts in the voltage supply, and temperature changes in the circuit under various operating conditions. A typical application for reference voltages is in analog- to- digital conversion, where the input voltage is compared to several reference levels in order to determine the corresponding digital value. The emphasis in this thesis work lies on theoretical understanding of the performance limitations as well as the design of a bandgap reference circuit, BGR.

One of the most used topologies of CMOS Bandgap Voltage References (BGR) is that one with operational amplifier (op-amp), current source, three resistors and two parasitic bipolar transistors. Besides the simplicity and good performance achieved by this BGR, this topology can be easily modified to achieve high-accuracy. Since this article using OTA Miller topology [1] and methodology to optimize the Bandgap Circuit would be declared, the main purpose of this is to deal with design of the Miller CMOS Active Conductivity The amplifier (OTA) uses a design-based approach gm/ID characteristics with early voltage (VA) to optimize energy consumption are studied by the article [1]. Furthermore, the bandgap reference block also clarifies the accuracy of constant power regulation over temperature variations, in order to provide analog circuits. This study suggests implementing a reference block with a low-power circuit topology using 65nm CMOS technology from TSMC. The block is expected to operate stable at 1.8V power supply and have a 54dB source noise cancellation coefficient. The circuit operates in the temperature range of -40 to 135 degrees Celsius, producing an output value of 1.2V with a dependence coefficient of just 6ppm/°C. From there, compare the development and which points are more optimal than the designs set out in the articles [2], [3], [4].

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I. INTRODUCTION

The reference voltage set is extremely important in the world of analog ICs, especially acting as the power supply for most electrical elements in the circuit. Why does it have so much influence? This is because BGR gives the circuit a stable current source without much error, thus making the blocks in the circuit easier to control the difference and more accurate for engineers. It is important to know that in reality, conventional sources are easily affected to a greater or lesser extent by many external factors, such as PVT - Pressure, Voltage and Temperature. In this research article, we will clarify how the above factors affect the circuit and how to adjust it through BGR. There, BGR will solve the problem being encountered.

In this study, the main goal to be achieved is to clarify and analyze the Bandgap Reference block whose Topology is provided in the document [6], the Topology of the Miller OTA amplifier used in the article [1]. Combine them using 65nm CMOS core technology provided by the TSMC65nm library. With harvest results at 6ppm/°C in the temperature range from 40-180°C when processed at a power supply voltage of 1.8V.

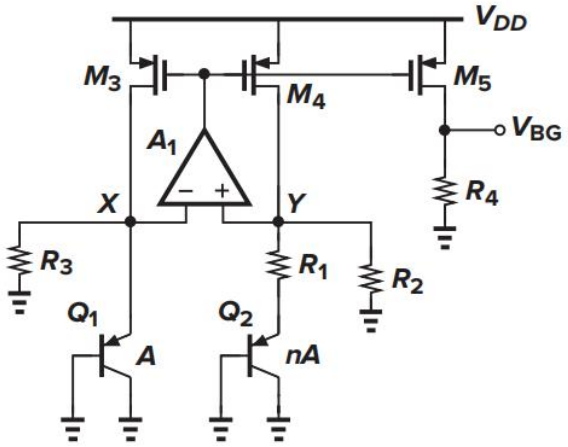


Figure 1. BGR topology [1]

II. PROPOSED BANDGAP REFERENCE

To be able to understand the structure and features of Bandgap circuits, this article will highlight some concepts that need to be clarified. To create a stable reference voltage source, the design will use two opposite quantities of temperature dependent variables PTAT and CTAT. With PTAT, the quantity is proportional to the

temperature variable, meaning that as the temperature increases, this quantity will also increase; CTAT has the opposite meaning, when the temperature increases, the amount of CTAT will decrease. When placing these two quantities close to each other, we have the idea of making them equal in order to achieve their sum equal to a quantity with a change close to 0 respected to the change in Temperature. Two opposite-TC voltages can be achieved by using temperature characteristics of bipolar junction transistors, as discussed in reference [6].

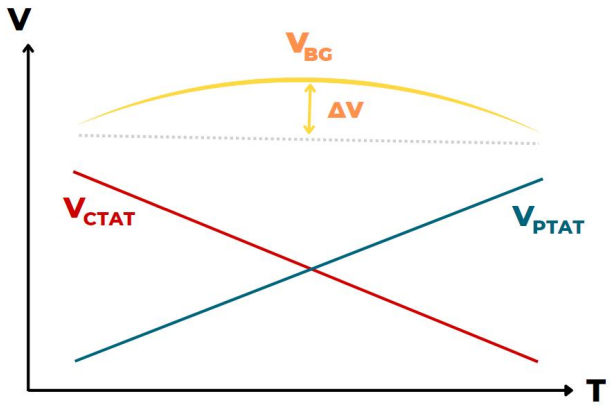


Figure 2. Constant voltage design idea on BGR

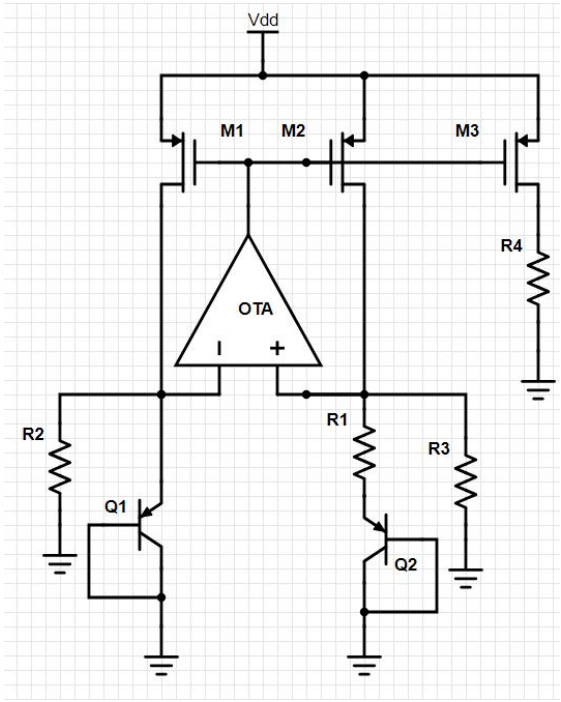


Figure 3. Complete circuit of the proposed bandgap reference

The curves are in opposite directions to effectively reduce the temperature deviation of the reference voltage. Detailed fundamentals and the proposed bandgap reference analysis is described as follows.

III. THEORY AND CALCULATION

Regarding the theory of the Bandgap circuit, we will rely on the topology from Fig. 1, through which through document [6], we can deduce that there is a Specification table of the reference circuit as Figure 4. For the purpose of this article, the voltage reference circuit will adjust the output VBG voltage to 1.2V with an error of only ± 5% (1.14-1.26V), then the IBG will also be achieved in the range from [40;60] on the temperature range -40-135 degrees Celsius. Thus, through Spec it can be seen that the VBG voltage will operate stably in the time domain, meeting the initially set needs of the Bandgap circuit. . It needs to be said that the minimum Gain used in the op-amp circuit must be 40dB, the ideal Phase Margin level is also 60deg. So it can be seen that this specification will meet a complete Bandgap circuit from the output voltage and output current.

Parameters	**Unit**	**Specifications**		
		Min	Typ	Max
Supply Voltage	V	1.62	1.8	1.98
Temperature	°C	-40	25	125
MOS	N/A	SS, TT, FF		
Output Current (IBG)	uA	40	50	60
Output Voltage (VBG)	V	1.14	1.2	1.26
Temperature Coffience	ppm/C			60
PSRR @1kHz	dB			-40
DC Gain	dB	40		
Phase Margin	deg	60		

Figure 4. Specifications of the BGR

Regarding the amplifier used in the circuit, it can be seen that the use of Op-Amp in BGR is extremely important and therefore the Specification of OP-AMP also needs

to be carefully considered, so that the output results are as expected. want. Based on the article [7], can be seen that the OTA circuit has a small Slew rate, low noise and Gain meets the Specification in Fig. 4 mentioned. In particular, the OTA circuit can apply the CMOS gm/iD size design method to make it convenient for engineers. Apply the OTA circuit researched in the article [1], based on Miller's OTA topology to design on the CMOS TSMC65nm lib. The specification for this paper can be deduced as Fig. 6.

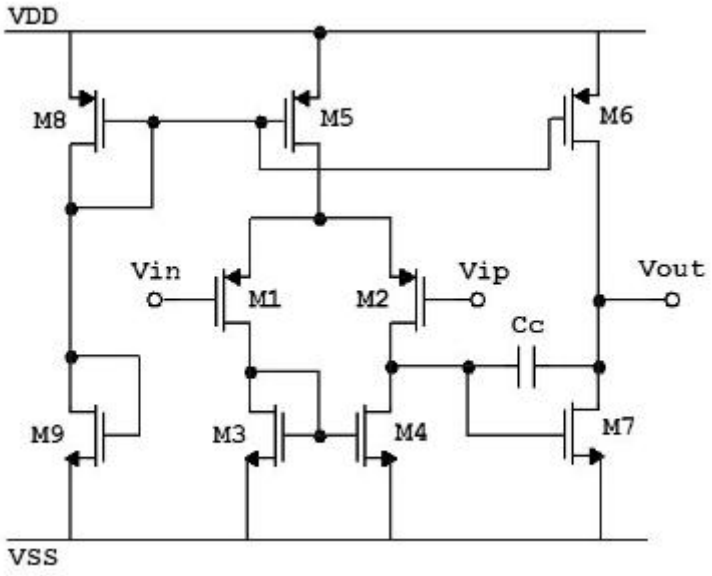


Figure 5. Miller's OTA topology

Parameters	Specs
Av (dB)	>40
PM (deg)	60
PSRR @1kHz (dB)	-40
GBW (MHz)	30

Figure 6. Specifications of the Miller's OTA topology

A. BANDGAP CORE

The BGR reference voltage theoretically applies the summation property of the Op-Amp to produce a stable output regulated by equivalent input values. Here, the input value is defined as the voltage of the bipolar transistor BJT.

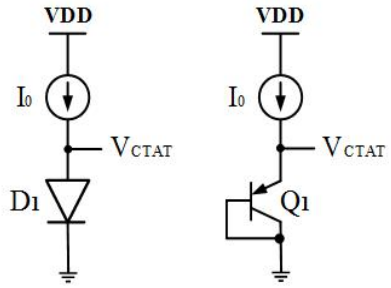


Figure 7. BJT the emitter–base junction voltage V_{BE1}

NAs stated above, the main design idea of the reference voltage is the sum of two required quantities: PTAT (a quantity proportional to temperature) and CTAT (a quantity inversely proportional to the variation of temperature). temperature). Temporarily deduce the main formula V_{BG} as follows:

$$V_{BG} = \alpha_1 V_{CTAT} + \alpha_2 V_{PTAT}$$

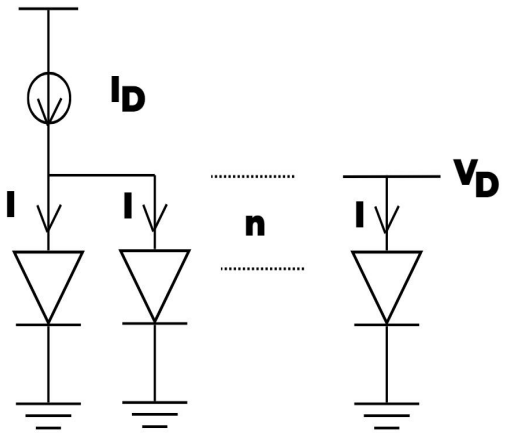
With BJT, it will automatically create a voltage value - a quantity that depends on the thermal voltage V_T (known as V_T = kT/q), is clearly shown in the formula for calculating the input current voltage V_{BE}.

$$V_{BE} = V_T \ln(\frac{I_C}{I_S})$$

Thus, we can completely determine that v_{BE} is a CTAT quantity that needs to be calculated based on design concept requirements. So the value of V_{BE} are affected by temperature V_T is also a PTAT quantity, however most of the above voltage values are more influenced by the multiplier behind it due to $I_S \prec bT$.

Based on the properties of natural logarithm, the design idea used to create the required PTAT quantity is as follows. The main thing is to use BJT in the remaining branch of Bandgap Core, but the way to eliminate the strong influence of CTAT index from V_{BE} to elimination I_S. This can apply the difference between two Napierian

Logarithm numbers to realize the design intention. Take V_{BE2} as the voltage value generated in the remaining branch of the Bandgap Core.



$$I = I_S e^{\frac{V_D}{V_T}} \quad (1)$$

$$I_D = nI \quad (2)$$

$$I_D = nI_S e^{\frac{V_D}{V_T}} \quad (3)$$

$$V_{D1} = ln(I_D/nI_S) \quad (4)$$

$$\Delta V_{BE} = V_{BE} - V_{BE1} = V_T ln(n) \quad (5)$$

Figure 8. PTAT generation by fomulas

As the formulas have been filled in above the image of the remaining branch of Bandgap Core - where it is necessary to create an equivalent quantity with a change proportional to time to compensate against CTAT. To get the log difference value, the design needs to connect the BJTs in parallel as shown in Figure 4. The experiment yields the ID current value equal to n times the value of the current entering the BJT (2). Then, imagine that the branch's VBE2 value is also equal to VTln(n) (5). Then, the obtained VBE2 is a PTAT quantity, with VT and ln(n) being constants according to n equal to the number of BJTs connected in parallel in the branch. In addition, the thermal variation of this voltage will also increase significantly as n increases. In theory, the proposed problem has the result that the two quantities CTAT and PTAT are formed in both opposing branches in the circuit. However, adding them together may not immediately create a VBG with ~ zero variation over a changing temperature range. But this article needs to consider a number of factors.

First, it is possible to know the exact gain or loss from the VBE output of the BJT in branch X through the measurement setup on the ADE-L with a temperature range of -40-135°C as follows. Give the BJT a source of vdd = 1.8V and set the current source to 50uA. It is known that with the formula of VBE of BJT, the obtained result will be equal VT x ln(IC/IS).

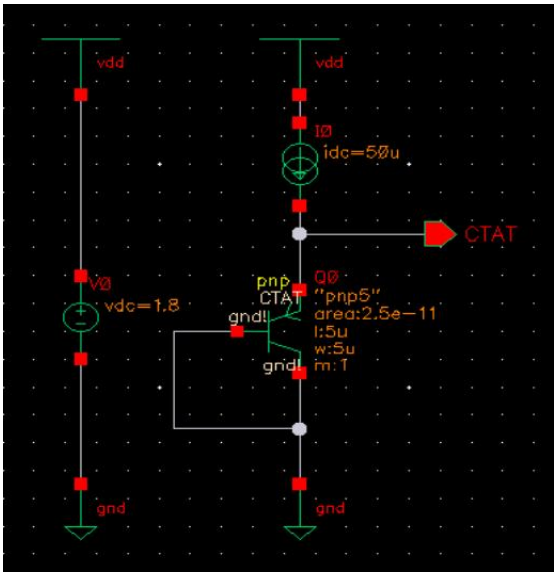


Figure 9. BJT circuit to generate CTAT (Complementary to Absolute Temperature)

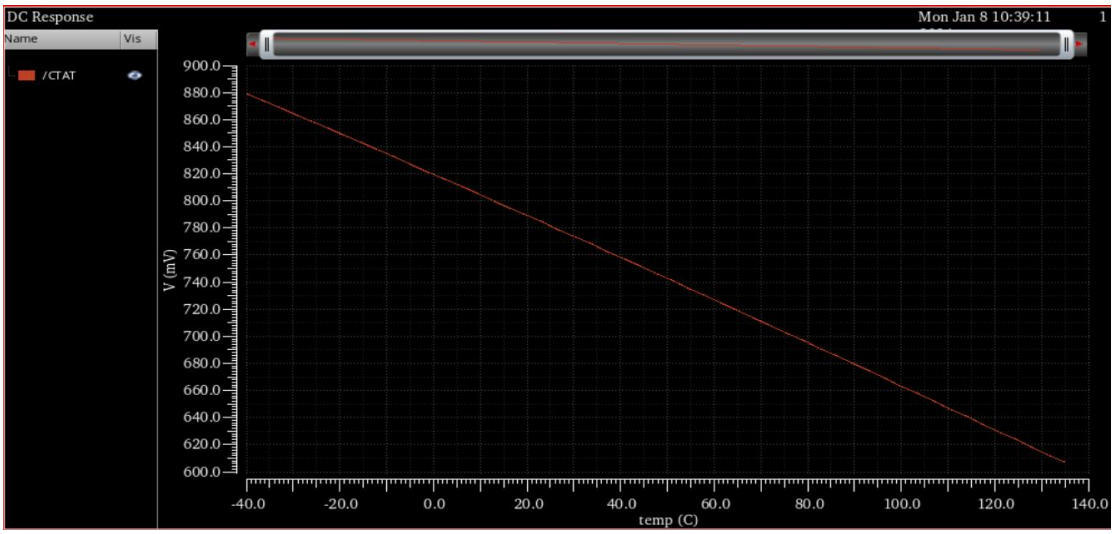


Figure 10. V_{BE}**-** Temperature graph from CTAT of BJT circuit

We obtain the value of VBE respects to Temperature as the Table given below:

V_{BE}	*Temperature*
879.739mV	-40
782.02mV	25
607.48mV	135

We have the equation of:

$$\frac{\delta v_{BE}}{\delta T} \approx \frac{\Delta v_{BE}}{\Delta T} (1)$$

Calculating the equation follow the table is given above:

$$\frac{\delta v_{BE}}{\delta T} \approx \frac{v_{BE3} - v_{BE1}}{T3 - T1}$$
$$\approx \frac{607.49mV - 879.739mV}{135 - (-40)}$$
$$\approx -1,556mV/o_C \ (2)$$

With the negative- and positive-TC voltages obtained above, we can now develop a reference that has a nominally zero temperature coefficient. We write:

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 V_T \ln(n) \ (3)$$

Derivative both side with respect to Temperature, we have:

$$\frac{\delta V_{REF}}{\delta T} = \alpha_1 \frac{\delta V_{BE}}{\delta T} + \alpha_2 \frac{\delta V_T}{\delta T} \ (4)$$

So we want the Voltage Reference should be constant even if any component appears in this equation changed, the $\frac{\delta V_{REF}}{\delta T}$ has to equal to Zero. While $\frac{\delta v_{BE}}{\delta T}$ has proven above (1) and $\frac{\delta V_T}{\delta T} = 0.087mV/o_C$

$$0 = \alpha_1(-1,556mV/o_C) + \alpha_2(0.087mV/o_C)$$
$$\Rightarrow \alpha_2 = 17.788 \approx 18 \ (5)$$

So from the above formula, we can easily calculate the alpha 2 amplification coefficient of the equation. From there, we can easily continue to calculate the corresponding resistance values.

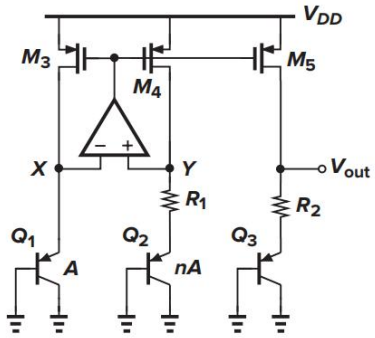


Figure 11. Generation of a temperature-independent voltage.

From the Figure 5 - describes the process of creating PTAT for V_{REF} becoming Temperature-independence, we also find out the formula for V_{REF} as:

$$V_{REF} = |V_{BE3}| + \frac{R_2}{R_1} V_T \ln n$$

Meanwhile, the value α_2 plays a role in this equation as a constant coefficient, where V_T is a coefficient that changes with temperature, so we can use $\frac{R_2}{R_1}\ln(n)$ as an α_2 amplification factor for the equation. Choose n = 8, for layout reason as the simulation Figure 6. So we can substitute the existing values to find the ratio value of $\frac{R_2}{R_1}$. From (5), we have:

$$\frac{R_2}{R_1} = \frac{\alpha_2}{ln(n)} = \frac{18}{ln(8)} = 9 \quad (6)$$

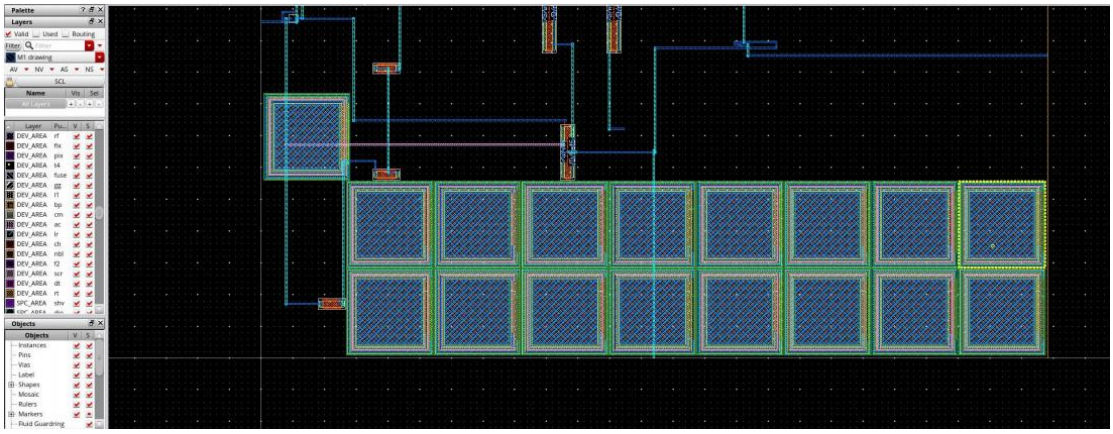


Figure 12. BJT Layout from Ajay Kumar-Gandi. Bandgap Reference

Based on the topology of the BGR, we can see that the legs of the Op Amp include X and Y. With the desire to adjust the output voltage to a low value of approximately 1.2V, the idea here is to install resistors to control the voltage. voltage at VBE of BJT like Figure 7. However, this will cause problems in the behavior of PTAT if the line $I_{C1} \neq I_{C2}$. To solve this problem, we have the idea of connecting 2 resistors to the X and Y pins instead of the above method. We observe that $V_X \approx V_Y \approx V_{BE}$ so I_{D3} should equals to I_{D4}. Thus,

$$I_{C1} + \frac{|V_{BE1}|}{R_3} = I_{C2} + \frac{|V_{BE1}|}{R_2}$$

In order to have $I_{C1} = I_{C2}$, also R2 should equals to R3. We have $V_{BE1} = V_{BE2} + I_{C2}R2$ when $I_{C2} = \frac{PTAT}{R_2} = \frac{V_T ln(n)}{R_2}$. Having equations from BGR topology $V_{BG} = I_{D4} \times R_4$ (7) and assuming that M3, M4, M5 are similar.

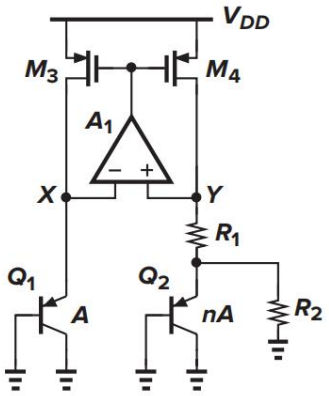


Figure 13. Placing a resistor in parallel with Q2

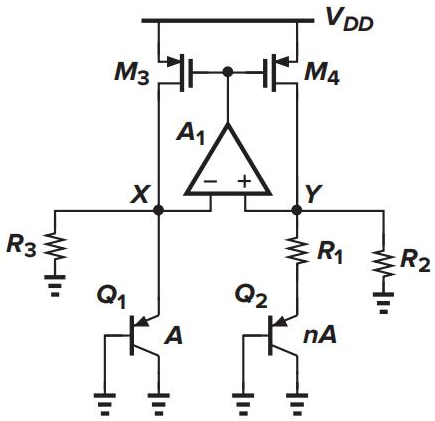


Figure 14. R2, R3 connects to X,Y which are parallel to Q1, Q2

This current and the current flowing through R_2, V_{BE1}/R_2, constitute I_{D4} at point Y:

$$\begin{aligned} I_{D4} &= \frac{V_T ln(n)}{R_1} + \frac{V_{BE}}{R_2} \\ &= \frac{1}{R_2}(\frac{R_2}{R_1} V_T \ln n + V_{BE}) \end{aligned}$$

From (7), we have:

$$V_{BG} = \frac{R_4}{R_2}(\frac{R_2}{R_1} V_T \ln n + V_{BE})$$

Based on the Figure (2) - the specifications of BGR, we can easily calculate R4 as:

$$R_4 = \frac{V_{BG}}{I_{BG}} = \frac{1.2V}{50uA} = 24kOhms$$

Since, we can also calculate all the value of the remained resistors:

$$\begin{aligned} R_2 &= \frac{R_4}{V_{BG}}(\frac{R_2}{R_1} V_T \ln n + V_{BE}) \\ &= \frac{24kOhms}{1.2V}(9 \times \ 26mV \times ln(8) + 782.02mV) \\ &= 25kOhms = R_3 \end{aligned}$$

From (6), we have:

$$R_1 = \frac{R_2}{9} = \frac{25kOhms}{9} = 2.8kOhms$$

Resistors	Value
R_1	*2.8 kOhms*
R_2	*25 kOhms*
R_3	*25 kOhms*
R_4	*24 kOhms*

B. OTA Miller's

First of all, it is necessary to know that the Miller Operational Transconductance Amplifier circuit design method is a special method, because: gm/ID strongly affects the size of each CMOS, greatly affecting the main operating process of the circuit. analog circuit. The normalized gm/ID ratio and current ID/(W/L) curve represent a unique characteristic for all transistors of the same type (NMOS and PMOS) in a particular technology. This "universal" quality can be exploited during the design phase when the transistor aspect ratio (W/L) is unknown. The gm/ID ratio and the Early Voltage (VA) parameter are the basic device technology relationships that determine the minimum allowable transistor length. The L of the transistor can be determined using this method. Taking into account these two aspects, the design process is divided into two main phases. First, the gm/ID vs. ID/(W/L) curve is used to determine each transistor's W/L.The transistor lengths (L) are then calculated taking the gm/ID vs. VA curve into account.

Consider getting Phase Margin equal to 60 deg => capacitor in OTA must be equal or higher than 1.9pF [1]. This will mean that the Gain Bandwidth reaches 30 as the Spec set in Figure 1. Next, there are two steps to consider when designing the transistor size as follows. In the first design phase, choose W/L for each transistor. Based on the implementation of [8], we choose the ratio of gm/iD and calculate ID/(W/L), identifying each transistor. semiconductor via gm/ID vs ID/(W/L) curve.

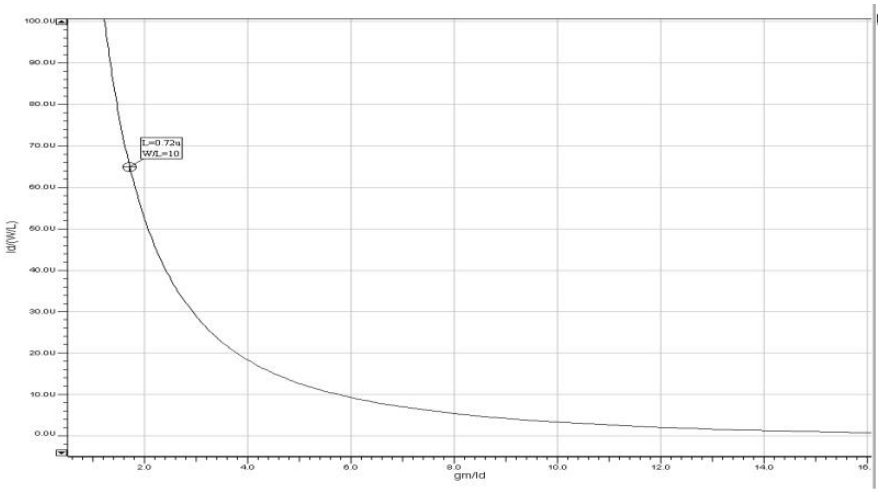


Figure 15. ID/(W/L) Vs gm/ID curve example from [8]

The remaining design phase will aim to choose the transistor length L to determine the design size through the curve between the gm/ID ratio and the advance voltage (VA). Design criteria and gm/ID values from The previous design phase can be used to determine the lowest allowed transistor length. The stage DC gain and output resistance of the transistor are closely correlated with the VA parameter.

Devices	W/L ratio	W	L
M1	30	30µm	1µm
M2	30	30µm	1µm
M3	108	108µm	1µm
M4	35	107µm	3µm
M5	35	107µm	3µm
M6	0.25	1µm	4µm
M7	10	6µm	0.6µm
M8	0.25	1µm	4µm
M9	10	6µm	0.6µm

IV. SIMULATION AND COMPARISON RESULTS

The article is based on TSMC's 65nm CMOS core technology. Simulating the product on the Cadence application will provide a clearer perspective on the implementation process and simulation results for engineers to make adjustments. based on professional knowledge. For the article on the topic of a reference voltage regulator circuit from the power supply, the purpose will be to conduct simulations and comparisons based on available article topics [2], [3], [4] and give comments on the optimal and sub-optimal levels of the circuit. The bandgap circuit that is implemented depends a lot on the amplifier being added. To see if the simulation is

really accurate or not, it is necessary to closely follow the parameters on the specification sheet in Figure 6. First, make their principle diagram based on OTA's Miller topology as shown in Fig. 16 below. Consider making a circuit and powering the circuit with 2 VDC sources with values approximately equal to the values of CTAT and PTAT proven and calculated in part III. Also, make sure that every single CMOS operate in saturation.

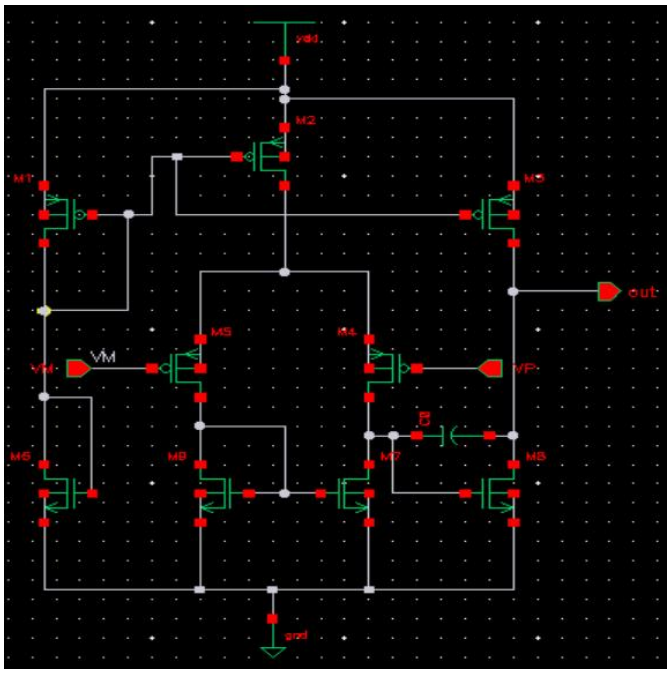


Figure 16. The Miller's OTA topology schematic

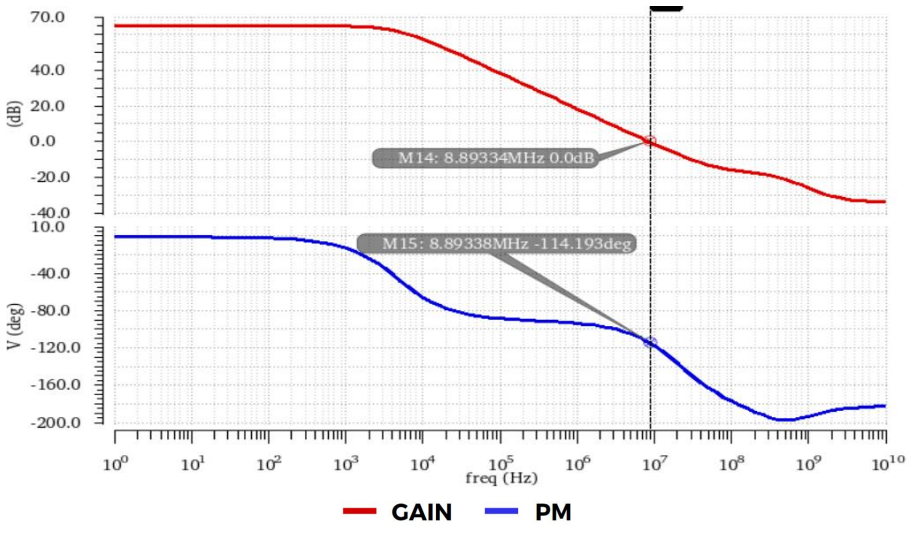


Figure 17. Gain and Phase Margin of OTA Miller

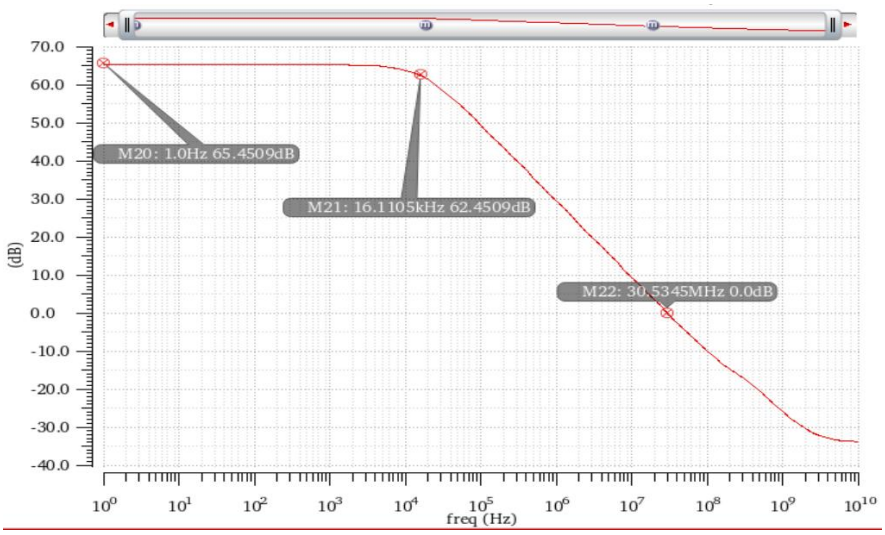


Figure 18. Gain and 3-dB Bandwidth of OTA

From the simulations Fig. 16-18, the results can be sum like the figure below.

	Unit	Value
Gain Av	dB	65.45dB
Phase Margin	degree	60
3-dB BW	Hz	16k
GBW	Hz	30M

[OPTIONAL] Create a symbol for Operational Transconductance Amplifier Miller, with 2 inputs VINM and VINP (representing Input Minus Voltage and Input Positive Voltage respectively). Some symbols can be referenced for this set, however in this article we will draw symbols for OTA shaped like Fig. 19.

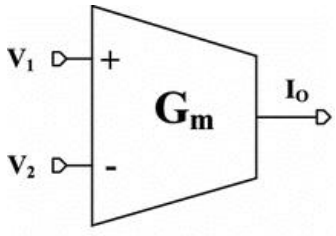


Figure 19. Operational Transconductance Amplifier Miller symbol

Connect the symbol of the OTA unit directly into the Bandgap core circuit with the positive terminal of the OTA connected to the branch containing the PTAT quantity and vice versa at the negative terminal. This is similar to the output of this set, which will be connected to the connection between the two Gate ports of the above branch circuit - which contains the Current Mirror set of 3 as shown in the principle diagram of Figure 20.

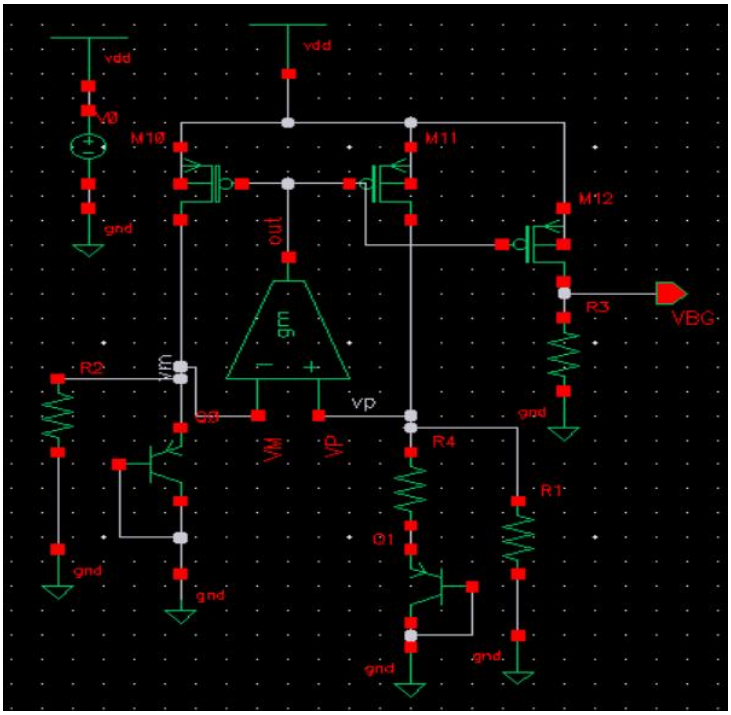


Figure 20. Complete BGR with OTA Miller

Devices	W	L
M10	110µm	16.5µm
M11	110µm	16.5µm
M12	110µm	16.5µm

Simulate the VBG value over the temperature range from -40 to 135 degrees Celsius. We get a VBG value that does not change with the change in temperature. It is known that to get that constant value, experiment It is also necessary that the result of the IBG line be in the region of 40 to 50uA. As measured, the output of this entire Bandgap circuit will be represented as shown in Fig. 21, where the signal is found to vary approximately to zero throughout the temperature range.

Additionally, the ideal VBG signal is known to have zero variation, but in reality, the VBG will be shaped like a curve, and the peak of that curve will lie at the typical temperature range (25 Celsius degree). The reason this bump forms is due to the cumulative influence of variation of base-emitter voltages, collector currents, and offset voltages. To minimize the size of the rise of the VBG signal, it is necessary to reduce the offset voltage in many ways, but the most common is to create a Trimming set, which is known to be used to adjust the electrical signal so that it Voffset is the lowest.

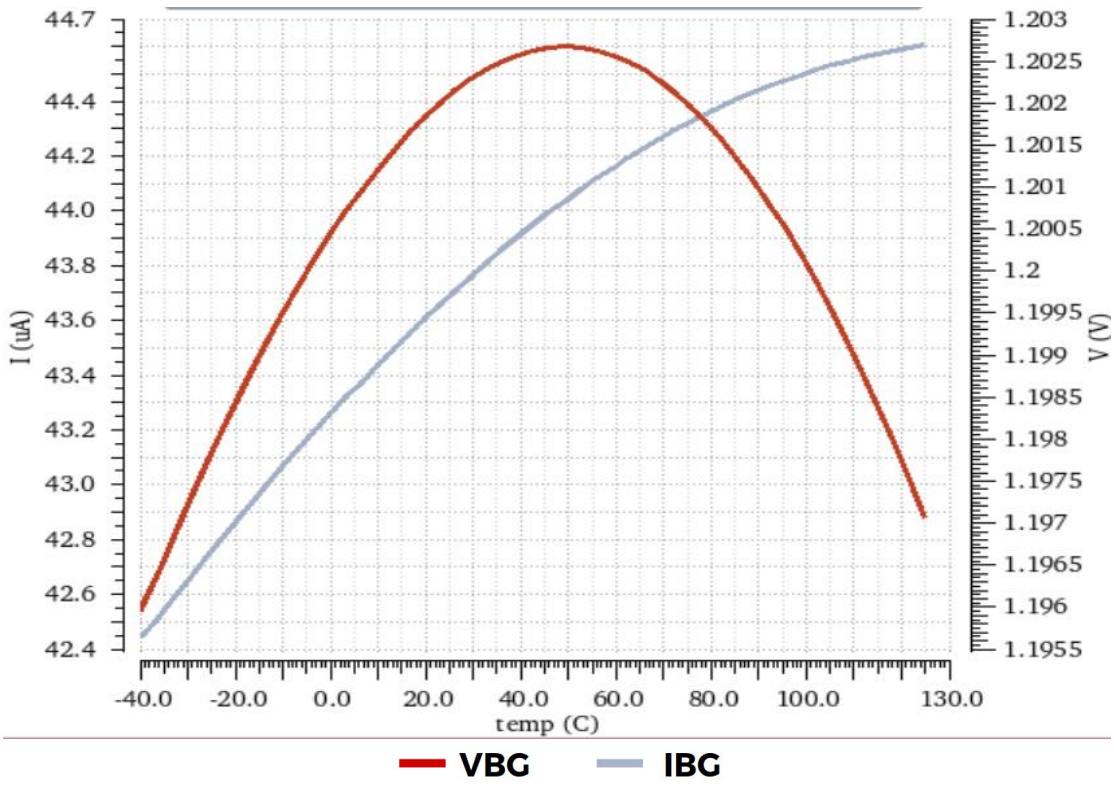


Figure 21. Bandgap Voltage and Current on Temp [-40;130]

Using the peakToPeak function in Cadence, it can be determined that the largest change found in the above simulation is about 6.71mV when the temperature reaches 50 degrees Celsius.

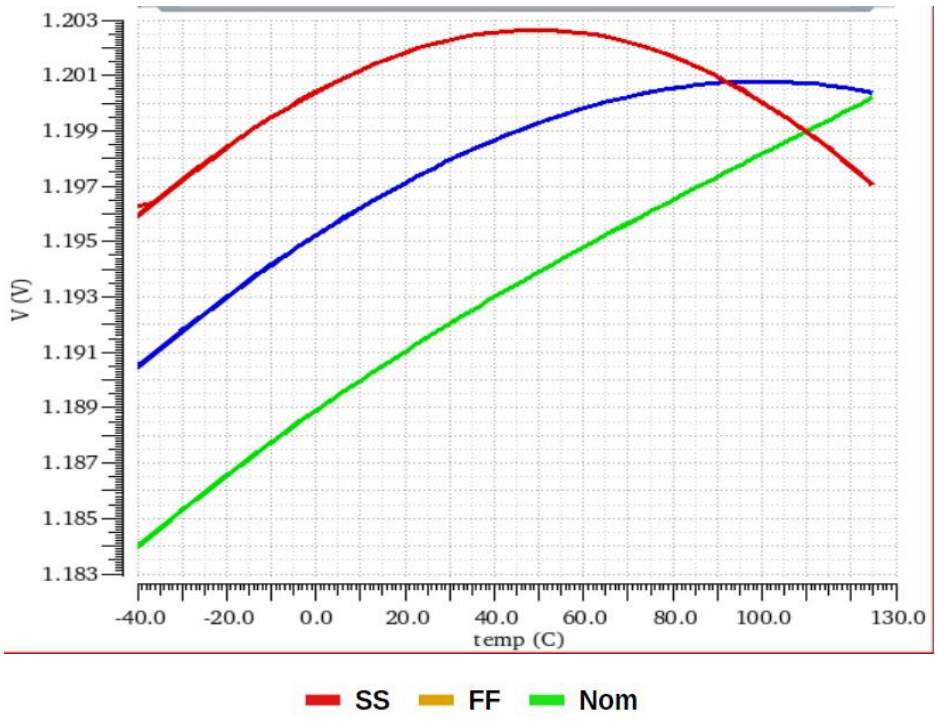


Figure 22. Bandgap Voltage on three design corners (SS, TT, FF)

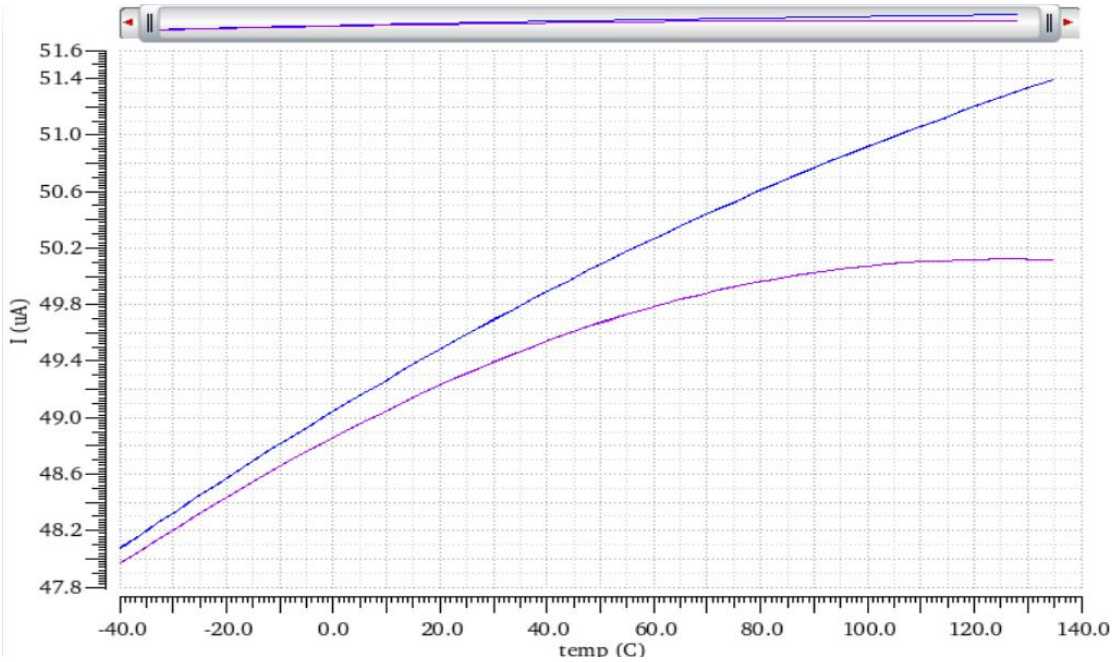


Figure 23. The diffrence between two IDs of M10 and M11 from CM

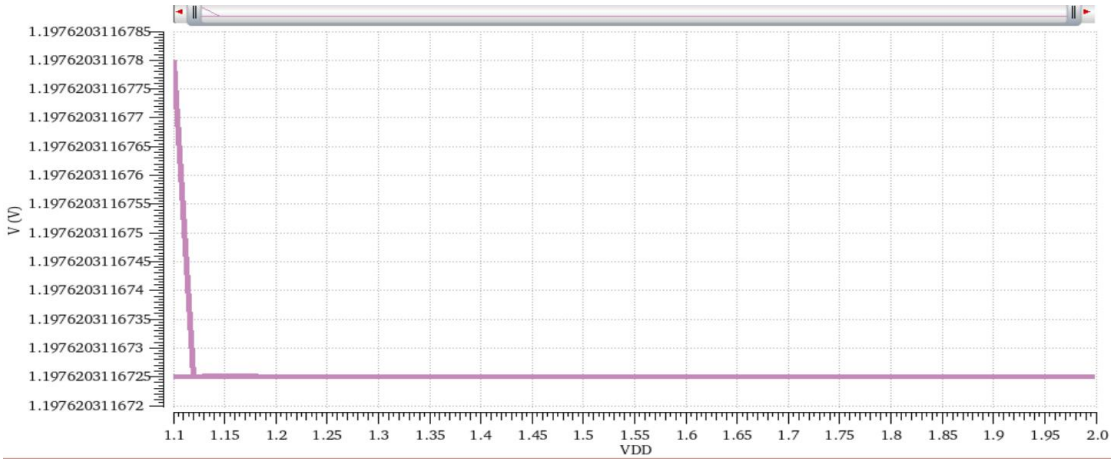


Figure 24. The diffrence between two IDs of M10 and M11 from CM

Figure 24's simulation results illustrate how the power supply voltage affects the reference voltage (VREF). Figure 11 makes it evident what the voltage value is in the voltage range of 1.1 to 2V. With extremely little variation in the reference (ΔVREF/supply voltage = 6.1pV), the source noise reduction factor (PSRR) is calculated as 20log(6.1pV) = -224.3dB.

	[2]	[3]	[4]	This work
Year	2020	2001	2020	2024
Tech Process	28nm	BiCMOS	180nm	65nm
VREF	0.6V	0.53V	0.494V	1.2V
ΔVREF	0.39mV	0.8mV	0.16mV	6.7mV
Supply Voltage	1.1- 2V	0.6- 2V	1.8V	1.8V
Temperature	[-40; 105]	[0; 80]	[-40; 140]	[-40; 135]
PSRR	-54	N/A	-68	-224dB
Trimming	YES	NO	NO	NO
Phase Margin	N/A	63	N/A	60

Figure 25. Synthesize and compare research result

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