CMOS 28 nm Fully On-Chip wideband Circulator IC

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***Abstract*— Herein, we verify the CMOS non-magnetic non-reciprocal passive circulator based on 4-path staggered commutation network that can break Lorentz reciprocity and replace ferrite-based circulator used for decades in history of wireless communication. The circulator prototype is designed in Samsung 28nm RF process, operated at 2.16 GHz, which exhibits 5 dB of loss in the transmitter-antenna (TX-ANT), 6.6 dB in the antenna-receiver (ANT-RX) path and has high isolation (TX-RX) up to 40 dB at single frequency of 2.16 GHz. To extend bandwidth of operation, we propose 3 on-chip branches of negative capacitor circuit (NCAP) delay lines instead of passive LC network counterparts. Besides, the clock generator is integrated on chip to guarantee a very compacted design. The measured results shows that the proposed circulator can work in the bandwidth of 65 MHz from 1.985 GHz to and 2.05 GHz and suffers 6 dB, 9dB maximum in-band loss for TX-ANT, ANT-RX path respectively while the TX-RX path achieves 20 dB of minimum isolation. The circulator IC costs a die area of only 1.1 x 1 mm^2. The IC consumes 7.2 mW for clock generator part, 14.4 mW for clock divider part and 54 mW for NCAP delay lines.**

***Index Terms* — CMOS magnetic-free Circulator, NCAP, non-reciprocity, non-foster element, negative group delay (NGD).**

I. INTRODUCTION

Linear, time-invariant, passive components in electronics such as R, L, C are reciprocal due to being fabricated by conventional materials with symmetric permittivity and permeability tensors. Traditionally in wireless communication, breaking Lorentz reciprocity is implemented by using ferrite materials under the external magnetic field bias application such as being seen in circulator, isolator devices [1], [2]. Nevertheless, ferrite material- based devices are bulky and not compatible with CMOS fabrication process, significantly restrict their impact. Additionally, antenna interface (Fig.1) in Full-Duplex (FD) wireless communication/power transfer system plays an important role and can be implemented by antenna pair [3] , shared antenna interface such as the electrical balance duplexer [4], [5] or circulator [6]–[8]. Among them, duplexers and circulators are regarded as good candidates as they easily transform to MIMO and antenna diversity applications. Due to large area occupancy and high loss, the duplexer becomes less attractive to system integration.

In this study, we switch our attention to how to integrate circulator device into system effectively. As aforementioned, nonreciprocal passive circulator using ferrite material even though proves excellent performance with high linearity and low loss [6], in term of integration, it finds amenable to CMOS technology. Moreover, circulators that apply the nonreciprocal

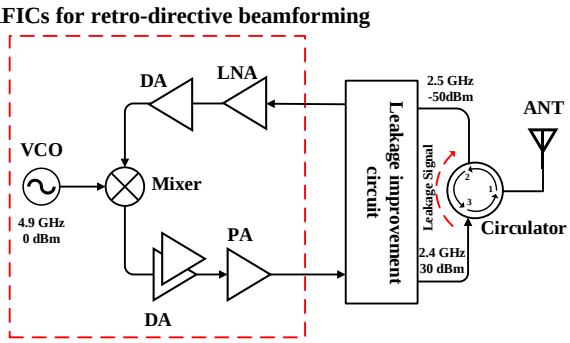


Fig.1 Antenna interface is implemented by a circulator in RF retro-directive beamforming IC for wireless power transfer application.

of active transistors [7]–[9],[10] confront the drawback of high noise and poor linearity [11]. Hence, requirement of low noise, high linearity and high TX-RX isolation circulator have still been open challenge to authors these days. Recently, there has been significant research regarding implementation of magnetic-free non-reciprocal circulators based on staggered commutation N-path network (seen as a parametric modulation with very high modulation ratio) [12]–[14] and spatio-temporal conductivity modulation [15],[16]. This study verifies the fundamental theory behind the narrow-band circulator based on staggered commutation N-path network by designing circulator fully on-chip in 28 nm RF CMOS process and propose a method of TX-RX isolation bandwidth extension for circulator IC by employing NCAP circuit [17].

II. ANALYSIS AND DESIGN

In this section, we investigate the fundamental of linear periodic time variant (LPTV) property of bandpass filter (BPF) based-gyrator in a staggered commutation network that can be conducted by a N-path switched capacitor array and how to establish a circulator circuit by employing this gyrator. Simultaneously, to tackle with limitation regarding bandwidth operation of such N-path BPF based circulator, there is a methodology of bandwidth extension given by proposing NCAP analog delay lines instead of conventional L-C network use in prior works [12]–[14].

A. LPTV Bandpass Filter Based-Gyrator

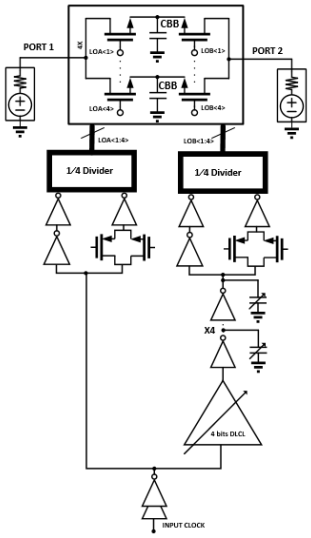


Fig.2 Non-reciprocal bandpass filter schematic (the digital controlled delay line (DCDL) and by-4 divider are not shown)

Figure 14 shows a 4-path differential 2-port BPF is designed in 28 nm RF CMOS technology. Capacitors C_{BB} is chosen to satisfy the condition of band pass filtering profile $C_{BB} \gg \frac{1}{2\pi fs.Z_0}$,. NMOS switches optimized for low resistance are driven by a 25% duty cycle 4-phase clock (LOA<1:4> and LOB<1:4>), which decides to reduce circulator insertion loss.

The complete S-parameter of a two-port 4-path BPF based gyrator at center frequency (fs) with 90^0 phase shift between the clock sets can be expressed as [13]:

$$S(fs) \approx \begin{pmatrix} sinc^2\left(\frac{\pi}{4}\right) - 1 & sinc^2\left(\frac{\pi}{4}\right) e^{-\frac{j\pi}{2}} \\ sinc^2\left(\frac{\pi}{4}\right) e^{+\frac{j\pi}{2}} & sinc^2\left(\frac{\pi}{4}\right) - 1 \end{pmatrix}$$

With noting that Z_0 is reference impedance and C_{BB} is capacitor in each commutation path.

Additionally, LOA<1:4> clocks connecting with respective switches are regarded as I/Q mixer with 90^0 phase difference and similarly, the LOB<1:4> is in an analogous regime. These 4-phase generators are achieved by employing the conventional Johnson-counter-based ¼ dividers [18] with high-speed D Flip-Flop (DFF) [19]. The clock generator is optimized for f_s= 2.4 GHz with a 9.6 GHz input clock supplied from the internal VCO. Moreover, for the staggering commutation purpose, we delay LOB<1> 90^0 versus LOA<1> thanks to the 5-bit digital controlled delay line (DCDL) [20] and inverter chains with fine-tuning cap banks as shown in Fig.2. There is a noticeable trade-off that choosing a large switch W/L will enhance the linearity and reduce loss in-band of the filter. However, the more NMOS switch sizes are, the larger the parasitic capacitors accumulate into ports. This results in a small frequency range and large clock leakage as well as requires more power to inquire sufficient skew of dividers to drive switches.

Fig. 3 shows the simulation results of the BPF based-gyrator designed. The gyrator shows a BPF lookalike magnitude response with 5.2 dB loss while the non-reciprocity in phase is given and separated at center frequency of 2.4 GHz. Nevertheless, as seen in the phase response of S21 and S12 in Fig.3, there is a nearly 180^0 phase difference ([delay LOB<1> - LOA<1>]*fs*360^0), which states firmly that the phase non-

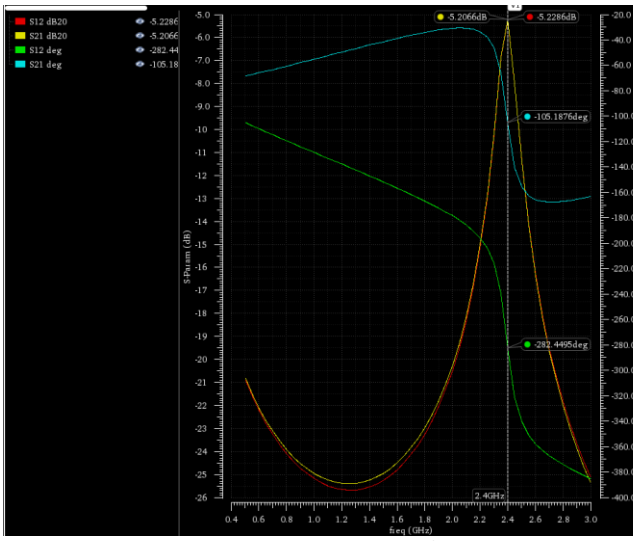


Fig.3 Magnitude and phase response of LPTV BPF

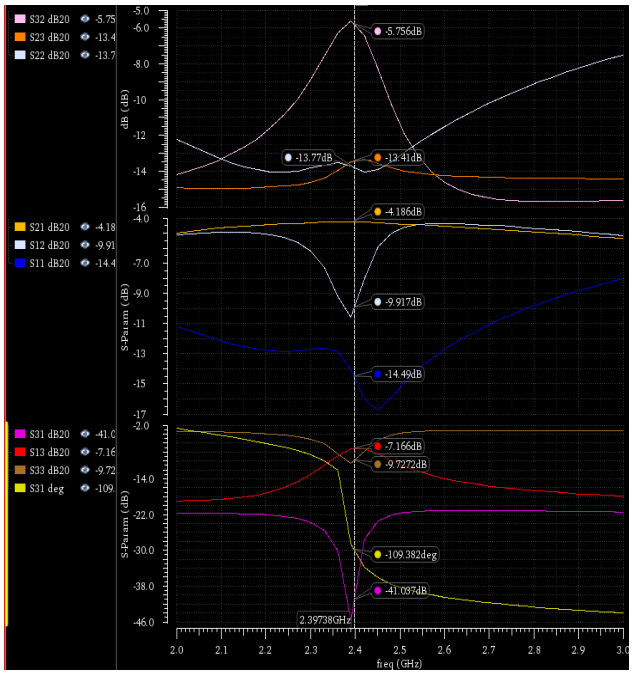


Figure 5 (a) Magnitude responses: insertion loss, isolation and matching of circulator in all ports: TX (port1), antenna (port 2), RX (port 3).

reciprocity obtained by the timing staggered commutation is true and exhibits a key obtainable result to make circulator possible in this work. The matching achieves approximate 12 dB (slightly shifts down due to parasitic capacitors contributed by switch sets) at 2.4 GHz while S21 and S12 still exhibit the reciprocal response between them.

B. Integrated Magnetic-Free Active Circulator

A standalone circulator is designed for tunable operation around 2.4 GHz in 28 nm CMOS RF. The schematic is shown in Fig.4 with the same clock paths designed in Part A. The analog delay line λ/4 is miniaturized utilizing the CLC structure (in fact acts as a high pass filter) implemented completely on-chip with MIM cap and PDK inductor (Q = 15.5, 2.8 nH). The BPF is designed with N=4 to ease burden for the clock generator circuit (increasing N inquires the larger input

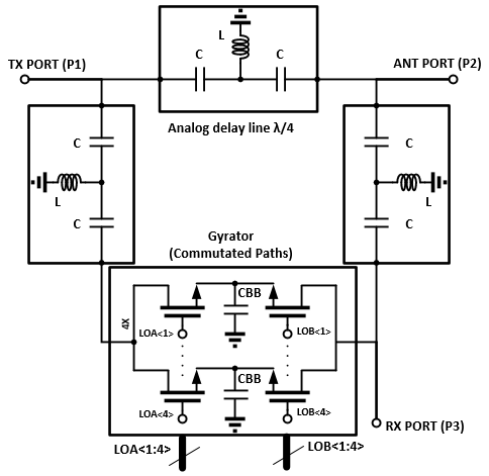


Fig. 4 Circulator schematic (clock generator circuit is not shown)

frequency clock to feed the dividers resulting in more power consumption for the same skews on the output clocks) while maintains the acceptable loss on the ANT-RX path.

In this study, non-zero loss and finite isolation between forward and reserve path in circulator topology are unavoidable because of finite number of path (N) in commutation network and the inherent non-zero resistor of CMOS switches (R_{sw}). these loss can be formulated for each forward path as following: [13].

TX – ANT path loss: $S_{21} = -\frac{jZ_0}{Z_0+R_{sw}}$ (1)

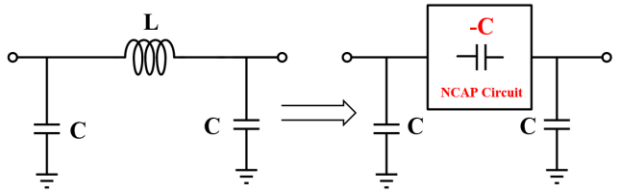
ANT- RX path loss: $S_{32} = -\frac{jZ_0\left(1+\left(\frac{1}{\alpha}-1\right)\left(\frac{R_{sw}}{Z_0}\right)\right)}{\left(Z_0+\left(\frac{1}{\alpha}-1\right)(Z_0+R_{sw})\right)}$ (2)

TX – RX path loss: $S_{31} = \frac{-R_{sw}Z_0\left(\frac{1}{\alpha}-1\right)}{(Z_0+R_{sw})\left(Z_0+\left(\frac{1}{\alpha}-1\right)(Z_0+R_{sw})\right)}$ (3)

Where $\alpha = sinc^2\left(\frac{\pi}{4}\right)$

The simulated S-parameters of circulator are presented in Fig.5 with port assignment as followed: TX: port 1, ANT: port 2 and RX: port 3 when all assigned ports are terminated with 50 Ω. At the center frequency fs = 2.4 GHz, the TX-ANT path in Fig.4 expresses a narrowband operation and suffers around 4.2 dB of loss (S21) while the isolation (S12) of around 10 dB is obtained between them. The ANT-RX path (S32) exhibits a filtering profile analogous to the BPF property in Part A with a minimum loss of 5.8 dB at 2.4 GHz (Fig.5 top part) and isolation (S23) of approximately 14 dB. The circulator shows a TX-RX isolation (S31) better than 40 dB between port 1 and 3, which manifests itself in significantly cancelling leakage power interference from TX to RX port.

C. NCAP delay lines proposal for wideband operation



(a) (b)

Fig.6 (a) LPF analog delay λ/4 (b) L is replaced by NCAP for negative group delay λ/4 transmission line

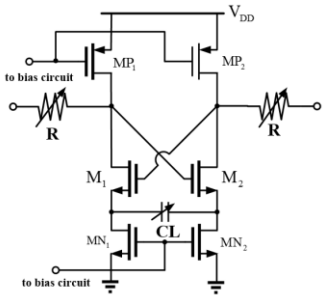


Fig. 7 NCAP-D circuit for the proposed delay line λ/4

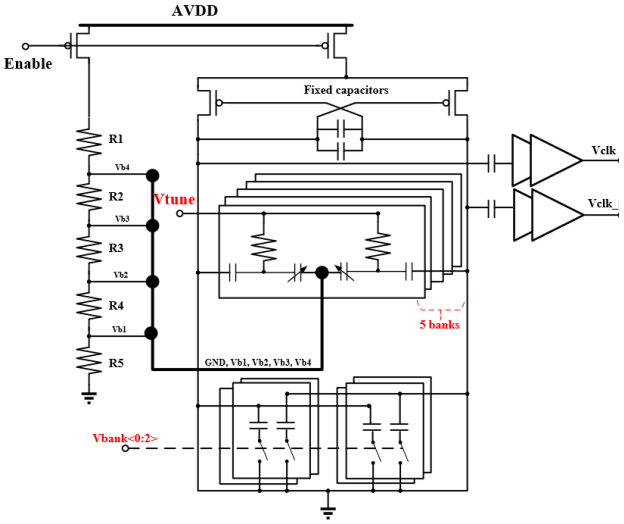


Fig.8 VCO 9.6 GHz circuit with 5 voltage levels for varactor trimming and 3-bit capacitor banks

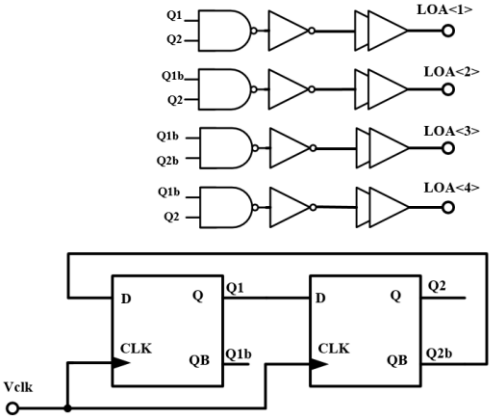


Fig.9 Johnson by-4 divider schematic (90^0 output phase difference)

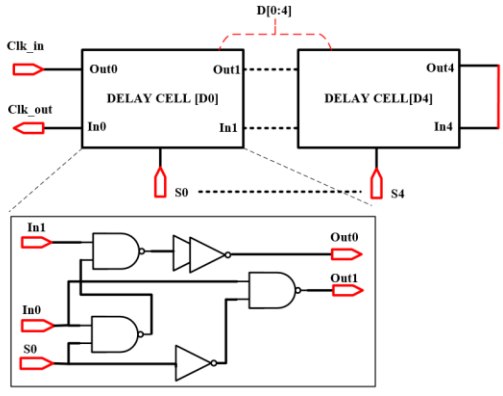


Fig. 10 5-bit Digital Controlled Delay Line Cells

First of all, to extend bandwidth of circulator, the 3 arms CLC high-pass network in Fig.4 are established under LPF structure (Fig. 6. (a)) such that their cut-off frequency are significantly greater than center frequency of circulator (2.4 GHz). Second, the principle of wideband operation is that to cancel positive group delay of gyrator, we insert a negative group delay non-foster element NCAP[21]. As a result, NCAP delay lines with negative group delay are able to cancel the positive group delay (PGD) counterpart produced by gyrators and make circulator magnitude response become widen in the bandwidth of interest. To mitigate the NCAP loss impact over loss of all proposed structure, the NCAP circuit with 2 symmetrical ports at drain terminals (Fig. 7) is employed in this study [17] at the cost of a deliberate stability consideration in sizing the circuit. Resistors are considered to compensate for negative resistance generated from cross-couple NMOS pair, which decides the overall circuit stability and insertion loss of NCAP circuit. Generally, this R is assigned to be tunability and greater than 1/gm. Otherwise, to provide NGD tunability for C_L, this component is also designed in 4 controllable banks for compensating the process variation.

III. IMPLEMENTATION AND MEASUREMENT RESULT

A. Integrated Narrowband and Wideband Magnetic-free Circulator IC.

First, the narrowband circulator is verified. The CLC structure in Fig.4 is implemented by PDK components, which C is assigned to MIM capacitor of 20 pF, L is located at highest layer of process with Q = 15.5 and L = 2.8 nH at 2.4 GHz. For staggered commutation network, the number of paths is chosen to 4 to release burden for clock divider circuit (straightforward layout requirement in clock paths) and clock generator circuit (= fs*N). The ON/OFF switch size is 200 u/0.1 u designed with thick gate oxide device to increase the power capability handle of circulator and result in small circulator insertion loss while guaranteeing the small contribution of parasitic capacitors accumulated at ports in circuit.

For a compactable design, the clock generator (input clock source in Fig.2) is designed fully on chip. Fig. 8 shows voltage control oscillator (VCO) circuit working at 9.6 GHz, which can provide a wide tuning range of 430 MHz and phase noise of -107 dBc/Hz at 1 MHz offset. The wide tuning capability is possible thanks to 5 voltage levels applied to the varactor arrays and 3-bit digital control for course tunning capacitor banks (Fig. 8). For staggered commutation operation of gyrator, the phase difference between LOA<1:4> and LOB<1:4> is chosen to be 90^0 and the Johnson divider in Fig.9 is a typical candidate to implement such idea with high-speed D-FFs employed. Standard cells in Fig.9 should be highly deliberately layout designed to optimize clock path parasitic for clock skew reduction and signal strength conversation at center frequency 2.4 GHz. The need for phase difference 90^0 between clock paths (LOA<1> and LOB<1>, LOA<2> and LOB<2> … and so on) in commutation network is to result in phase non-reciprocity of S21 and S12 that phase splits apart at center frequency 2.4 GHz. Fig.10 shows the realization of delaying clock paths throughout 5 delay cells [D0:D4], which covers the phase tunning range of sufficient 180^0 by switching 5 bits [S0:S4] respectively.

Regarding NCAP delay lines in wideband circulator structure, the design technique from [17] is fully used for NCAP-D that supplies by VDD = 2 V, consumes a current of 9 mA. R value in Fig.7 is 9 Ω and C_L = 1.2 pF, both R, C_L components are designed in banks for tunability.

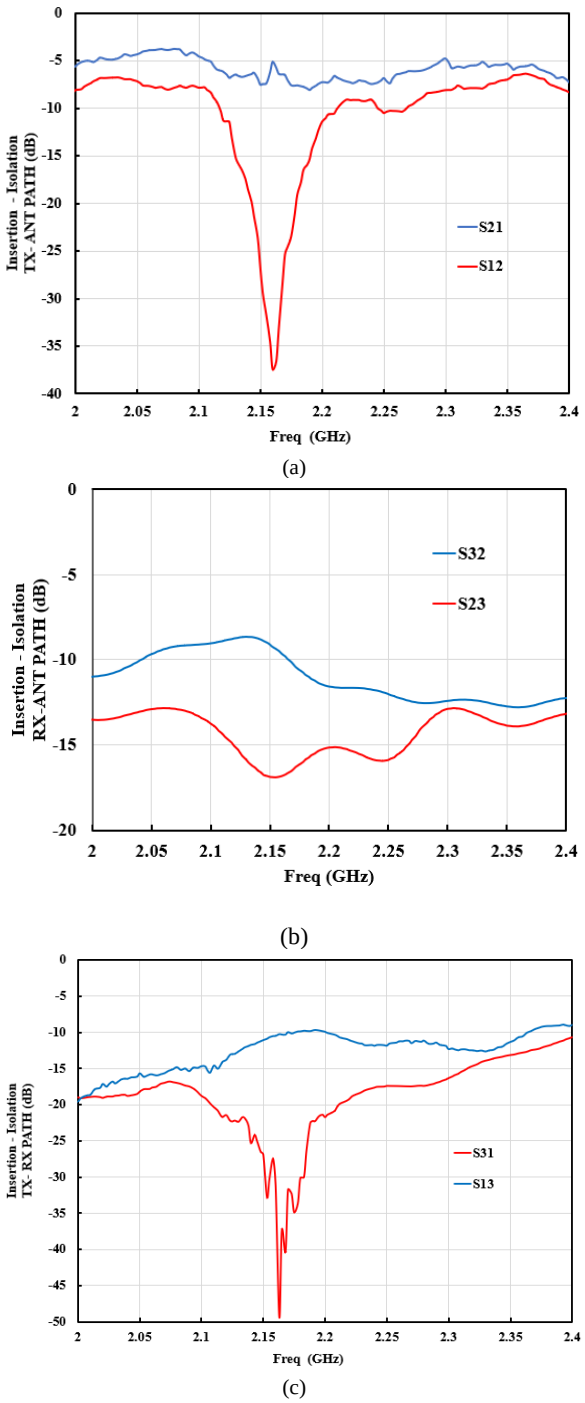
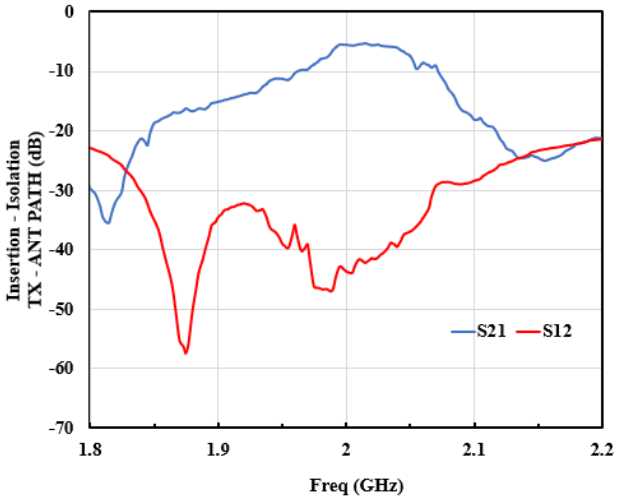


Fig. 11 Insertion and isolation measurement of 3 ports in narrow band circulator (a) TX-RX, (b) ANT- RX, (c) TX- ANT path.

B. Measurement

Fig. 11 shows the S-parameters in all ports measured in narrowband circulator prototype. The circulator exhibits 5 dB of loss in the transmitter-antenna (TX-ANT), 6.6 dB in the antenna-receiver (ANT-RX) path and has high isolation (TX-RX) up to 40 dB at single frequency of 2.16 GHz. This maximum frequency moves downward versus initial plan of 2.4



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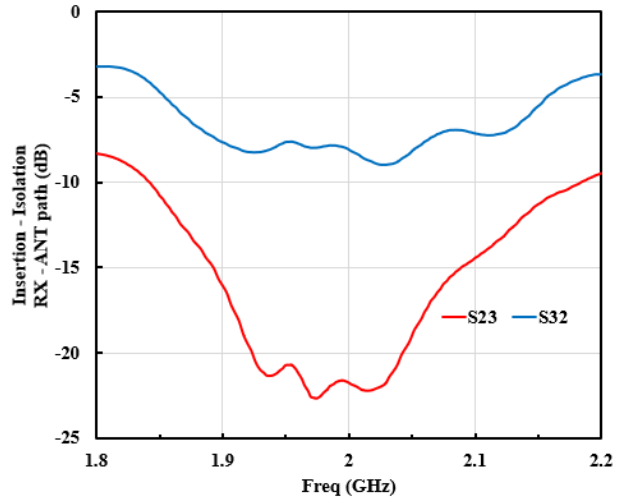

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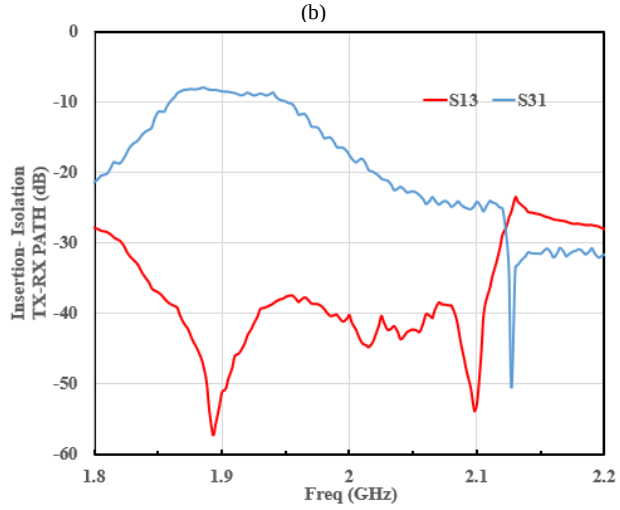
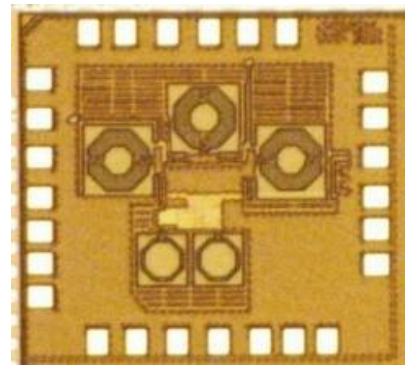


(c)

Fig. 12 Insertion and isolation measurement of 3 ports in wideband circulator (a) TX-RX, (b) ANT- RX, (c) TX- ANT path.

GHz due to large unpredicted parasitic by measurement equipment's (cable, PCB and connectors) and excessive parasitic layout resulting in a VCO tunning range degradation.

Fig.12 shows all three-port S-parameters of NCAP delay lines based- wideband circulator. Measurement indicate that the proposed circulator can work in the bandwidth of 65 MHz from 1.985 GHz to and 2.05 GHz and suffers 6 dB, 9dB maximum in-band loss for TX-ANT, ANT-RX path respectively while the TX-RX path achieves 20 dB of minimum isolation. When compared with the narrowband circulator prototype, the proposed one is extended its bandwidth by up to 13 times. Even though, the TX-RX isolation is decreased by a half, the in-band isolation of proposed circulator still proves a fairly good result. Moreover, the TX-ANT and ANT-RX insertion loss show worse figures (6dB vs 5dB and 9db vs 6.6 dB) however still in an acceptable margin in design. In term of power consumption, the wideband counterpart consumes 2.5 times more than the narrowband circulator. This happens due to the large bias current for NCAP circuit. Fig. 13 (a) and (b) shows micro-photograph of prototype chips: narrowband and NCAP delay lines-based circulator respectively.



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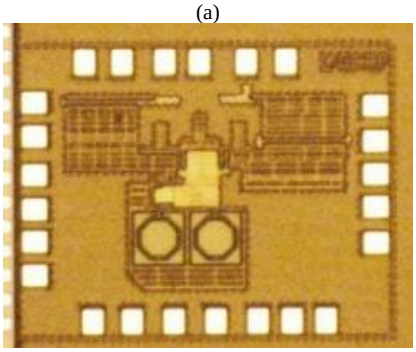

(b)

Fig. 13 Micro-photograph of (a) narrowband circulator (b) NCAP delay lines-based circulator

IV. Conclusion

In this study, we have demonstrated and verified successfully the non-magnetic non-reciprocal passive CMOS circulators based on 4-path staggered commutation network that work out both in narrow and wide-band regime. A proposed circulator is implemented in 28 nm CMOS RF process, which employed the NCAP delay lines to cancel PGD generated by gyrator and as a result, extend the circulator bandwidth up to 65 MHz, 13 times greater than that of narrowband counterpart. Moreover, the wideband circulator achieves maximum of 6 dB and 9 dB insertion loss for TX-ANT and ANT-RX path respectively while TX-RX isolation is 20dB – 26 dB over 65 MHz from 1.985 GHz to 2.05 GHz.

Further research directions will be conducted relevant to circulator P1dB improvement and TX power handling capacity. Besides, the over NF in ANT-RX path should be improved in case of NCAP delay lines employment.

REFERENCES

[1] V. E. D. R. W. Roberts, "New Design Techniques For Miniature VHF Circulators," *Lect. Notes Electr. Eng.*, vol. 294, pp. 89–142, 2014, doi: 10.1007/978-3-319-04708-9_3.
[2] "410 to 3500MHz – Surface Mount Circulator," p. 3500.
[3] T. Dinc and H. Krishnaswamy, "A T/R antenna pair with polarization-based reconfigurable wideband self-interference cancellation for simultaneous transmit and receive," *2015 IEEE MTT-S Int. Microw. Symp. IMS 2015*, pp. 2–5, 2015, doi: 10.1109/MWSYM.2015.7167135.
[4] M. Mikhemar, H. Darabi, and A. A. Abidi, "A multiband RF antenna duplexer on CMOS: Design and performance," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2067–2077, 2013, doi: 10.1109/JSSC.2013.2264626.
[5] M. Elkholy, M. Mikhemar, H. Darabi, and K. Entesari, "Low-Loss Integrated Passive CMOS Electrical Balance Duplexers With Single-Ended LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 5, pp. 1544–1559, 2016, doi: 10.1109/TMTT.2016.2541118.
[6] H. Bosma, "On Stripline Y-Citculation At Uhf," *IEEE Trans. Microw. Theory Tech.*, vol. 12, no. 1, pp. 61–72, 1964, doi: 10.1109/TMTT.1964.1125753.
[7] S. Wang, C. H. Lee, and Y. Bin Wu, "Fully Integrated 10-GHz Active Circulator and Quasi-Circulator Using Bridged-T Networks in Standard CMOS," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 10, pp. 3184–3192, 2016, doi: 10.1109/TVLSI.2016.2535377.
[8] S. A. Ayati, D. Mandal, B. Bakkaloglu, and S. Kiaei, "Adaptive integrated CMOS circulator," *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, vol. 2016-July, pp. 146–149, 2016, doi: 10.1109/RFIC.2016.7508272.
[9] I. Circulator, "Active Circulators-The Realization," no. 1, 2021.
[10] I. Transactions and O. N. Magnetics, "Field Effect Transistor Circulator," *IEEE Trans. Magn.*, vol. 37, no. 4 II, 2001.
[11] G. Carchon and B. Nauwelaers, "Power and Noise Limitation of Active Circulators," vol. 48, no. 2, pp. 316–319, 2000.
[12] N. Reiskarimian and H. Krishnaswamy, "Magnetic-free non-reciprocity based on staggered commutation," *Nat. Commun.*, vol. 7, pp. 1–10, 2016, doi: 10.1038/ncomms11217.
[13] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, "A CMOS Passive LPTV Nonmagnetic Circulator and Its Application in a Full-Duplex Receiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, 2017, doi: 10.1109/JSSC.2017.2647924.
[14] N. Reiskarimian, M. B. Dastjerdi, J. Zhou, and H. Krishnaswamy, "Analysis and design of commutation-based circulator-receivers for integrated full-duplex wireless," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2190–2201, 2018, doi: 10.1109/JSSC.2018.2828827.
[15] T. Dinc, A. Nagulu, and H. Krishnaswamy, "A Millimeter-Wave Non-Magnetic Passive SOI CMOS Circulator Based on Spatio-Temporal Conductivity Modulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3276–3292, 2017, doi: 10.1109/JSSC.2017.2759422.
[16] T. Dinc, M. Tymchenko, A. Nagulu, D. Sounas, A. Alu, and H. Krishnaswamy, "Synchronized conductivity modulation to realize broadband lossless magnetic-free non-reciprocity," *Nat. Commun.*, vol. 8, no. 1, pp. 1–9, 2017, doi: 10.1038/s41467-017-00798-9.
[17] N. D. H. Lai, N. T. Doan, H. Kim, and S. W. Yoon, "A 2-port stable negative capacitance circuit design with unilateral gain boosting technique," *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 12, pp. 4953–4959, 2017, doi: 10.1109/TMTT.2017.2747540.
[18] M. K. Soni and R. Mehra, "Optimized design and performance analysis of Johnson counter using 45 nm technology," *1st IEEE Int. Conf. Power Electron. Intell. Control Energy Syst. ICPEICES 2016*, 2017, doi: 10.1109/ICPEICES.2016.7853097.
[19] H. Joshi, P. S. M. Ranjan, and P. Vijay, "Design of High Speed Flip-Flop Based Frequency Divider for GHz PLL System : Theory and Design Techniques in 250nm CMOS Technology," *Ijecse.Org*, 1956, [Online]. Available: http://www.ijecse.org/wp-content/uploads/2012/07/Volume-1Number-3PP-1220-1225.pdf
[20] Maiti and Bidinger, *Clocking in Modern VLSI Systems*, vol. 53, no. 9. 1981.
[21] H. Mirzaei and G. V. Eleftheriades, "Realizing non-foster reactive elements using negative-group-delay networks," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 12, pp. 4322–4332, 2013, doi: 10.1109/TMTT.2013.2281967.