Retro-directive RF SOC with Magnetic-free Circulator

***Abstract*— Herein, the paper presents RF front-end ICs for a wireless power transmission system (WPTS) employing phase conjugating retro-directive array. The system operates at 2.4 GHz ISM band. RF ICs includes a low noise small signal amplifier, mixer, and drive amplifier. RF ICs are implemented in GF 130nm RF CMOS technology. The size including all blocks of the RF ICs is 15.25 mm^2. The supply voltage is 1.2 V. The circuit simulations are fully verified by Cadence platform Tools. The fabricated RF Front-end module is measured by a signal generator and a speed sampling oscilloscope. A two-port vector network analyzer is used to measure the S-parameter of the circulator 2 ports at a time, whereas the third port is terminated with a variable impedance tuner to tune the port impedance.**

***Index Terms* — CMOS magnetic-free Circulator, mixer, low noise amplifier, retro-directive array, drive amplifier, beamforming, jitter.**

I. INTRODUCTION

Fig. 1(b) shows the phase conjugating technique to perform retrodirective array. The method requires active blocks such as local oscillator (LO) and mixer. The incident wave at each antenna will be employed to generate signal has conjugated phase. The conjugated phase signal is fed to the same antenna. Therefore, array will generate a main beam which has direction towards the location positioning the power hungry device (PHD).

The Van Atta array is rather simple for implementation. Nevertheless, it is only applied for plane wave due to its bulky

geometry, thus inefficient for application. In this work, we propose the use of phase conjugate technique which is more preferable to realize the power transmission retrodirective radar system. The operating frequency is chosen at 2.4 GHz, which is defined for industrial, scientific and medical (ISM) using. The phase conjugating circuit will be implemented by commercial devices as well as CMOS technology. Section II presents the fundamental principles for beamforming system. The critical blocks will be examined based on the reported articles as well as whole simulation results are shown to verify the system principle in section III. Finally, section IV concludes the work.

II. CIRCUIT DESIGN EXPERIMENTS

Fig. 1(b) shows the phase conjugating circuitry for one

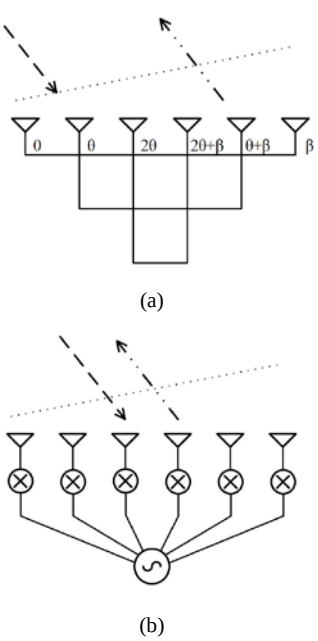

Fig. 1. Retrodirective array system (a) Van Atta array and (b) phase conjugate array

element in array antenna. The array is defined to be 8x8 elements. Basically, a phase conjugating circuitry contains five blocks such as voltage controlled oscillator (VCO), low noise amplifier (LNA), mixer, power amplifier (PA), power amplifier (PA). The VCO performs the role of local oscillator which provides ω_{LO} for down conversion operation of mixer. The RF signal as normal is received at antenna and goes forwards the counterclockwise to LNA via a circulator. After that, the LNA

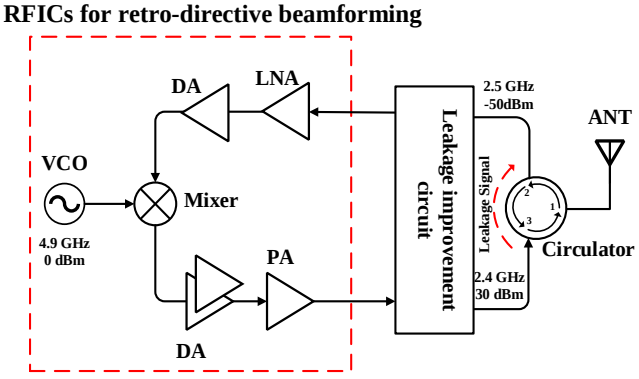

Fig. 2. Phase conjugating circuitry at block diagram level

is in charge of augmenting the RF signal to a certain level that much larger before being multiplied with LO signal by mixer.

$$V_{Mixer} = V_{RF}\cos(\omega_{RF}t+\theta)\,V_{LO}\cos(\omega_{LO}t)$$
$$= \frac{1}{2}V_{RF}V_{LO}[\cos\big((\omega_{LO}-\omega_{RF})t-\theta\big) + \cos\big((\omega_{LO}+\omega_{RF})t+\theta\big)] \quad (1)$$

where ω_{LO}, ω_{RF} is angular frequency of LO and RF signal, respectively. With noting that θ is initial phase of RF signal at receiving antenna. After unveiling the underlying specifications about the beamforming system by the PCB implementation, RF signal is supposed to be more convenient when working at 2.5 GHz while the LO one is generated at 4.9 GHz by VCO. Consequently, the IF frequency is 2.4 GHz falling within ISM band. Otherwise, the second term in (1) locates at 7.4 GHz without degrading the beamforming system's performance itself as well as interfering other bands. The following subsections describe critical blocks in detail.

A. *Mixer*

At the heart of any communication system, mixer plays a major role in translating input RF signal down to the IF signal of interest. This mixer circuit employs a well-known double balance Gilbert topology on which has a differential input sensing signal from LNA, LO signal generated by VCO and the differential IF appears at output as can be seen in Fig. 3. The signal at the output is namely the convolution product of 2 input signals: RF and LO in term of frequency domain. As a result, V_{Mixer} is the inclusion of two terms of frequency, ($f_{LO} - f_{RF}$) and ($f_{LO} + f_{RF}$) after a fashion of translation. However, the unique down conversion component ($f_{LO} - f_{RF}$) might be beneficial for the beamforming use and thus mentioned in this design. To well meet the phase conjugating criteria established for retrodirective beamforming system, mixer with respect to performance in this design not only provides such a constant output power as varied input power but also the superior AM-PM property so that the main lope power radiated by antenna does not go astray out of the position of power hungry device (PHD). Therefore, there should essentially come up with an additional circuit subsequent to core mixer, which is called the limiter. It is basically as seen as a differential amplifier operating in the saturation regime. Thanks to this improvement, the overall mixer circuit exhibits a broader input P1dB as well as a smaller AM-PM attribute than employing solely the single Gilbert cell. Particularly, the Fig. 4, as can be seen below, shows the P1dB point reaching down to -23 dBm while AM-PM is recorded only at figure of roughly 0.1^0/dB. This P1dB point corresponds to for each an increase of 20 dB input power from one end of mixer, the phase locating in IF signal is modulated by approximate 2^0 from the other end under the simulation conditions including: 0 dBm at LO port of 4.9 GHz, 2.5 GHz is assigned for input RF port and all other parameters are provided at standard conditions (TT corner, 16.85^0 for thermal noise simulation and VDD, VBIAS, VDIFF of 1.4 V). Block area estimation for layout is around **2 x 1 mm^2.**

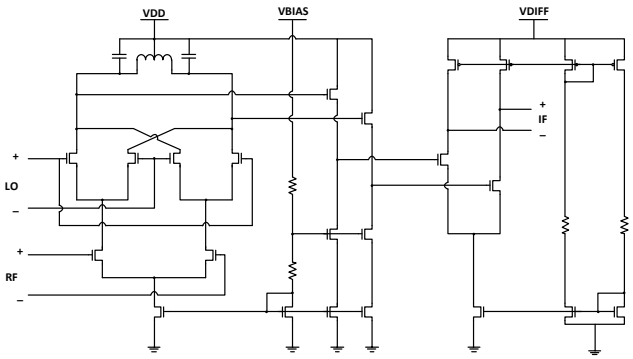

Fig. 3. Full schematic of double balance mixer for the phase conjugation

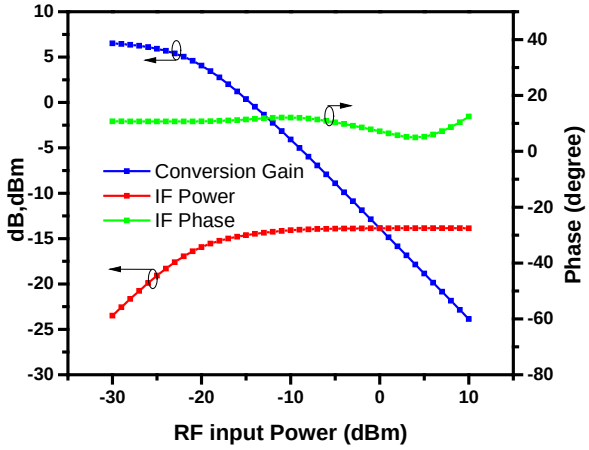

Fig. 4. Conversion gain, P1dB and AM-PM modulation

B. *Low Noise Amplifier + DA buffer*

Fig.5 presents the most conventional structure of LNA. This circuit works under differential regime, consists of a pair of cascoded NMOS, an off chip inductor at gate for noise figure (NF) optimization, an inductive degeneration to generate the matching impedance of 50 Ω and an inductive load resonated with output capacitor that imposes the 2.5 GHz operation upon suited with the input of succeeding mixer stage, an engineered drive amplifier (DA) is in essence to magnify signal sensed by LNA to some more orders. Moreover, to cope with the ubiquitous matching problem between 2 stages, it is supposed to be highly essential of inter-stage matching circuit (not given here) which helps the power transferred throughout stages obtain the output power after LNA well without being loss as much as possible.

Fig. 7 shows the overall performance of LNA cooperated with the power buffering DA circuit. Gain is basically engineered to achieve at around 43 dB which can push the small signal sensed by antenna up to some extents such that it goes beyond the P1dB point of -23 dBm and falls into the saturation region in mixer circuit. Additionally, all port matchings prove relatively good by reaching below 30 dB for a given frequency

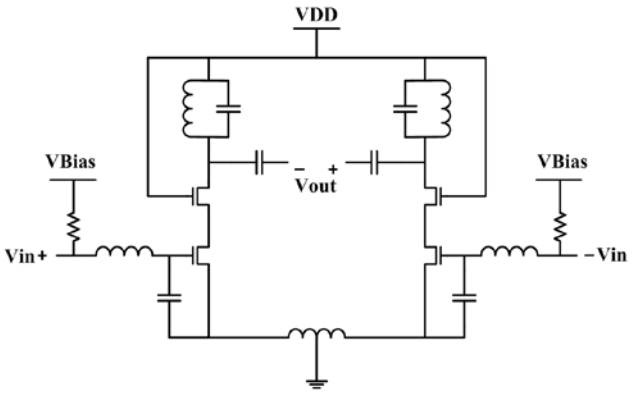

Fig. 5 Low noise amplifier (LNA) schematic

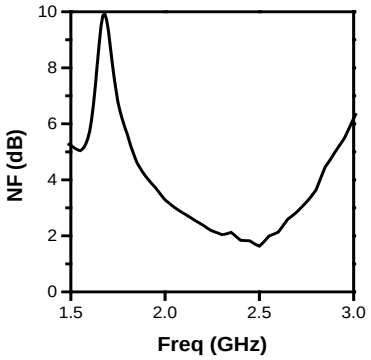

Fig.6 Noise Figure optimized at 2.5 GHz for LNA

of 2.5 GHz. Also be more as to the taped-out chip, these matching circuits would be disturbed by coupling capacitors formed during layout, as a result, matching point tends to jump down another spot. Hence, reserving a room for laser cutting is an unreplaceable part for passive tuning.

Considering noise performance in Fig. 6, even though DA circuit comes behind LNA for attaining a larger signal, the equivalent NF still remains rather low around 1.6 dB at 2.5 GHz due to the good noise performance first provided by the individual LNA stage.

The layout area estimated for this block is about **1x 1 mm^2** and DA is approximate **1.2 x 1.5 mm^2**.

C. Power Amplifier Class E

As a matter of fact, the signal after being translated by mixer

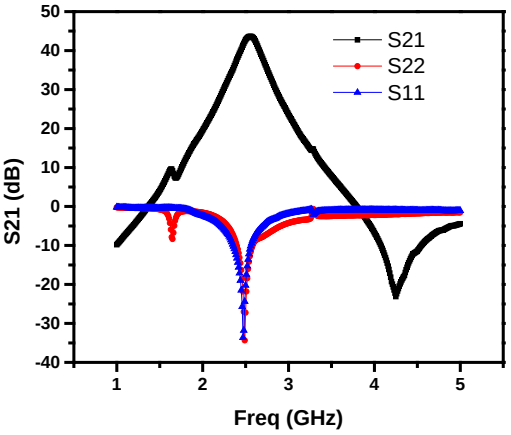

Fig.7 Gain and matching performance at 2.5 GHz

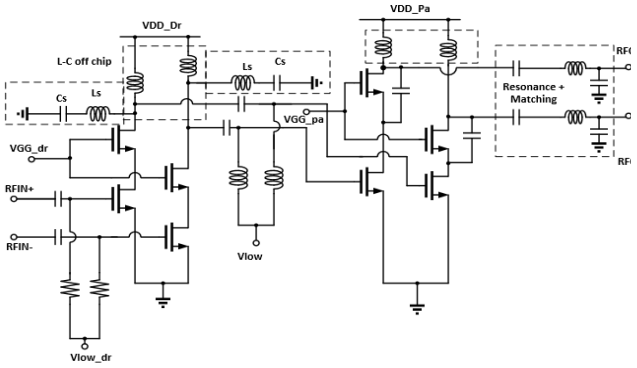

Fig. 8 A 2-stage Power amplifiers at TX path

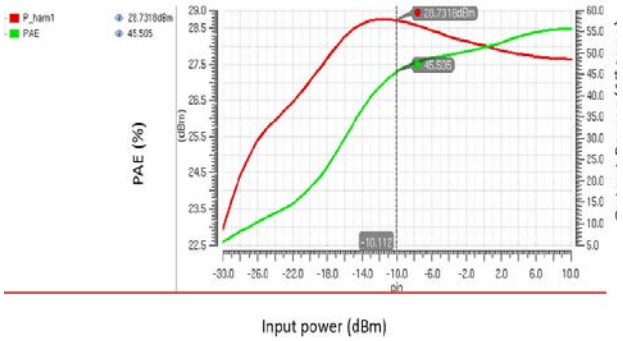

Fig. 9 P1dB and AM-PM modulation of PA at 2.4 GHz

is not sufficiently large to convey over the long distance. Thus, magnifying the IF signal to a level is a major job that the PA at transmitting path should involve in.

Fig. 11 introduces a popular-used structure of PA, which employs a first stage to amplify the small signal at 2.4 GHz by roughly 15 dB and delivers more gain at the next stage. This circuit is powered by VDD_dr and VDD_pa which are equal to 1.2 and 2.4 V respectively while consuming a current of approximate 45 mA. Otherwise, a gm-constant bias circuit is built up as well (not included here) to provide the reference voltages used for VG1 and VG2 as well as makes our chip more compact with being as least as pins to the outside possible.

As similar as LNA in section B, inter-stage and output matching in PA should be interleaved accordingly such that not only maintains the impedance matching throughout transition among stages but at ease of DC isolation and tuning capability. For those criteria, C-C-C topology is widely used at the lowest cost when compared with the others. Fig. 12 shows the gain and matching properties of PA for TX part, which contributes roughly 34 dB to signal as well as express the good matching capabilities at well below 30 dB for both terminations. The other properties, furthermore, presented in Fig. 13 are P1 dB point and AM-PM modulation. As can be seen, when reaching about -23 dBm as to input power, RF output power starts off being saturated and become significantly flatten at approximate 13.5 dBm. Concurrently, AM-PM feature shows a 0.2^0/dB

which permits the DA to operate effectively without distorting too much the phase of signal. To layout this block, area requirement is approximately **2x 2 mm^2**

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D. CMOS Magnetic-Free Circulator Device

D.1 LPTV Bandpass Filter Based-Gyrator

Figure 14 shows a 4-path differential 2-port BPF is designed in 130 nm GF CMRF8SF CMOS technology. Capacitors CBB of 20 pF is chosen with MIM cap prototype. NMOS switches optimized for low resistance by W/L = 200/0.12 (5.5 Ω) are driven by a 25% duty cycle 4-phase clock (LOA<1:4> and LOB<1:4>).

Additionally, LOA<1:4> clocks connecting with respective switches are regarded as I/Q mixer with 90^0 phase difference and similarly, the LOB<1:4> is too. These 4-phase generators are achieved by employing the conventional Johnson-counter-based ¼ dividers. The clock generator is optimized for f_s= 1GHz with a 4GHz input clock supplied from the outside. Moreover, for the staggering commutation purpose, we delay LOB<1> 90^0 versus LOA<1> thanks to the 4-bit digital controlled delay line (DCDL) [11] and inverter chains with fine-tuning cap banks as shown in Figure 14. There is a noticeable trade-off that choosing a large switch W/L will enhance the linearity and reduce loss in band of the filter. However, the more are size is the larger the parasitic

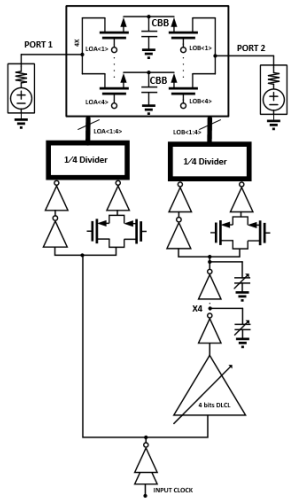
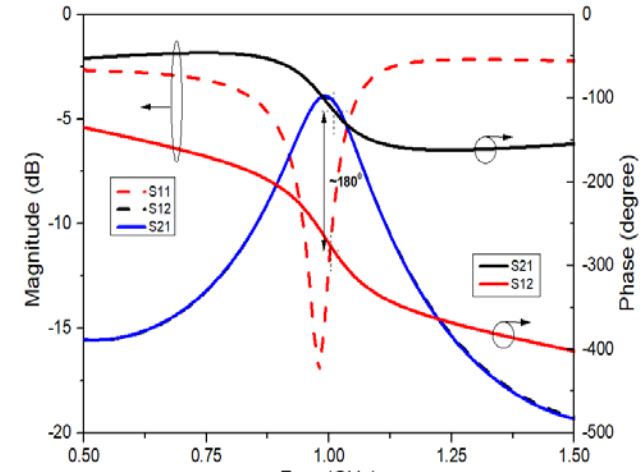


Figure 10 Non-reciprocal bandpass filter schematic (the digital controlled delay line (DCDL) and ¼ divider are not shown)

capacitors get. This results in a small frequency range and large clock leakage as well as requires more power to inquire sufficient skew of dividers to drive switches.

Figure 3 shows the simulation results of the BPF designed. magnitude response property with around 3.94 dB loss. Nevertheless, as shown in the phase response of S21 and S12 in Figure 15, there is a nearly 1800 phase difference ([delay LOB<1> -LOA<1>]*f_s*360), which states firmly that the phase non-reciprocity obtained by the timing staggered commutation is true and is most likely a crucial portion to make circulator possible in this work. The matching achieves approximate 12 dB (slightly shifts down due to parasitic



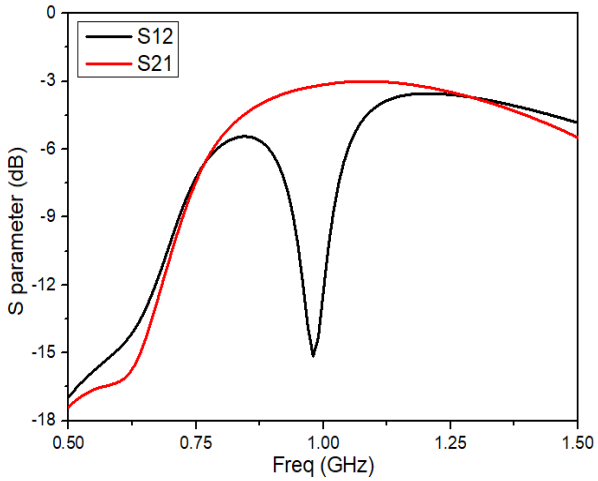


Figure 13 (a) Magnitude response of TX-ANT path and vice versa

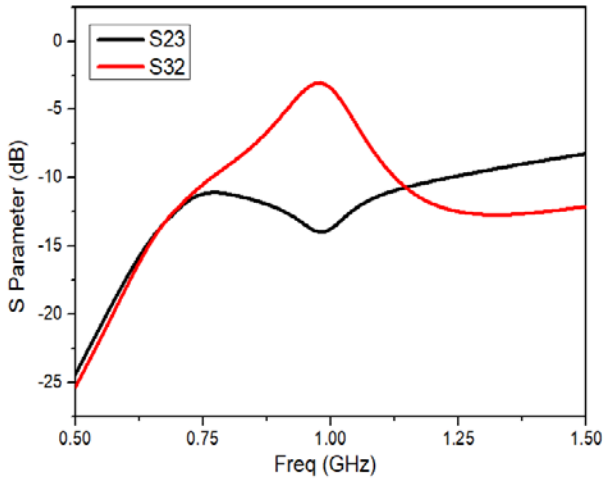


Figure 13 (b) Magnitude response of ANT-R

capacitors contributed by switch sets) at 1GHz while S21 and S12 still convey the reciprocal

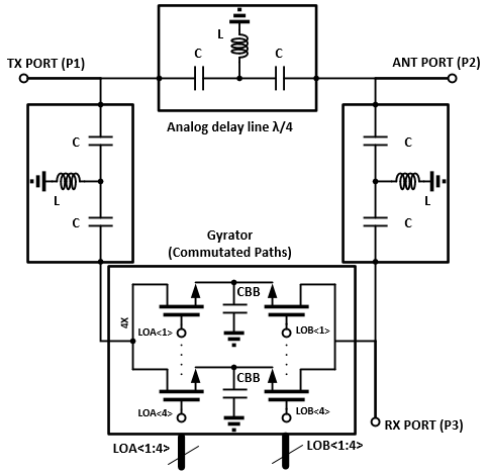


Figure 12 Circulator schematic (clock generator circuit is not shown)

D.2 Integrated Magnetic-Free Passive Circulator

A standalone circulator was implemented for tunable operation around 1 GHz in 130nm CMOS GF. The schematic is shown in Figure 16 with the same clock paths designed in Part A. The analog delay line λ/4 is miniaturized utilizing the CLC structure (in fact acts as a low pass filter) implemented completely on-chip with MIM cap and PDK inductor (Q = 5.5, 6.56 nH). The BPF is designed with N=4 to ease burden for the clock generator circuit (increasing N inquires the larger input frequency clock to feed the dividers resulting in more power consumption for the same skews on the output clocks) while maintains the acceptable loss on the ANT-RX path. The simulated S-parameters of circulator are presented in Figure 5 when all ports are terminated with 50 Ω. At the center frequency fs = 1GHz, the TX-ANT path in Figure 17 (a) expresses a wideband operation and suffers around 3.2 dB of loss while the matching ability can stand at lower than 12 dB. The ANT-RX path S32 possesses a filtering profile analogous to the BPF property in Part A with a minimum loss of 3.4 dB at 1 GHz (as be seen in Figure 17 (b)). The circulator shows a broadband TX-RX isolation (S31) better than 18.6 dB across a band of approximately 430 MHz as described in Figure 5 (c). To increase the isolation between TX and RX, there will be an off-chip impedance tuner at the Antenna port employed once we do measurements after the tape-out period. BSIM4 model manifests an expected limitation as to the 3rd Nonlinearity simulation in CMOS passive circuit [12]. Thus, in this work, we merely introduce the power compression simulation showing the relation between input power and power gain of fundamental tone (1 GHz) in the TX-ANT path instead of the common IIP3 simulation. The high linearity of circulator where the power gain is kept at around -2.6 dB corresponding to the input power level greater than 20 dBm. The measured NF at receiving path is 2.9 dB in our simulation run, this is due to phase noise stemming from imperfect driving clock signals produced by divider circuits. For layout design of this block, it is required a minimum of **3.5x0.7 mm^2**.

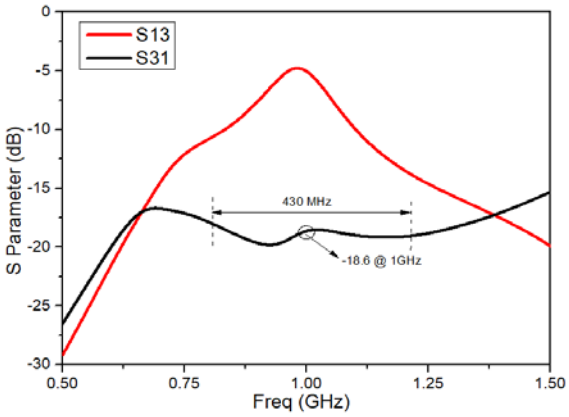


Figure 13 (c) Isolation response TX-RX and forward path.

III. CIRCUIT DESIGN METHODS

A. CIRCUIT DESIGN FLOW

Flow	ANSYS	Cadence	Siemens
Schematic	Electronics	Virtuoso Schematic Editor L	
Simulation		SPECTRE RF 19	
Waveform		Virtuoso ADE L/XL	
Layout		Virtuoso Layout L	
DRC,LVS			Calibre nmDRC, nmLVS
LPE			Calibre PEX (RC)
Post Simulation		SPECTRE RF 19	
Waveform		Virtuoso ADE L/XL	
Package/PCB		Sigrity 2021	PADS

Fig 14. Design Flow is used in our SOC

We have plan to design our system with Analog/RF design flow using available tools provided by IDEC as mentioned in Figure 14.

B. CHIP LAYOUT PLAN

The area essential for overall SOC is floored plan as shown in Figure 15, herein, we would like a die of around **4 x4 mm^2** to implement our idea in this tape out. Additionally, this area does not take into account the area for back-up and testing another Circulator IC. Hence Area of minimum 4x4 mm^2 would be a best choice to help our study be successful in this strategic study.

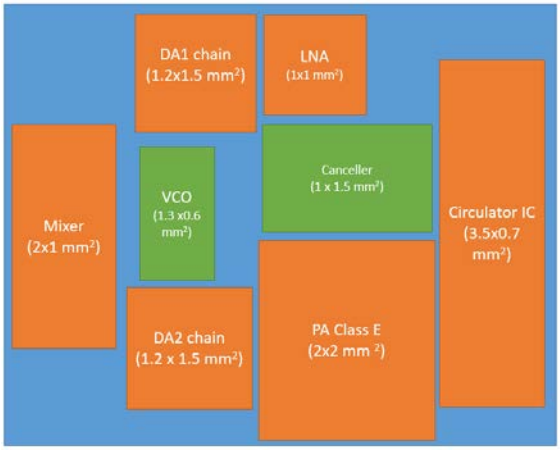


Fig 15. Estimated Layout of **4x4 mm²** Chip

C. SIMULATION VERIFICATION

A clock generator of 4 GHz is used to provide initial input clock for circulator. A two-port vector network analyzer (VNA) is used to measure the S-parameter of circulator two ports at a time, whereas the third port is terminated with a variable impedance tuner to tune the port impedance. For the IP3 test, a two-way power combiner is used to combine two sinusoidal signals generated from two additional signal generators and feed the input port under consideration. A spectrum analyzer (SA) is used to monitor the fundamental signals and the third-order intermodulation distortion products of the circulator at the output port under consideration, whereas the third port is terminated with a 50 Ω termination.

IV. CONCLUSION

RF ICs for retro-directive beamforming system on chip which consists of fundamental blocks of communication system (LNA, mixer, drive amplifiers) incorporates with a very novel design: magnetic-free circulator is fully presented in this paper by the potential simulation results. RF ICs are implemented in GF 130nm CMOS technology. The system employs the phase conjugating retrodirective array technique and a novel magnetic-free compact circulator device to transmit the power toward the receiver without knowing the incident carrier's phase. This method proves extremely convenient and fast-paced for intelligent applications especially in the state of the art nowadays. If design is proven by measurement after fabrication, this chip is able to take a big step into a play of wireless power transfer devices market.

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