

**ĐẠI HỌC QUỐC GIA
ĐẠI HỌC BÁCH KHOA TP HỒ CHÍ MINH**



LSI Logic Design Report Lab 4

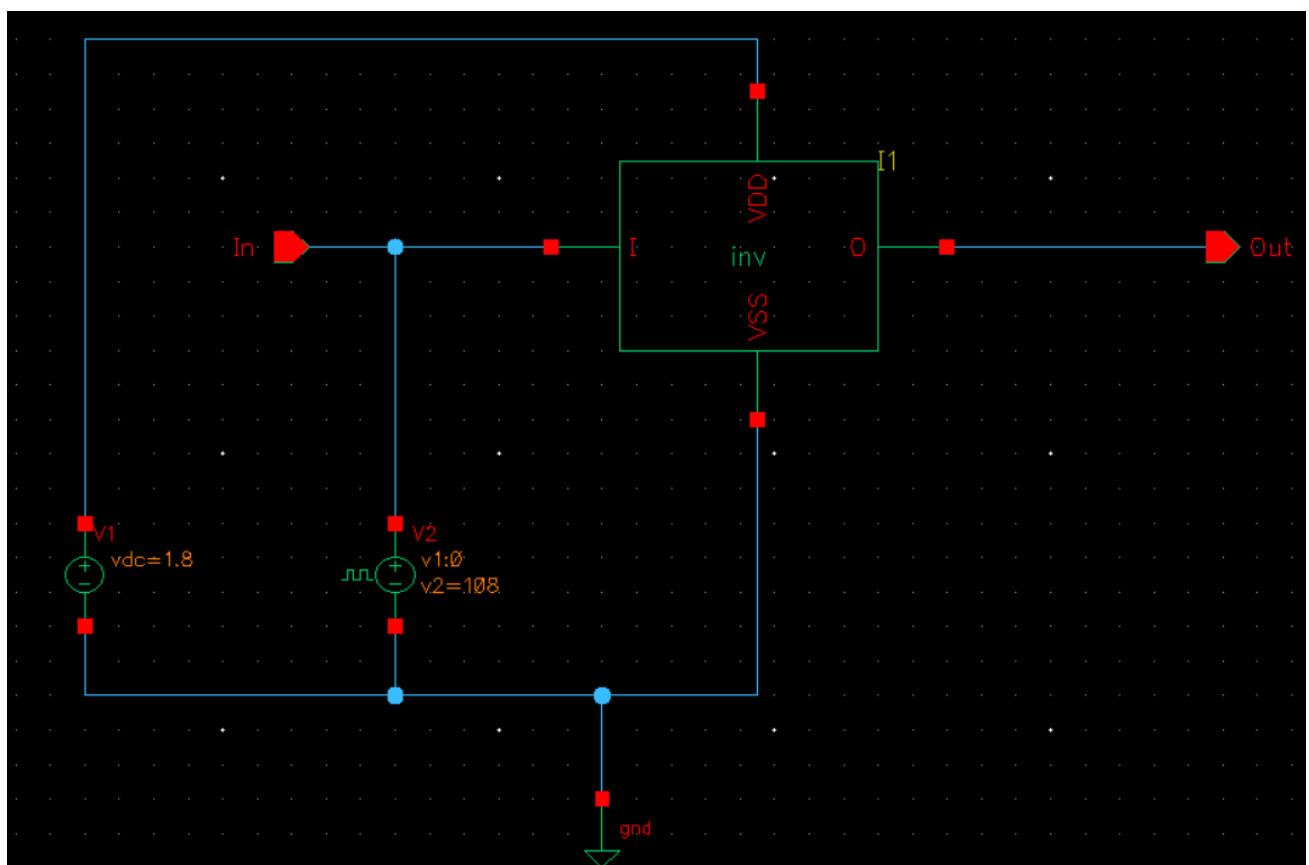
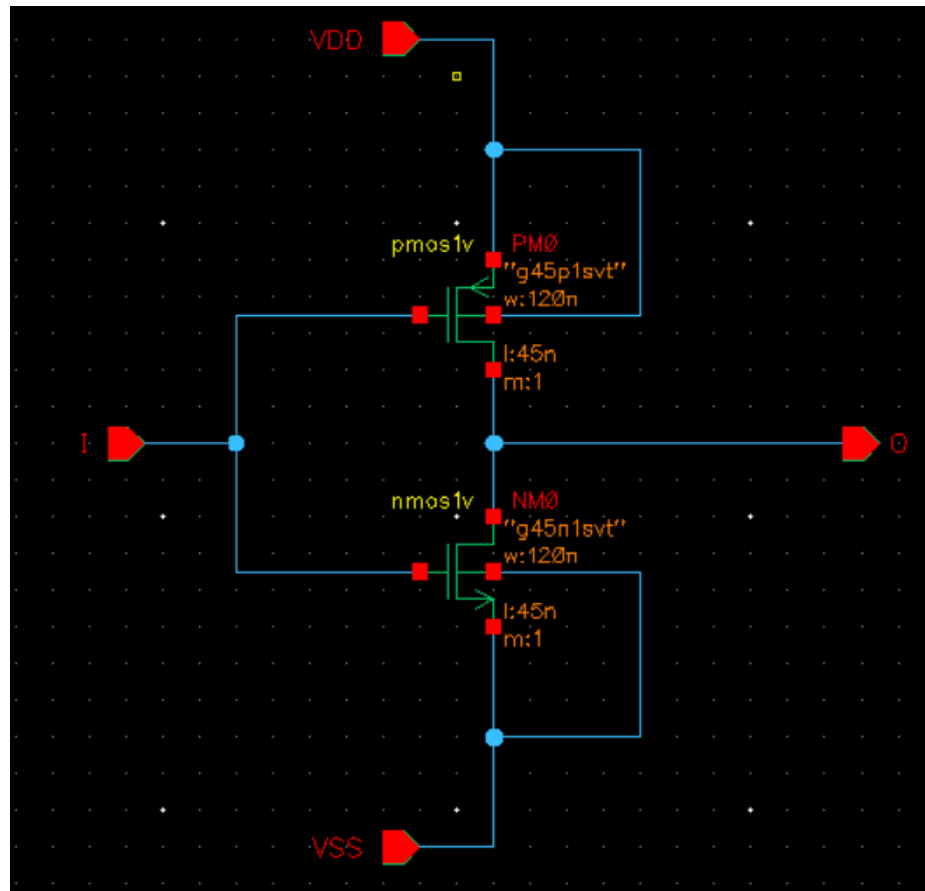
Instructor: Nguyễn Thiên Ân

Student: Lê Gia Huy – Student ID: 1952717

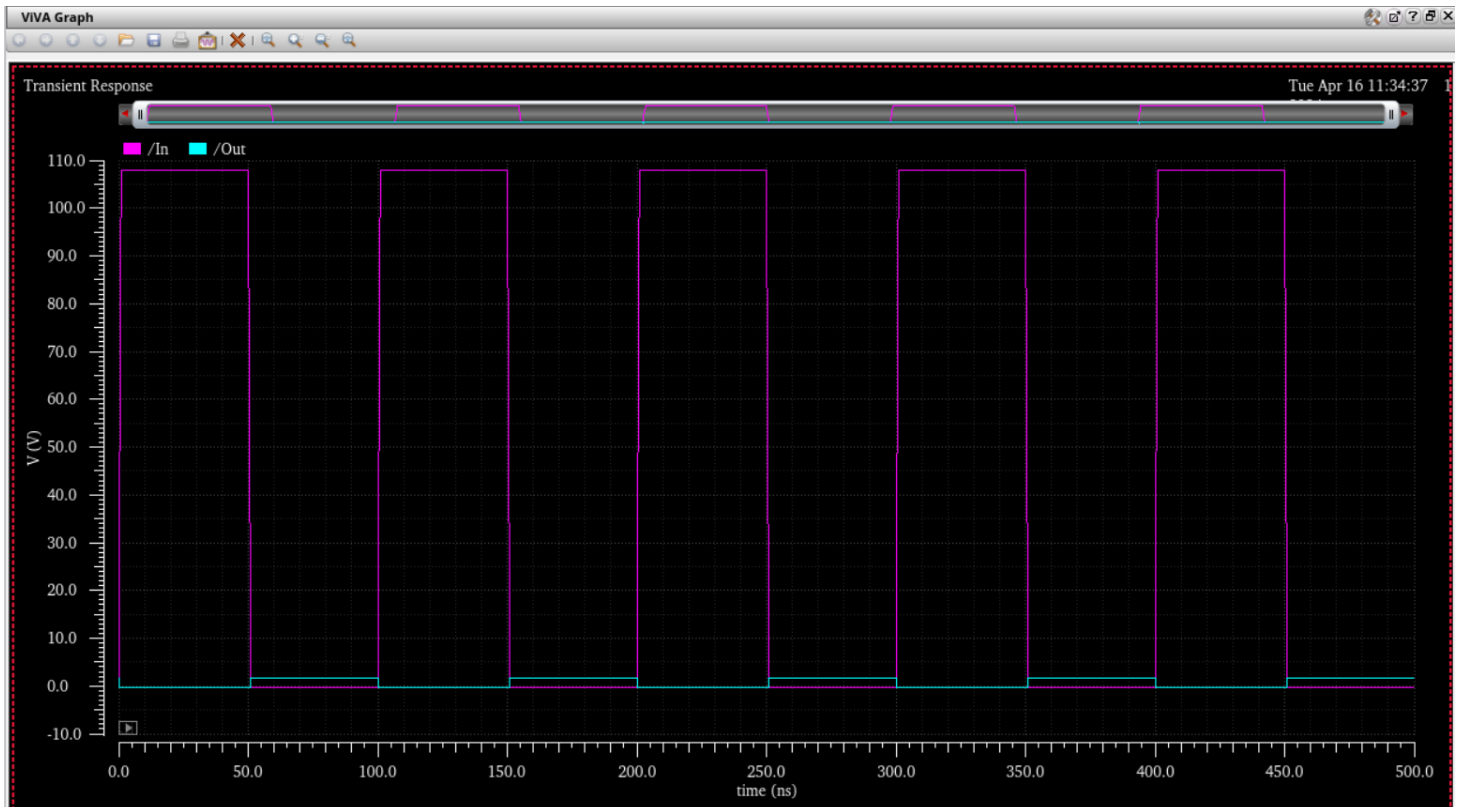
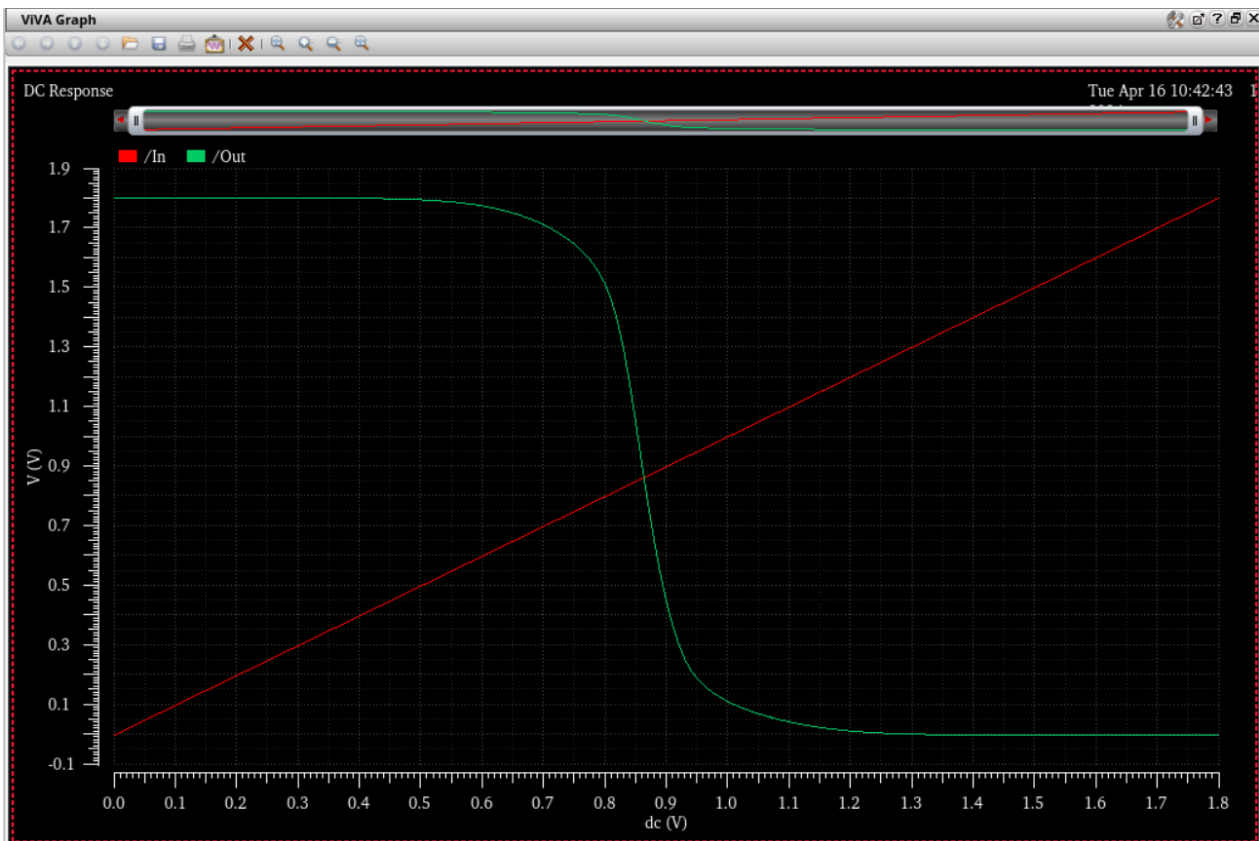
Thành phố Hồ Chí Minh – 2024

I. INVERTE GATE

1. Schematic

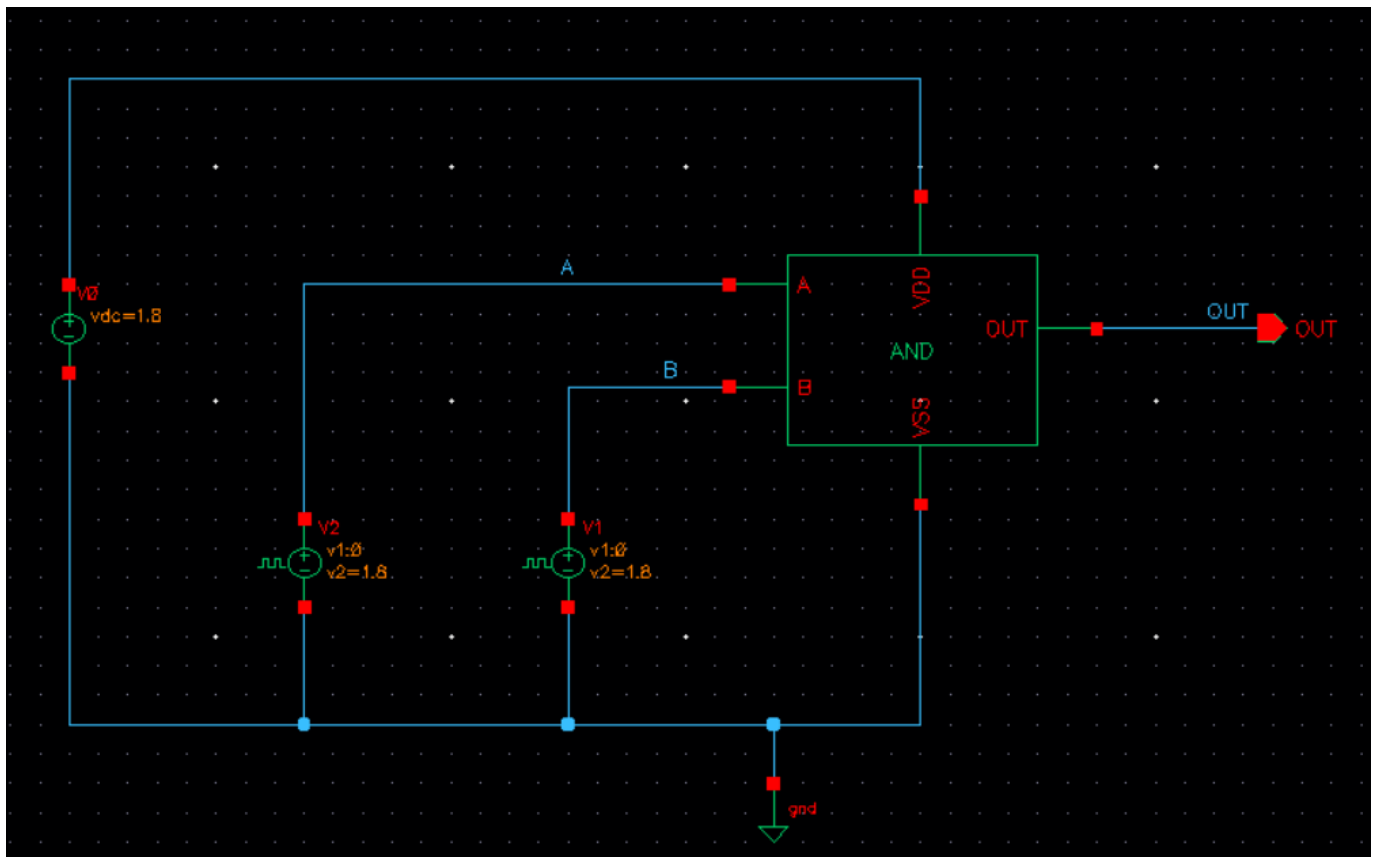
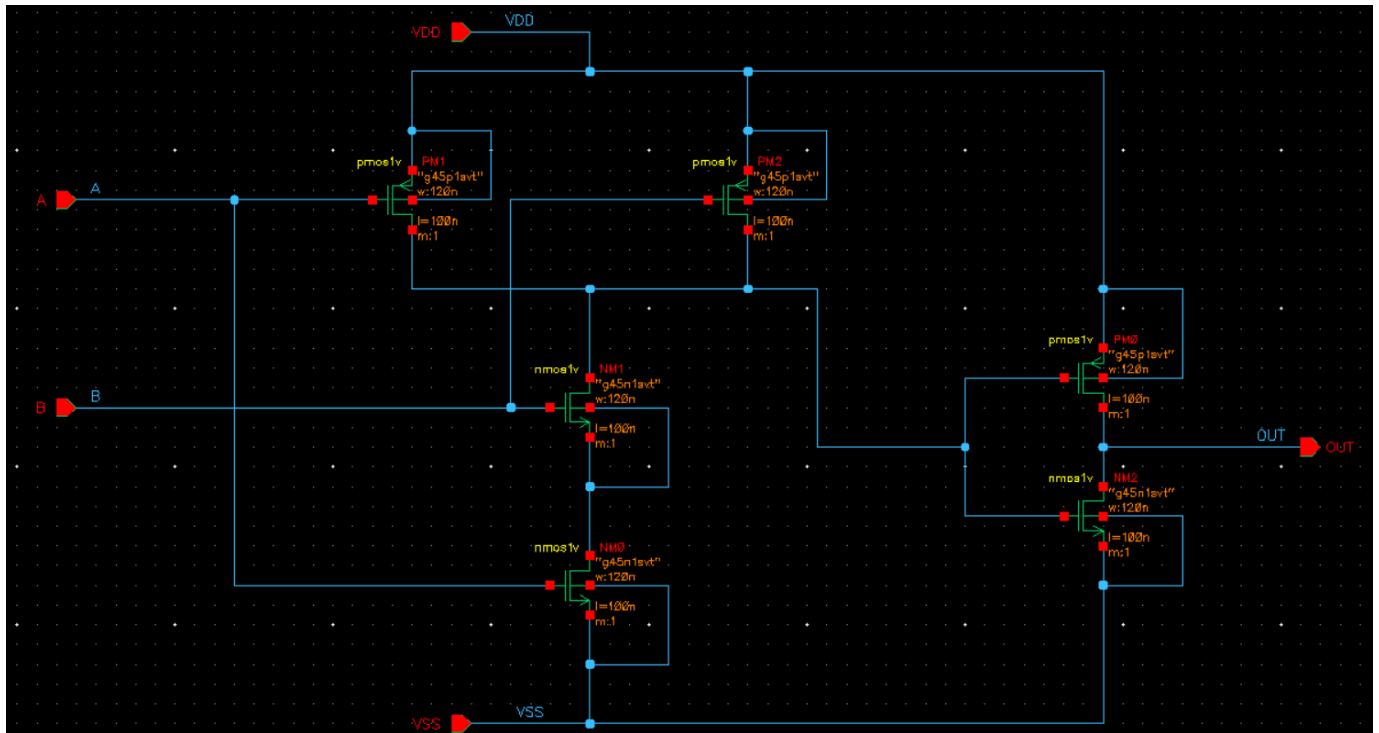


2. Simulation result

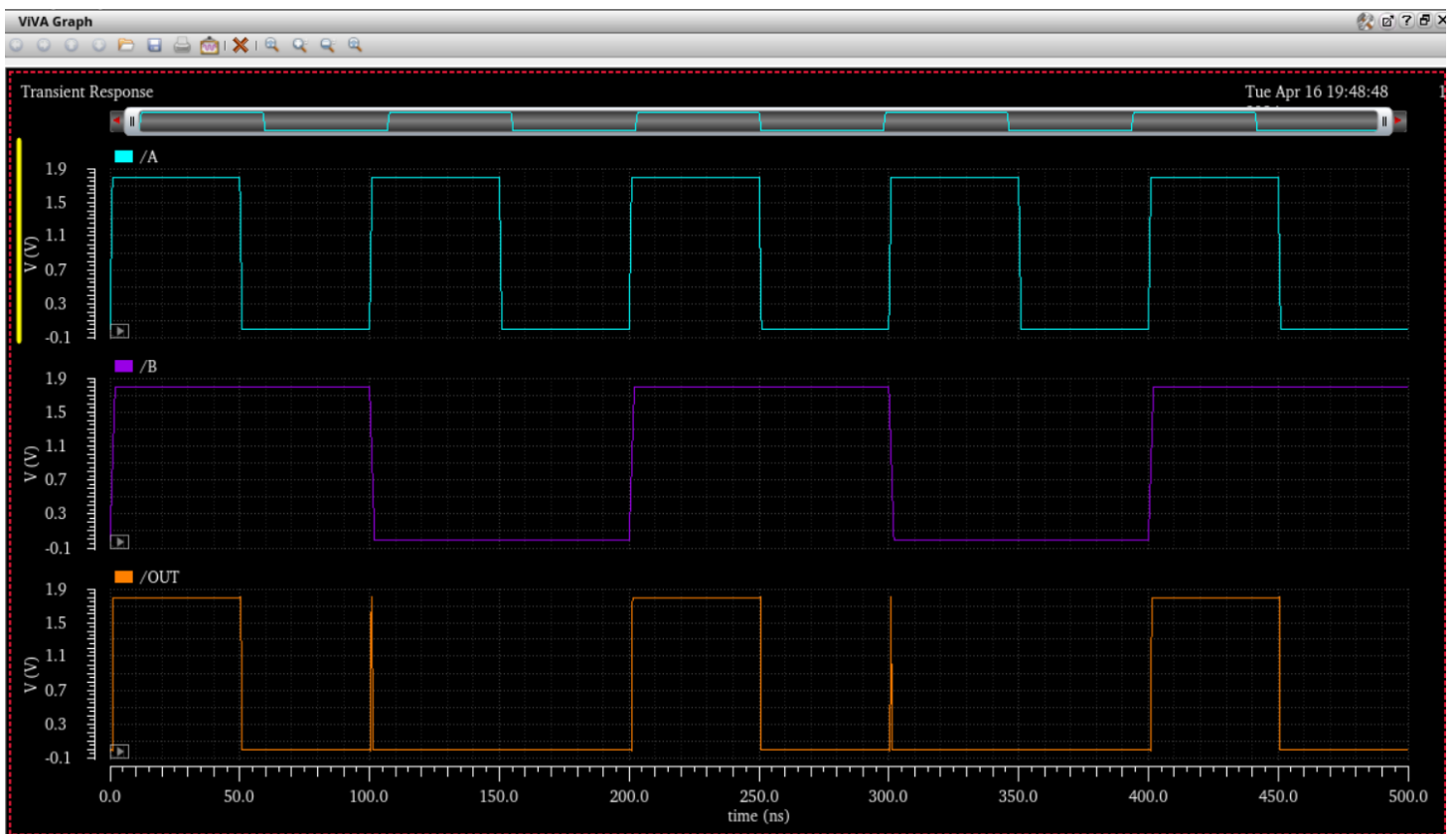


II. AND GATE

1. Schemetic

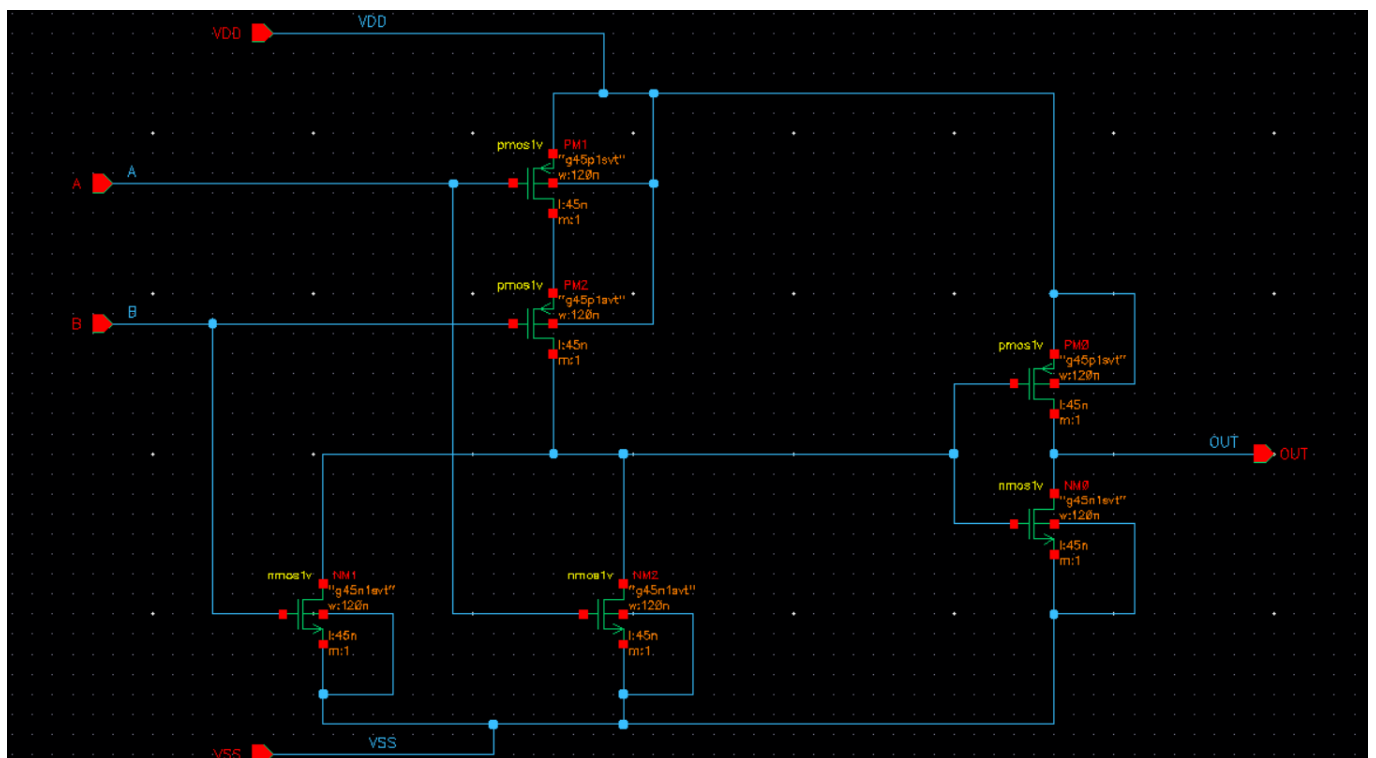


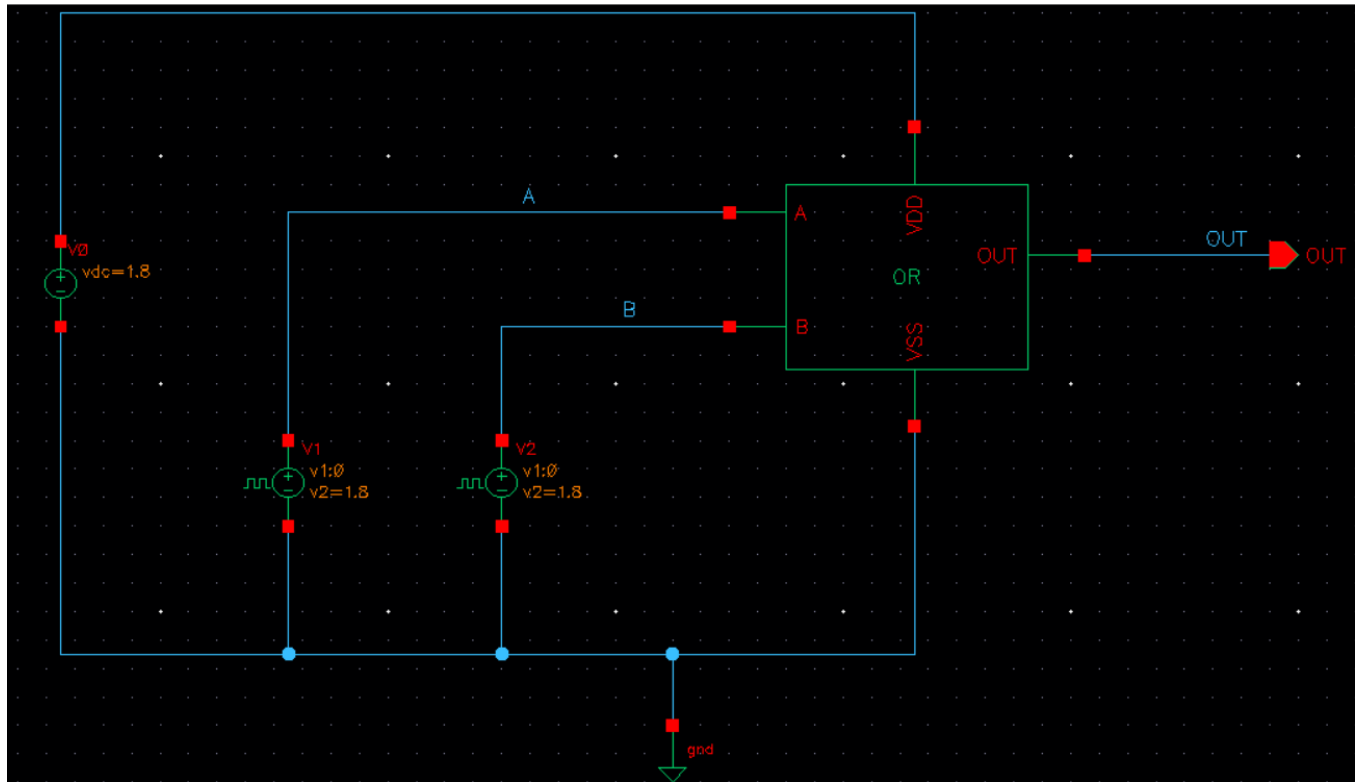
2. Simulation results



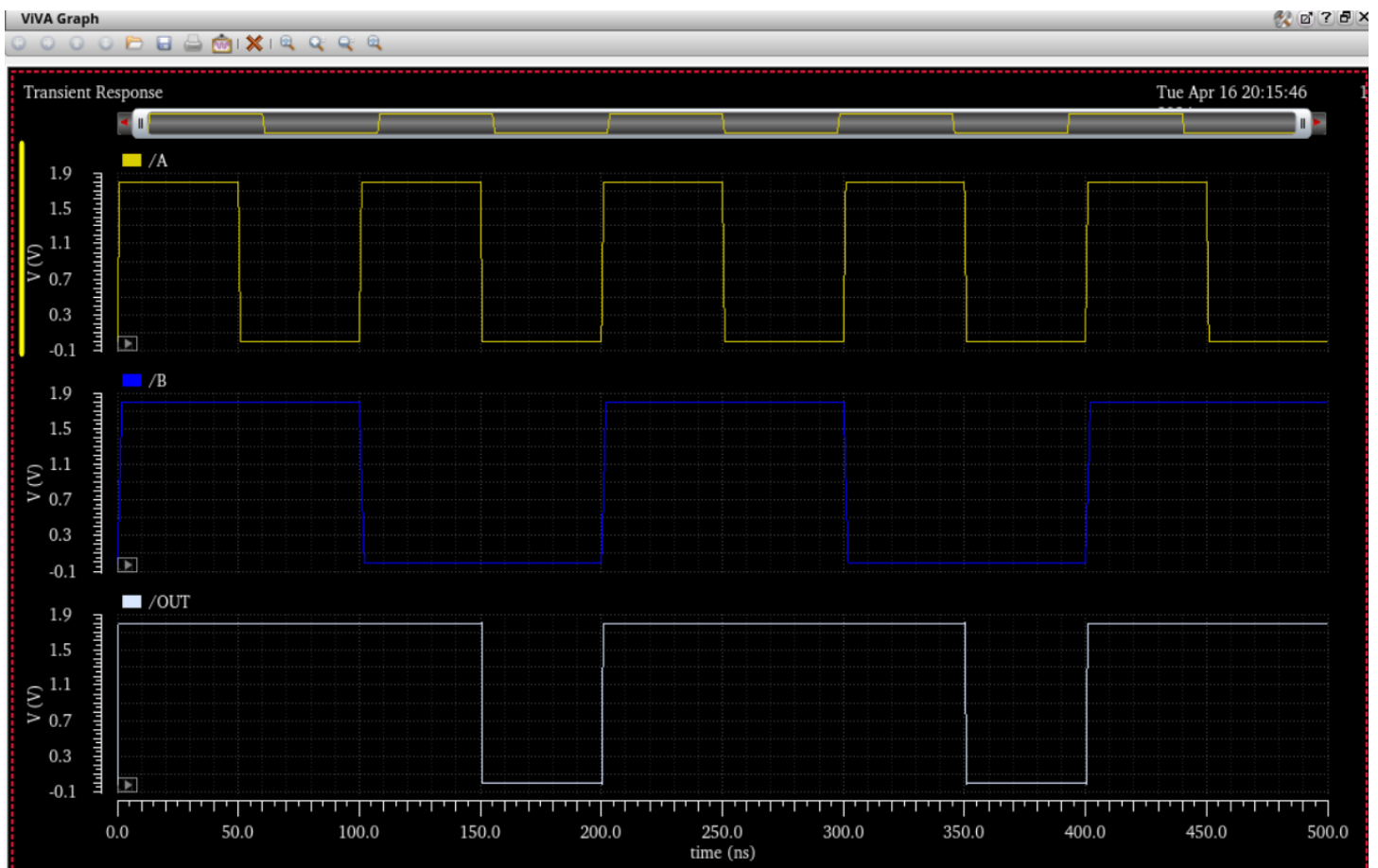
III. OR GATE

1. Schematic

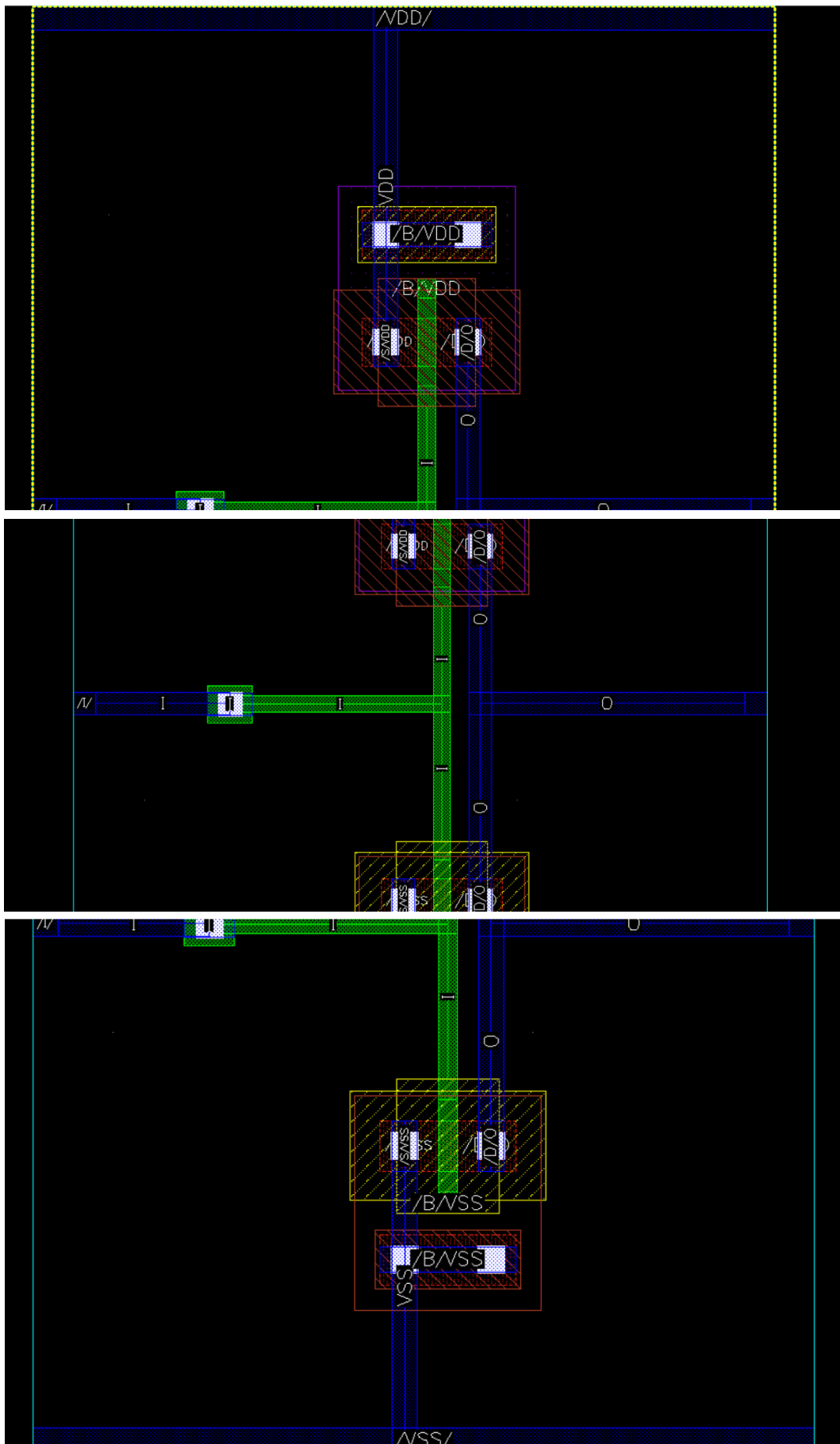




2. Simulation results



IV. Layout design of NOT Gate



V. DRC Report

PVS 21.12-64b Reports: Done [DRC] inv_@kmtt

[DRC] inv

```
NET AREA: Cumulative Time CPU = 0 (s) REAL = 0 (s)
DENSITY: Cumulative Time CPU = 0 (s) REAL = 0 (s)
MISCELLANEOUS: Cumulative Time CPU = 0 (s) REAL = 0 (s)
CONNECT: Cumulative Time CPU = 0 (s) REAL = 0 (s)
DEVICE: Cumulative Time CPU = 0 (s) REAL = 0 (s)
ERC: Cumulative Time CPU = 0 (s) REAL = 0 (s)
PATTERN_MATCH: Cumulative Time CPU = 0 (s) REAL = 0 (s)
DFM FILL: Cumulative Time CPU = 0 (s) REAL = 0 (s)

Total CPU Time : 1 (s)
Total Real Time : 1 (s)
Peak Memory Used : 26 (M)
Total Original Geometry : 55 (55)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file inv.sum
ASCII report database is /home/cc02group7/vlsi/1952717/work/testINV/inv/inv.drc_errors.asci
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Wed Apr 17 16:38:59 2024
```

Find

No errors found Warnings: 6 Info: 573

- *WARNING* LIB testINV from File /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/cds.lib Line 10 redefines
- *WARNING* LIB AND from File /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/cds.lib Line 12 redefines
- [WARN] LAYOUT_PATH at line 30 in file /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/pvs/!pvsDRC.rul is skipped. It is set in control file.
- [WARN] Cmd-line override: LAYOUT_PRIMARY "inv";

Find

Help Issues Warnings Info

ReRun ReSubmit Close Report Full

/home/cc02group7/vlsi/1952717/work/testINV/inv

VI. LVS Report

PVS 21.12-64b Reports: Done [LVS] pv_@kmtt

[DRC] inv [LVS] pvs

```
Total Real Time : 1 (s)
Peak Memory Used : 35.00 (M)

NVN Run Summary
Total CPU Time : 1 (s)
Total Real Time : 2 (s)
Peak Memory Used : 246.97 (M)

LVS Summary
Total CPU Time : 2 (s)
Total Real Time : 3 (s)
Peak Memory Used : 246.97 (M)

#####
# Run Result : MATCH #
# Run Summary : [INFO] ERC Results: Empty #
# : [INFO] Extraction Clean #
# ERC Summary File : inv.sum #
# Extraction Report File : inv.rep #
# Comparison Report File : inv.rep.cls #
#####
```

PVS 21.12-64b LVS Run Status@kmtt

ERC Results: Empty
Extraction Results: Clean
Comparison Results: Match

Do you want to start the LVS DE? Yes No

Find

No errors found Warnings: 17 Info: 12

- *WARNING* LIB testINV from File /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/cds.lib Line 10 redefines
- *WARNING* LIB AND from File /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/cds.lib Line 12 redefines
- *WARNING* LIB testINV from File /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/cds.lib Line 10 redefines
- *WARNING* LIB AND from File /data/vlsi2023/cc02group7/1952717/work/layout_env/pdk/gpdk045_v_6_0/cds.lib Line 12 redefines

Find

Help Issues Warnings Info

ReRun ReSubmit Close Report Full