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**Document Name:**

**ADSP FRAMEWORK: FIFO DRIVER**

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# Overview

This section provides an overview of software architecture.

User Application

ADSP Interface

Kernel Space

User Space

ADSP Driver

ARM

Audio HW

**ADSP Framework**

TDM class

Renderer class

Equalizer class

Capture class

TDM Plugin

ADSP

Plugin

Equalizer Plugin\*

Capture Plugin

Renderer Plugin

This document’s target is in side of red square

\* not connect to hardware modules

DAC/

ADC

FIFO

SCU

PDMA

SSI

SSIU

ADMA

Figure 1‑1 ****The software architecture****

# Function list

The following is list of functions:

Table 2‑1 Function list

|  |  |  |
| --- | --- | --- |
| **Type** | **Function Name** | **Outline** |
| API | fifo\_enable | This API is to enable the input/output of FIFO |
| fifo\_disable | This API is to disable the input/output of FIFO |
| fifo\_config | This API is to set up registers necessary for FIFO module execution |
| fifo\_register\_interrupt\_handler | This API is to register interrupt handler for FIFO |
| fifo\_unregister\_interrupt\_handler | This API is to unregister interrupt handler for FIFO |
| fifo\_disable\_interrupt | This API is to disable FIFO interrupt |
| fifo\_enable\_interrupt | This API is to enable FIFO interrupt |
| fifo\_clear\_interrupt | This API is to clear FIFO interrupt |
| fifo\_stop | This API is to stop FIFO operation |
| fifo\_check\_available | This API is to check availability of FIFO module and choose an available one |
| Internal function | fifo\_get\_int\_num | This function is to get the interrupt number |

# Detail information

This section describes detail information of data types, macro definitions, implemented APIs and internal function units, global variable.

## Data type definition

### fifo\_modules

The data type fifo\_modules is a type-defined enumeration that lists all supported FIFO modules.

Table 3‑1 fifo\_modules type information

|  |  |  |
| --- | --- | --- |
| **Member name** | **Value** | **Outline** |
| FIFO0 | 0 | 1st FIFO |
| FIFO1 | 1 | 2nd FIFO |
| FIFO2 | 2 | 3rd FIFO |
| FIFO3 | 3 | 4th FIFO |
| FIFOMAX | 4 | Number of FIFO modules |

### fifo\_error\_code

The data type fifo\_error\_code is a type-defined enumeration that lists all error codes for FIFO.

Table 3‑2 fifo\_error\_code type information

|  |  |
| --- | --- |
| **Member name** | **Value** |
| FIFO\_ERROR\_NONE | 0 |
| FIFO\_ERROR\_INVALID | -1 |
| FIFO\_ERROR\_INTERNAL | -2 |
| FIFO\_ERROR\_BUSY | -3 |
| FIFO\_ERROR\_OUT\_RANGE | -4 |

### fifo\_type

The data type fifo\_type is a type-defined enumeration of indicators of whether FIFO’s input or output is used.

Table 3‑3 fifo\_type type information

|  |  |  |
| --- | --- | --- |
| **Member name** | **Value** | **Outline** |
| FIFO\_INPUT | 0 | FIFO input is used |
| FIFO\_OUTPUT | 1 | FIFO output is used |

### FIFO\_PARAM

The data type FIFO\_PARAM is a type-defined structure that possesses necessary parameters for FIFO module.

Table 3‑4 FIFO\_PARAM type information

|  |  |  |
| --- | --- | --- |
| **Member name** | **Data type** | **Outline** |
| channel | UWORD32 | channel of data used for FIFO module |
| pcm\_width | UWORD32 | PCM width of data used for FIFO module |
| sample\_rate | UWORD32 | Sampling rate of data used for FIFO module |
| fifo\_num | fifo\_modules | FIFO module |
| type | fifo\_type | FIFO type |
| dev\_connect | UWORD32 | Indicator to show which module FIFO connects |

## Macro definition

|  |  |  |
| --- | --- | --- |
| **Macros** | **Value** | **Outline** |
| XA\_FIFO\_FULL | 1024 | FIFO full size |
| XA\_FIFO\_NEARFULL | 768 | FIFO nearly full size |
| XA\_FIFO\_NEAREMPTY | 64 | FIFO nearly empty size |
| XA\_FIFO\_EMPTY | 0 | FIFO empty size |
| XA\_FIFO\_CONNECT\_SRC | 0 | FIFO is connected to SRC |
| XA\_FIFO\_CONNECT\_SSI | 1 | FIFO is connected to SSI |

## Register definition

Below is the table listing all items that are macros representing register addresses located in repository s492d/include/sys/xt-shmem/board-rcar/xf-registers.h

|  |  |
| --- | --- |
| **Register** | **Outline** |
| XF\_RCAR\_REG\_OF\_EN | Register OF\_EN |
| XF\_RCAR\_REG\_IF\_EN | Register IF\_EN |
| XF\_RCAR\_REG\_ADSP\_TIMSEL | ADSP Output Timing Select Register |
| XF\_RCAR\_REG\_ADSP\_TIMSEL1 | ADSP Output Timing Select Register 1 |
| XF\_RCAR\_REG\_ADSP\_TIMSEL2 | ADSP Output Timing Select Register 2 |
| XF\_RCAR\_REG\_ADSP\_TIMSEL3 | ADSP Output Timing Select Register 3 |
| XF\_RCAR\_REG\_OF\_MSTP | Output FIFO Module Stop Register |
| XF\_RCAR\_REG\_OF\_PTRRST | Output FIFO Pointer Reset Register |
| XF\_RCAR\_REG\_OF0\_CH | Output FIFO0 Channel Register |
| XF\_RCAR\_REG\_OF1\_CH | Output FIFO1 Channel Register |
| XF\_RCAR\_REG\_OF2\_CH | Output FIFO2 Channel Register |
| XF\_RCAR\_REG\_OF3\_CH | Output FIFO3 Channel Register |
| XF\_RCAR\_REG\_OF\_ADINR | Output FIFO0 Audio Information Register |
| XF\_RCAR\_REG\_OF1\_ADINR | Output FIFO1 Audio Information Register |
| XF\_RCAR\_REG\_OF2\_ADINR | Output FIFO2 Audio Information Register |
| XF\_RCAR\_REG\_OF3\_ADINR | Output FIFO3 Audio Information Register |
| XF\_RCAR\_REG\_OF0\_INT\_TH | Output FIFO0 Interrupt Threshold Register |
| XF\_RCAR\_REG\_OF1\_INT\_TH | Output FIFO1 Interrupt Threshold Register |
| XF\_RCAR\_REG\_OF2\_INT\_TH | Output FIFO2 Interrupt Threshold Register |
| XF\_RCAR\_REG\_OF3\_INT\_TH | Output FIFO3 Interrupt Threshold Register |
| XF\_RCAR\_REG\_OF\_INT\_CLR | Output FIFO Interrupt Clear Register |
| XF\_RCAR\_REG\_IF\_MSTP | Input FIFO Module Stop Register |
| XF\_RCAR\_REG\_IF\_PTRRST | Input FIFO Pointer Reset Register |
| XF\_RCAR\_REG\_IF0\_CH | Input FIFO0 Channel Register |
| XF\_RCAR\_REG\_IF1\_CH | Input FIFO1 Channel Register |
| XF\_RCAR\_REG\_IF2\_CH | Input FIFO2 Channel Register |
| XF\_RCAR\_REG\_IF3\_CH | Input FIFO3 Channel Register |
| XF\_RCAR\_REG\_IF\_ADINR | Input FIFO0 Audio Information Register |
| XF\_RCAR\_REG\_IF1\_ADINR | Input FIFO1 Audio Information Register |
| XF\_RCAR\_REG\_IF2\_ADINR | Input FIFO2 Audio Information Register |
| XF\_RCAR\_REG\_IF3\_ADINR | Input FIFO3 Audio Information Register |
| XF\_RCAR\_REG\_IF0\_INT\_TH | Input FIFO0 Interrupt Threshold Register |
| XF\_RCAR\_REG\_IF1\_INT\_TH | Input FIFO1 Interrupt Threshold Register |
| XF\_RCAR\_REG\_IF2\_INT\_TH | Input FIFO2 Interrupt Threshold Register |
| XF\_RCAR\_REG\_IF3\_INT\_TH | Input FIFO3 Interrupt Threshold Register |
| XF\_RCAR\_REG\_IF\_INT\_CLR | Input FIFO Interrupt Clear Register |

## Function definition

### fifo\_disable

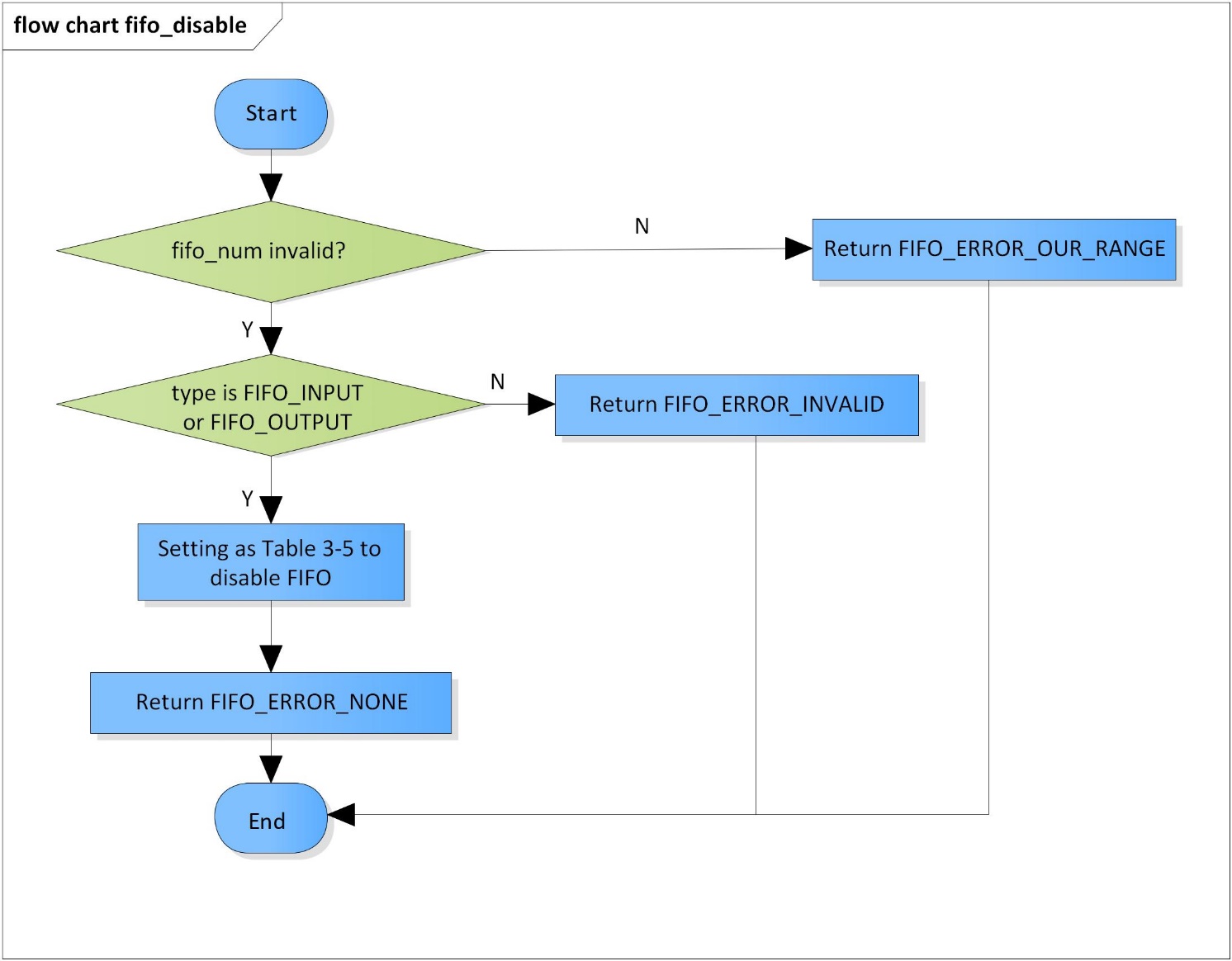
DD\_PLG\_RDR\_06\_001

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_disable(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to disable the input/output of FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO uses its input or output  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is neither FIFO\_INPUT nor FIFO\_OUTPUT | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_disable command processing:   - Set either register OF\_EN or IF\_EN based on FIFO type | | | |

[Covers: FD\_PLG\_RDR\_005, FD\_PLG\_RDR\_014, FD\_PLG\_RDR\_032, FD\_PLG\_RDR\_043]

Table 3‑5 Setting registers OF\_EN and IF\_EN to disable FIFO

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **fifo\_num** | **type** | **Register** | **Bit** | **Value** |
| FIFO0 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 0 | 0 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 0 | 0 |
| FIFO1 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 1 | 0 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 1 | 0 |
| FIFO2 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 2 | 0 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 2 | 0 |
| FIFO3 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 3 | 0 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 3 | 0 |

Figure 3‑1 fifo\_disable flowchart

### fifo\_enable

DD\_PLG\_RDR\_06\_002

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_enable(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to enable the input/output of FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO uses its input or output  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is neither FIFO\_INPUT nor FIFO\_OUTPUT | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_enable command processing:   - Set either register OF\_EN or IF\_EN based on FIFO type | | | |

[Covers: FD\_PLG\_RDR\_005, FD\_PLG\_RDR\_014, FD\_PLG\_RDR\_032, FD\_PLG\_RDR\_043]

Table 3‑6 Setting registers OF\_EN and IF\_EN to enable FIFO

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **fifo\_num** | **type** | **Register** | **Bit** | **Value** |
| FIFO0 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 0 | 1 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 0 | 1 |
| FIFO1 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 1 | 1 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 1 | 1 |
| FIFO2 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 2 | 1 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 2 | 1 |
| FIFO3 | FIFO\_OUTPUT | XF\_RCAR\_REG\_OF\_EN | 3 | 1 |
| FIFO\_INPUT | XF\_RCAR\_REG\_IF\_EN | 3 | 1 |

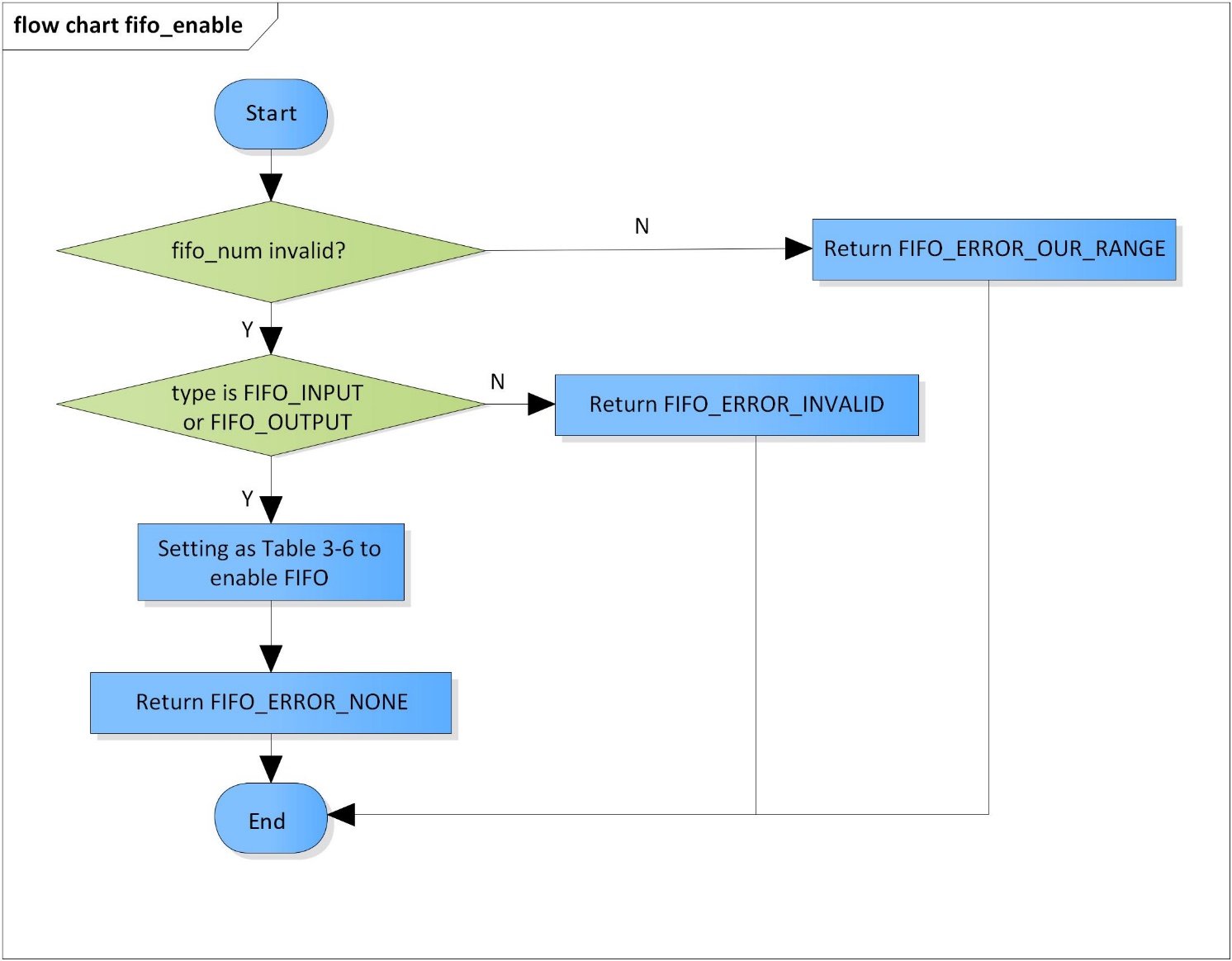


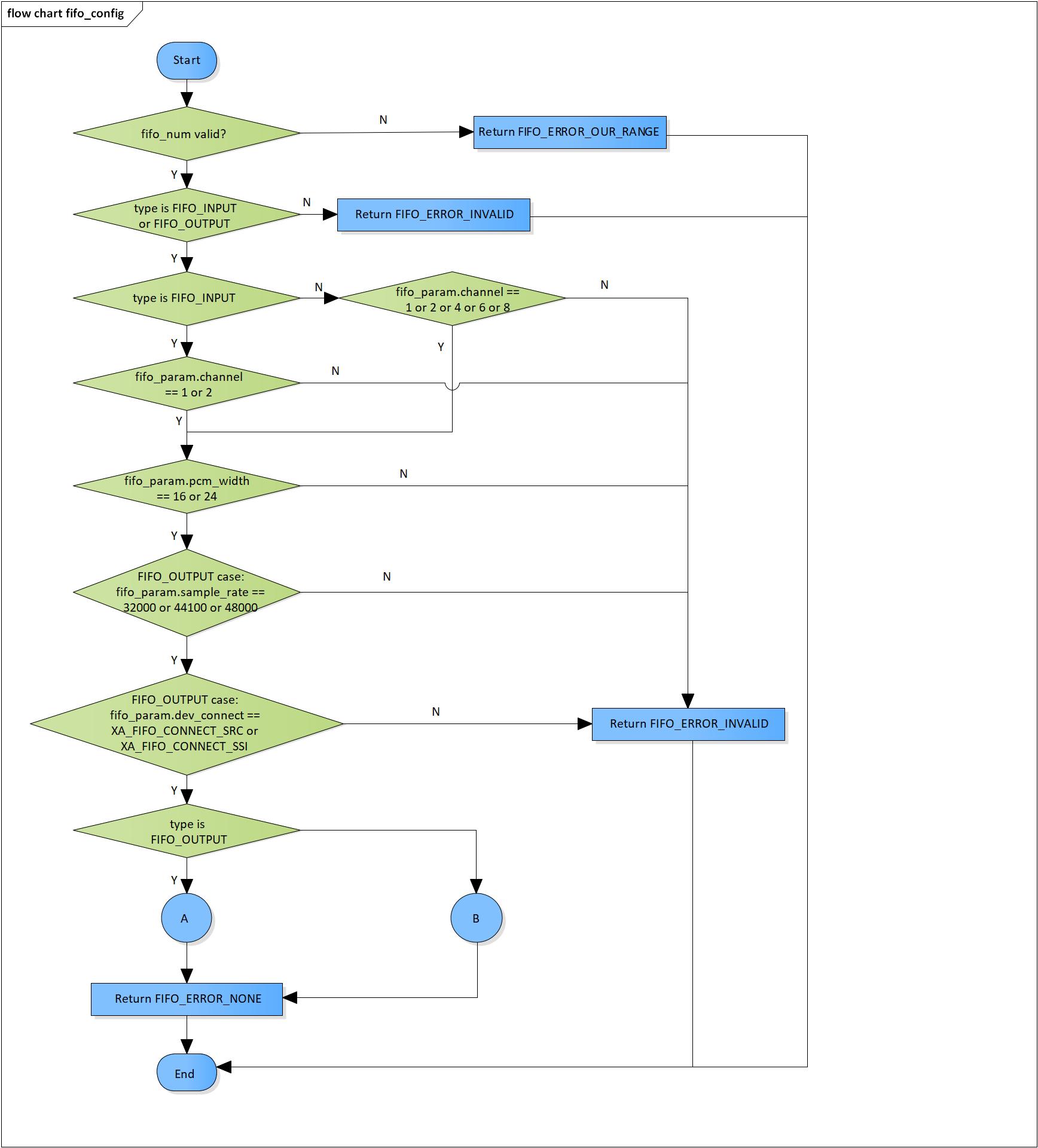
Figure 3‑2 fifo\_enable flowchart

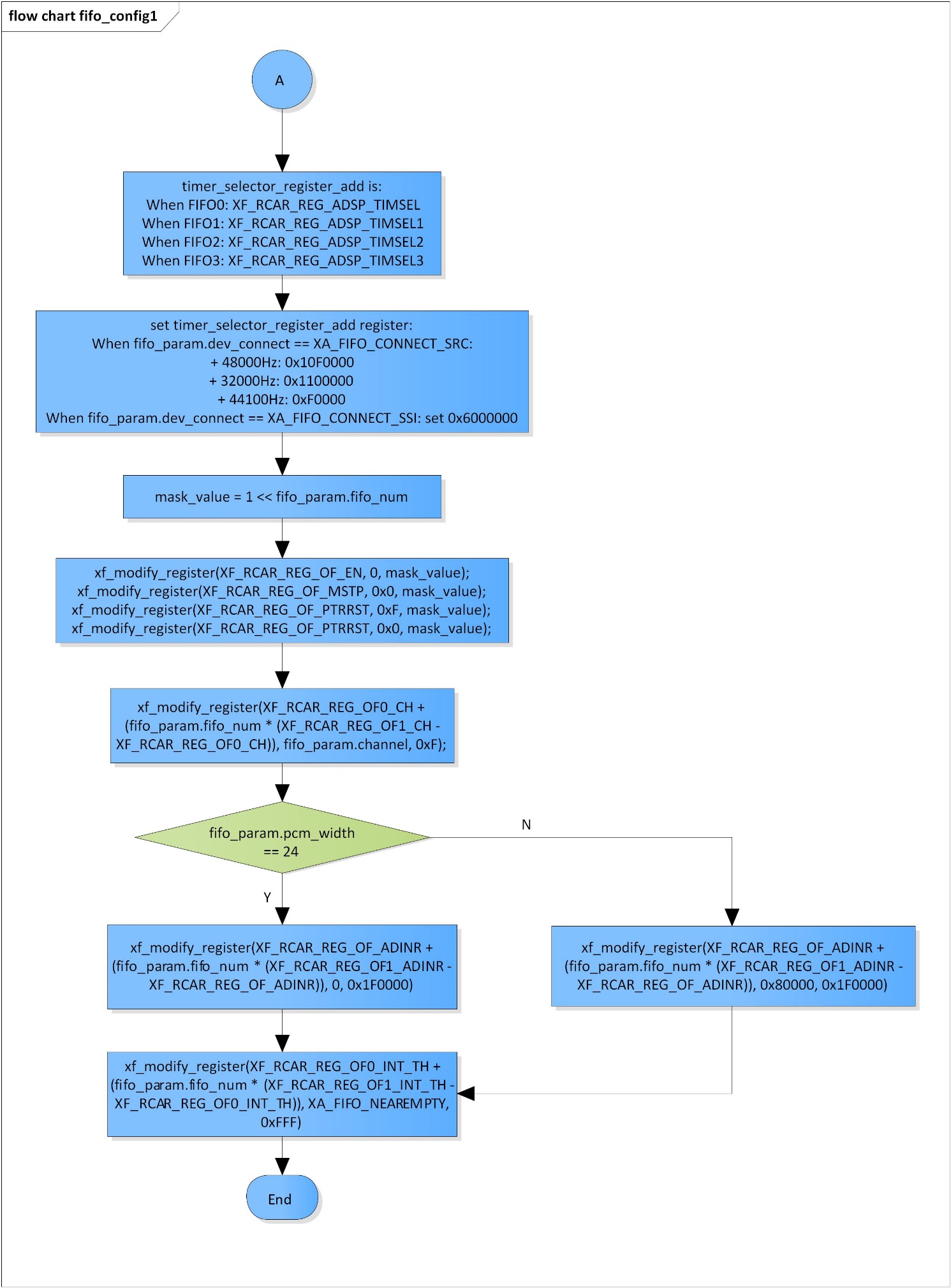
### fifo\_config

DD\_PLG\_RDR\_06\_003

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_config(FIFO\_PARAM fifo\_param) | | | |
| **Function** | This function is to set up registers necessary for FIFO module execution. | | | |
| **Arguments** | Type | Name | I/O | Description |
| FIFO\_PARAM | fifo\_param | I | Struct of parameters of FIFO |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid  Channel is invalid  PCM width is invalid  Sampling rate is invalid when FIFO type is FIFO\_OUTPUT  FIFO is not connected to and hardware module when FIFO type is FIFO\_OUTPUT | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_config command processing:   - Set registers SSI\_BUSIF\_MODE, SSI\_BUSIF\_ADINR, SSI mode register | | | |

[Covers: FD\_PLG\_RDR\_005]





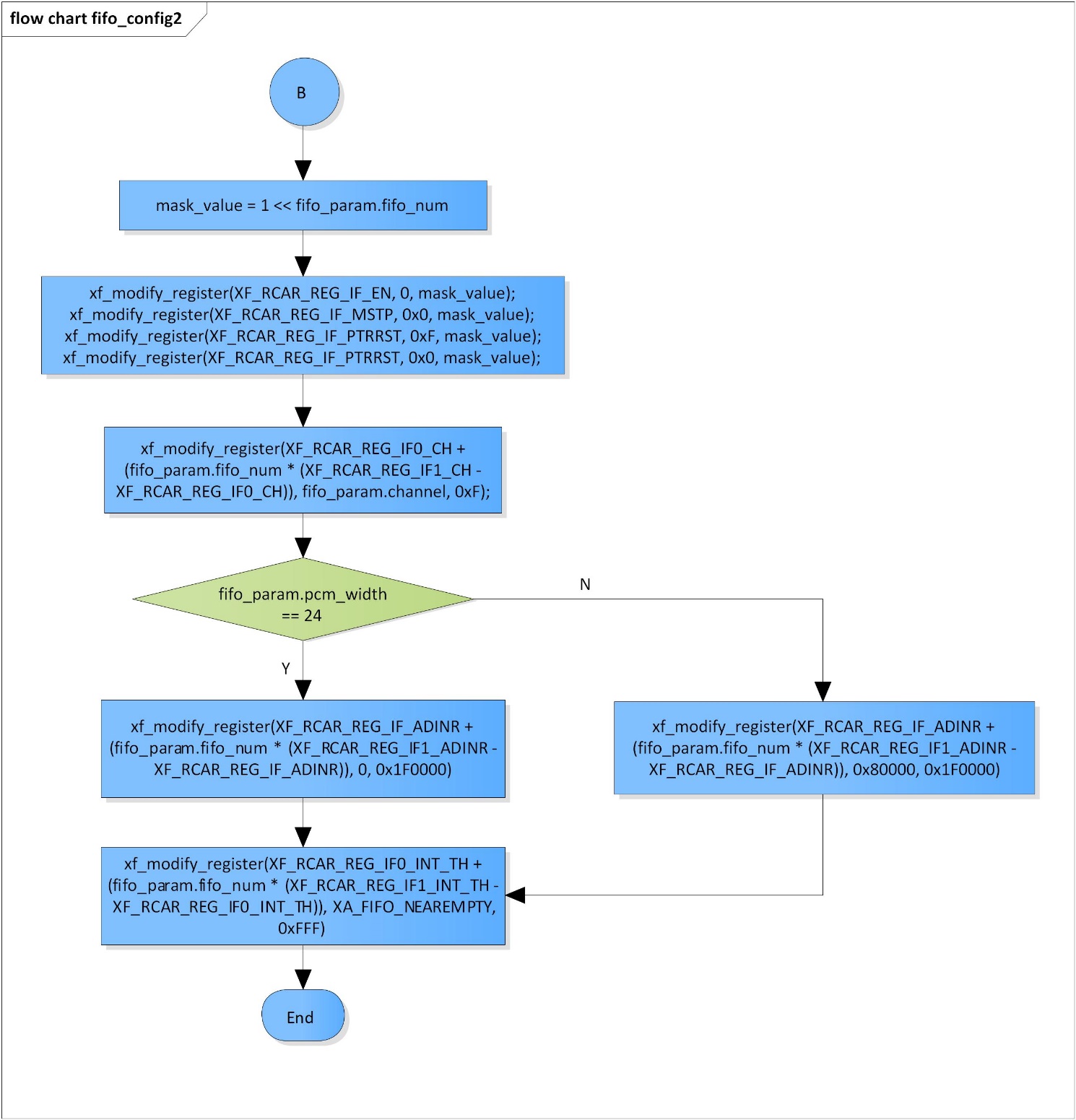


Figure 3‑3 fifo\_config flowchart

### fifo\_get\_int\_num

DD\_PLG\_RDR\_06\_004

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | static inline fifo\_error\_code fifo\_get\_int\_num(fifo\_modules module, fifo\_type type, pUWORD32 num) | | | |
| **Function** | This function is to get the interrupt number of FIFO module. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| pUWORD32 | num | I/O | Interrupt number |
| **Return value** | FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_get\_int\_num command processing:   - Get interrupt number based on FIFO module and its type (FIFO\_INPUT or FIFO\_OUTPUT) | | | |

[Covers: FD\_PLG\_RDR\_005, FD\_PLG\_RDR\_014, FD\_PLG\_RDR\_032, FD\_PLG\_RDR\_043]

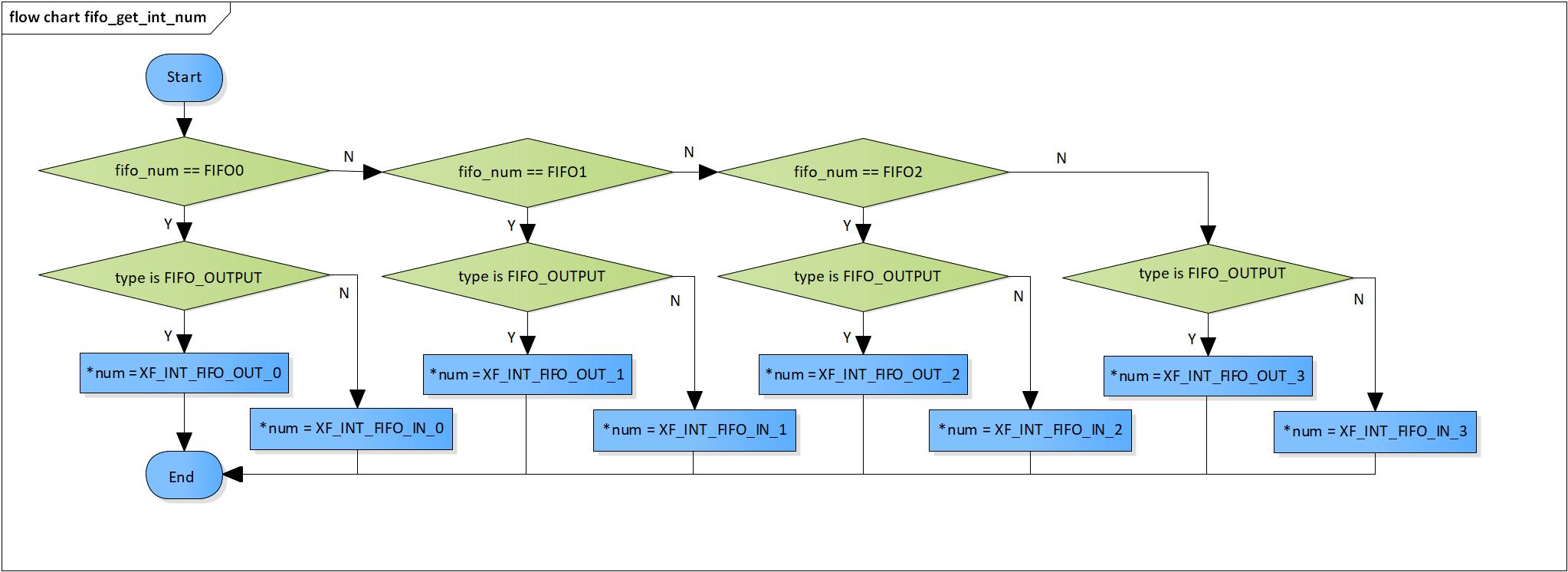


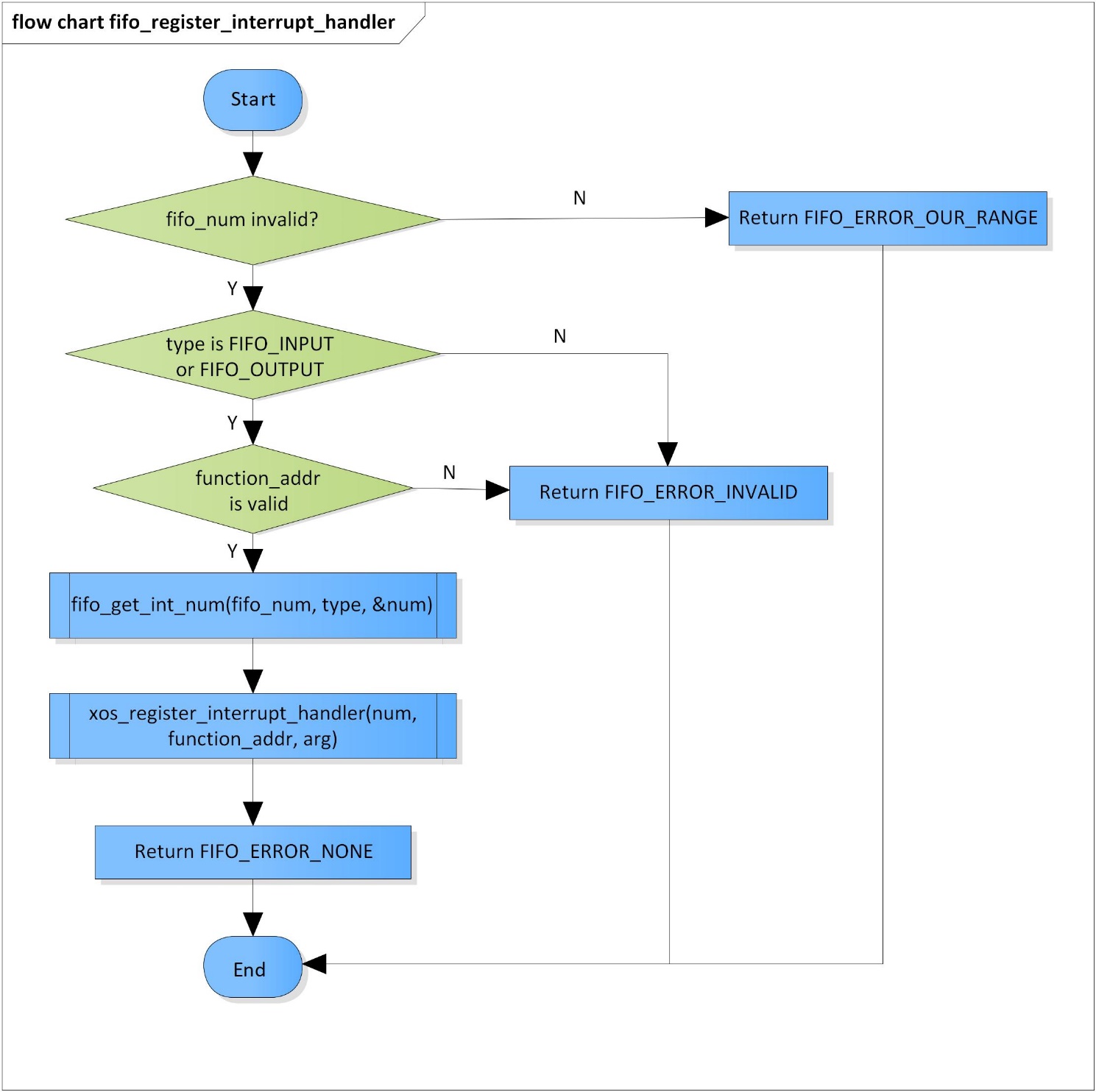
Figure 3‑4 fifo\_get\_int\_num flowchart

### fifo\_register\_interrupt\_handler

DD\_PLG\_RDR\_06\_005

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_register\_interrupt\_handler(fifo\_modules fifo\_num, fifo\_type type, pVOID function\_addr, pVOID arg) | | | |
| **Function** | This function is to register interrupt handler for FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| pVOID | function\_addr | I | Pointer to handler function |
| pVOID | arg | I | Argument passed to handler |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type or function\_addr is invalid | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_register\_interrupt\_handler command processing:   - Register interrupt handler for FIFO | | | |

[Covers: FD\_PLG\_RDR\_005]

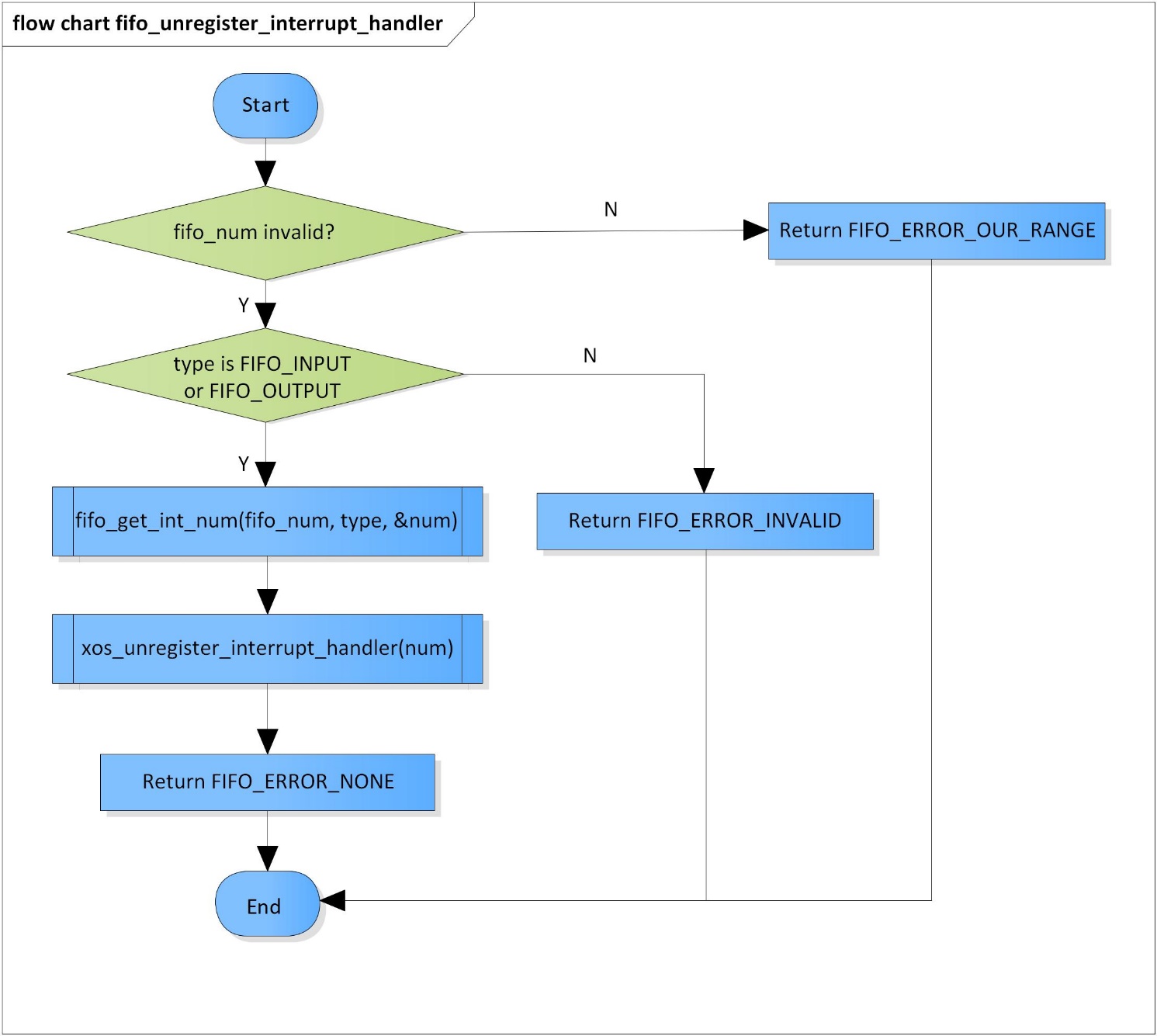
Figure 3‑5 fifo\_register\_interrupt\_handler flowchart

### fifo\_unregister\_interrupt\_handler

DD\_PLG\_RDR\_06\_006

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_unregister\_interrupt\_handler(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to unregister interrupt handler for FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_unregister\_interrupt\_handler command processing:   - Unregister interrupt handler for FIFO | | | |

[Covers: FD\_PLG\_RDR\_005, FD\_PLG\_RDR\_014, FD\_PLG\_RDR\_032, FD\_PLG\_RDR\_043]

Figure 3‑6 fifo\_unregister\_interrupt\_handler flowchart

### fifo\_disable\_interrupt

DD\_PLG\_RDR\_06\_007

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_disable\_interrupt(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to disable interrupt for FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_disable\_interrupt command processing:   - Disable FIFO interrupt | | | |

[Covers: FD\_PLG\_RDR\_005, FD\_PLG\_RDR\_014, FD\_PLG\_RDR\_032, FD\_PLG\_RDR\_043]

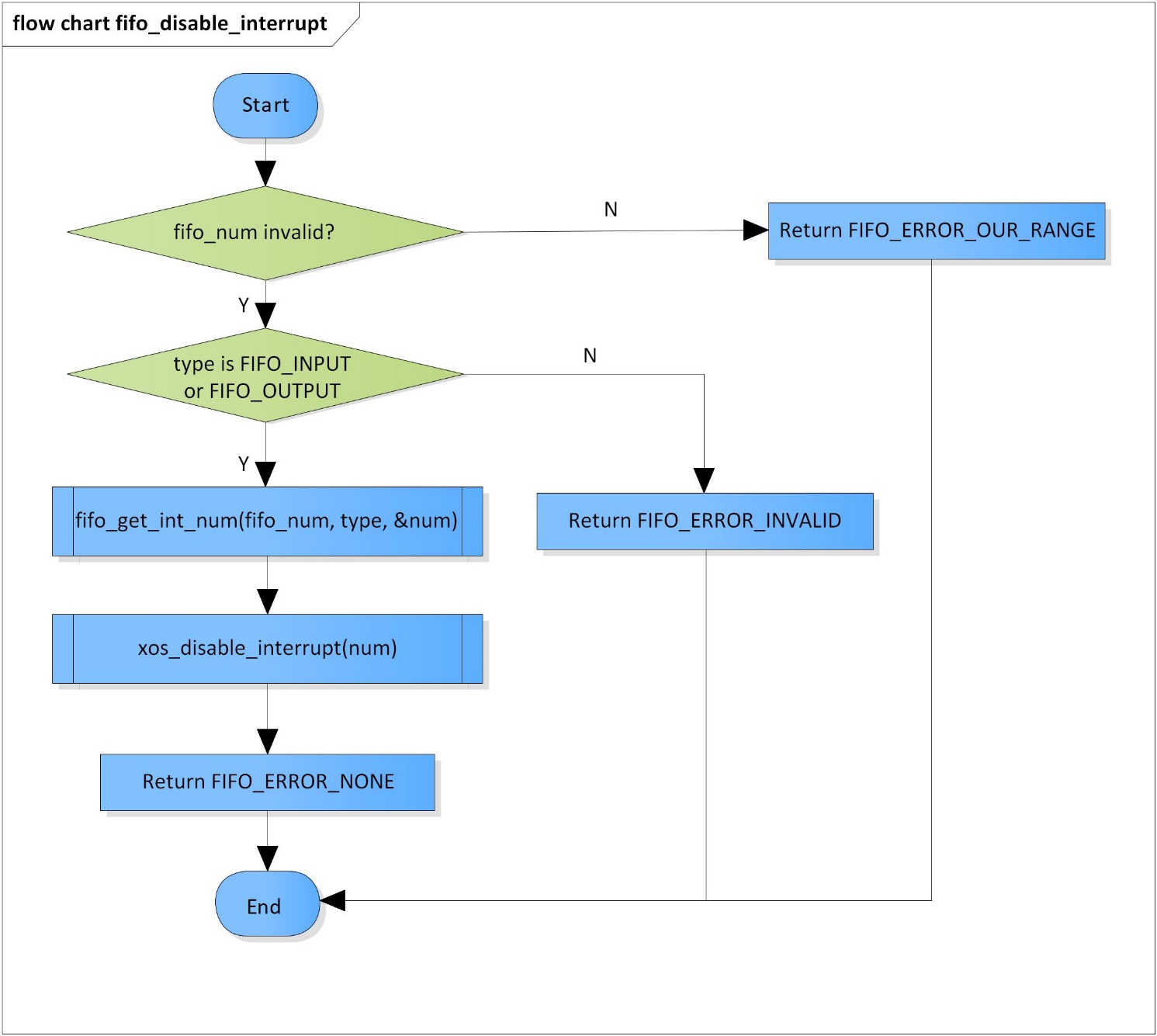


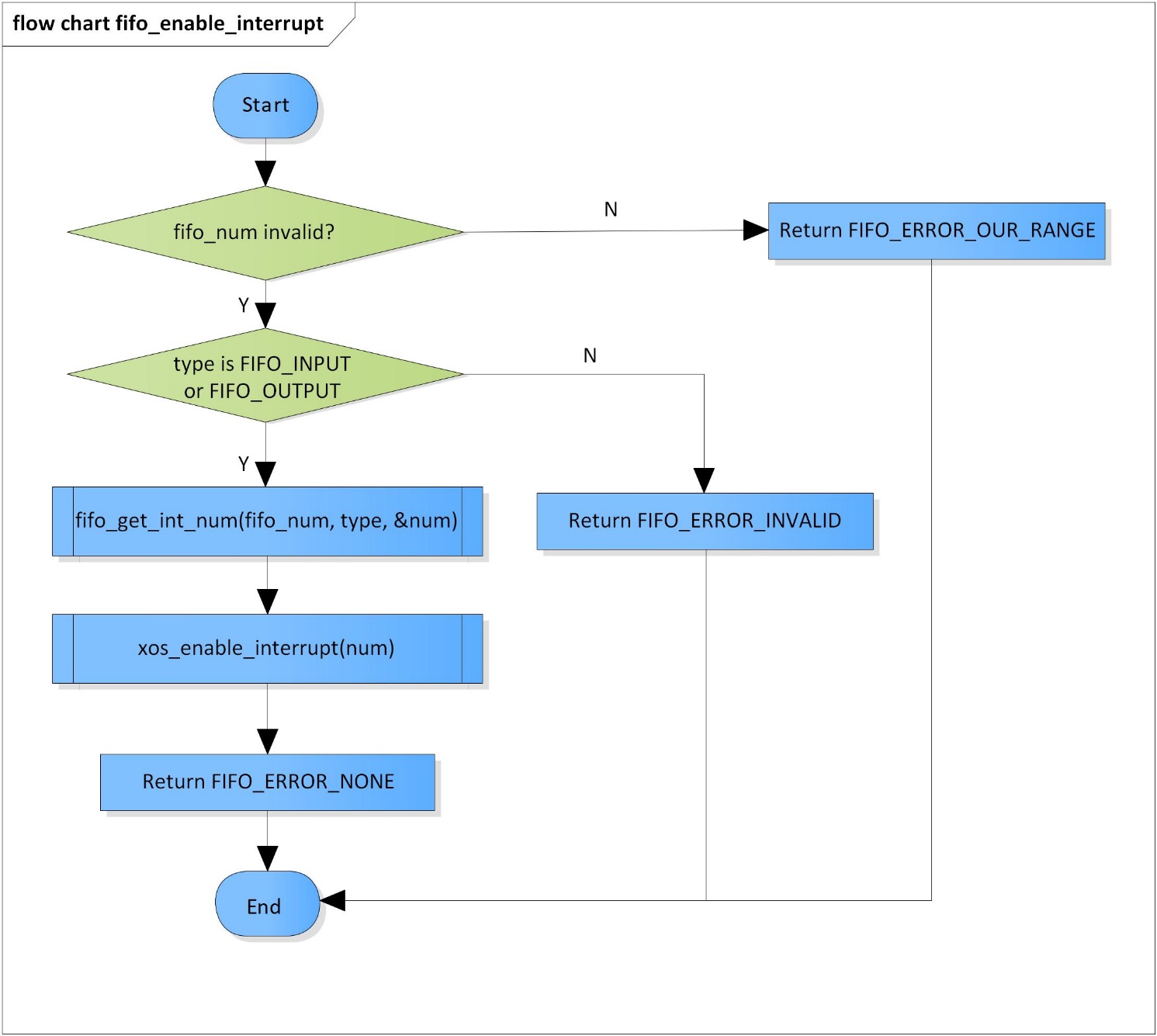
Figure 3‑7 fifo\_disable\_interrupt flowchart

### fifo\_enable\_interrupt

DD\_PLG\_RDR\_06\_008

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_enable\_interrupt(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to enable interrupt for FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_enable\_interrupt command processing:   - Enable FIFO interrupt | | | |

[Covers: FD\_PLG\_RDR\_005]

Figure 3‑8 fifo\_enable\_interrupt flowchart

### fifo\_clear\_interrupt

DD\_PLG\_RDR\_06\_009

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_clear\_interrupt(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to clear FIFO interrupt. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_clear\_interrupt command processing:   - Clear FIFO interrupt | | | |

[Covers: FD\_PLG\_RDR\_005]

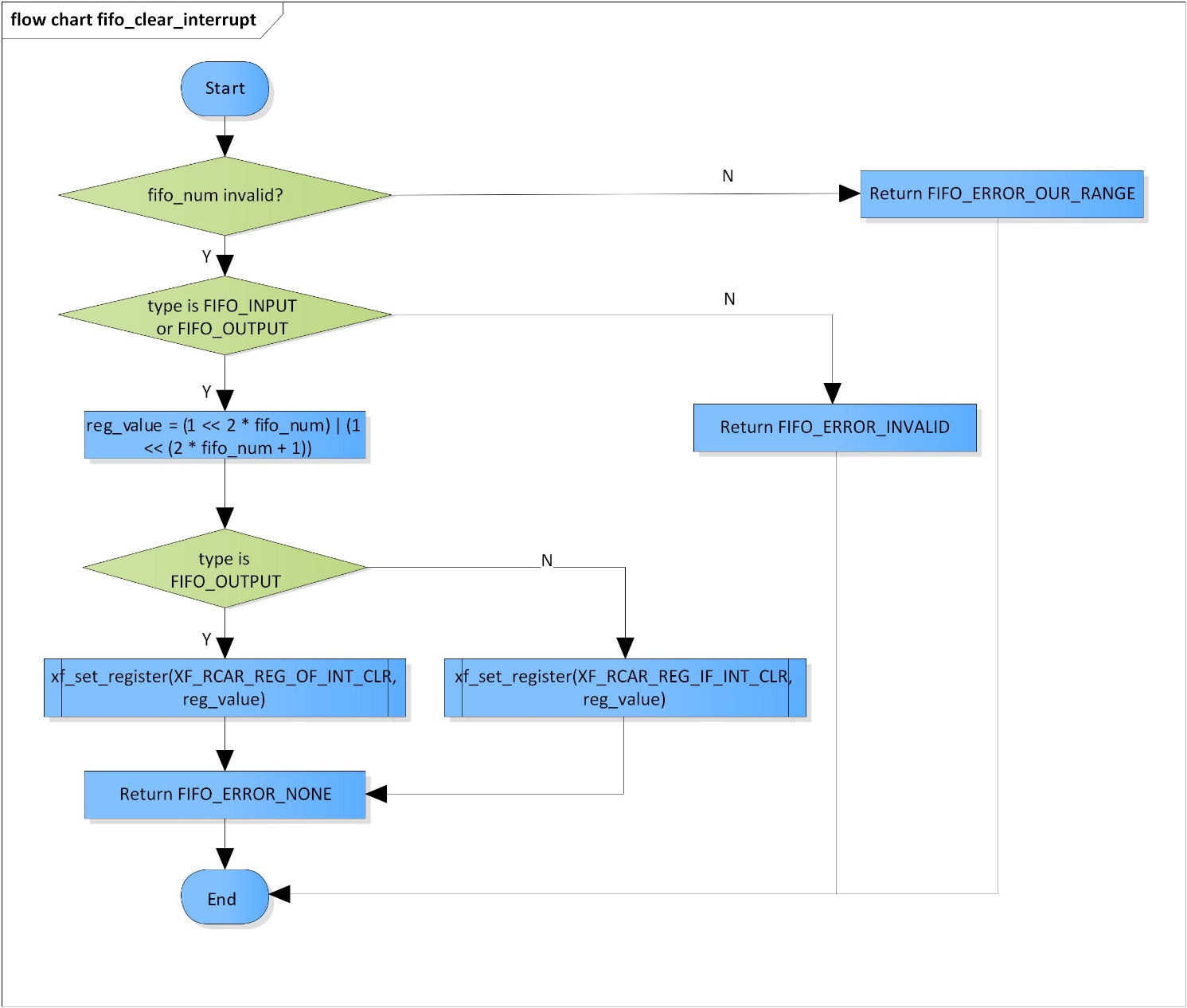


Figure 3‑9 fifo\_clear\_interrupt flowchart

### fifo\_stop

DD\_PLG\_RDR\_06\_010

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_stop(fifo\_modules fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to stop FIFO. | | | |
| **Arguments** | Type | Name | I/O | Description |
| fifo\_modules | fifo\_num | I | FIFO module  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_stop command processing:   - Stop FIFO operation | | | |

[Covers: FD\_PLG\_RDR\_005, FD\_PLG\_RDR\_014, FD\_PLG\_RDR\_032, FD\_PLG\_RDR\_043]

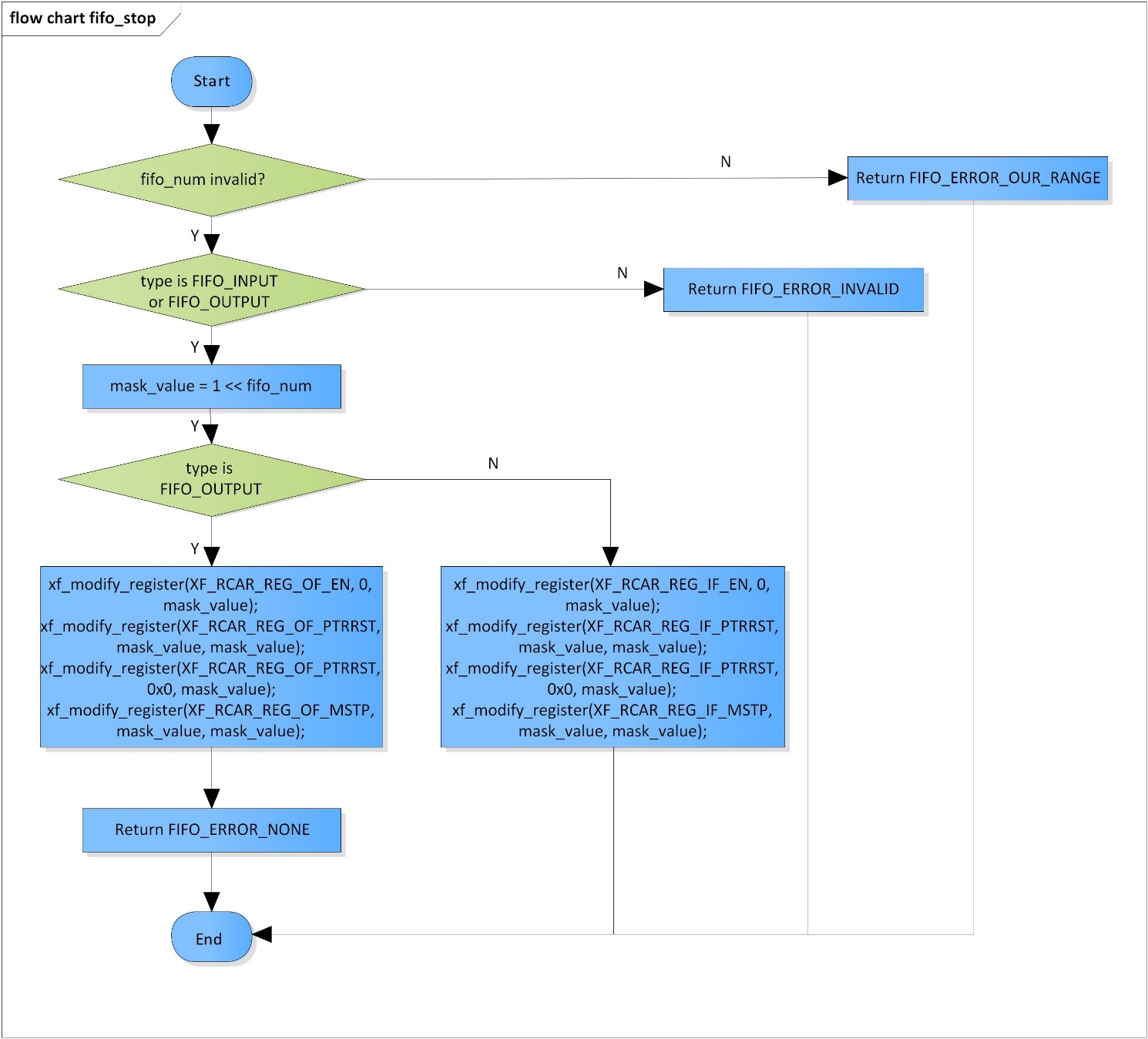


Figure 3‑10 fifo\_stop flowchart

### fifo\_check\_available

DD\_PLG\_RDR\_06\_011

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Syntax** | inline fifo\_error\_code fifo\_check\_available(UWORD32 \*fifo\_num, fifo\_type type) | | | |
| **Function** | This function is to check availability of FIFOs and choose an available one for operation. | | | |
| **Arguments** | Type | Name | I/O | Description |
| UWORD32 \* | fifo\_num | I/O | Pointer to FIFO number  Valid range: [0: 3] |
| fifo\_type | type | I | FIFO type  Valid values:  FIFO\_OUTPUT  FIFO\_INPUT |
| **Return value** | FIFO\_ERROR\_OUT\_RANGE | | FIFO module is invalid | |
| FIFO\_ERROR\_INVALID | | FIFO type is invalid | |
| FIFO\_ERROR\_BUSY | | No available FIFO module | |
| FIFO\_ERROR\_NONE | | Normal end | |
| **Description** | * fifo\_check\_available command processing:   - Check availability of FIFOs  - Choose an available one for operation | | | |

[Covers: FD\_PLG\_RDR\_005]

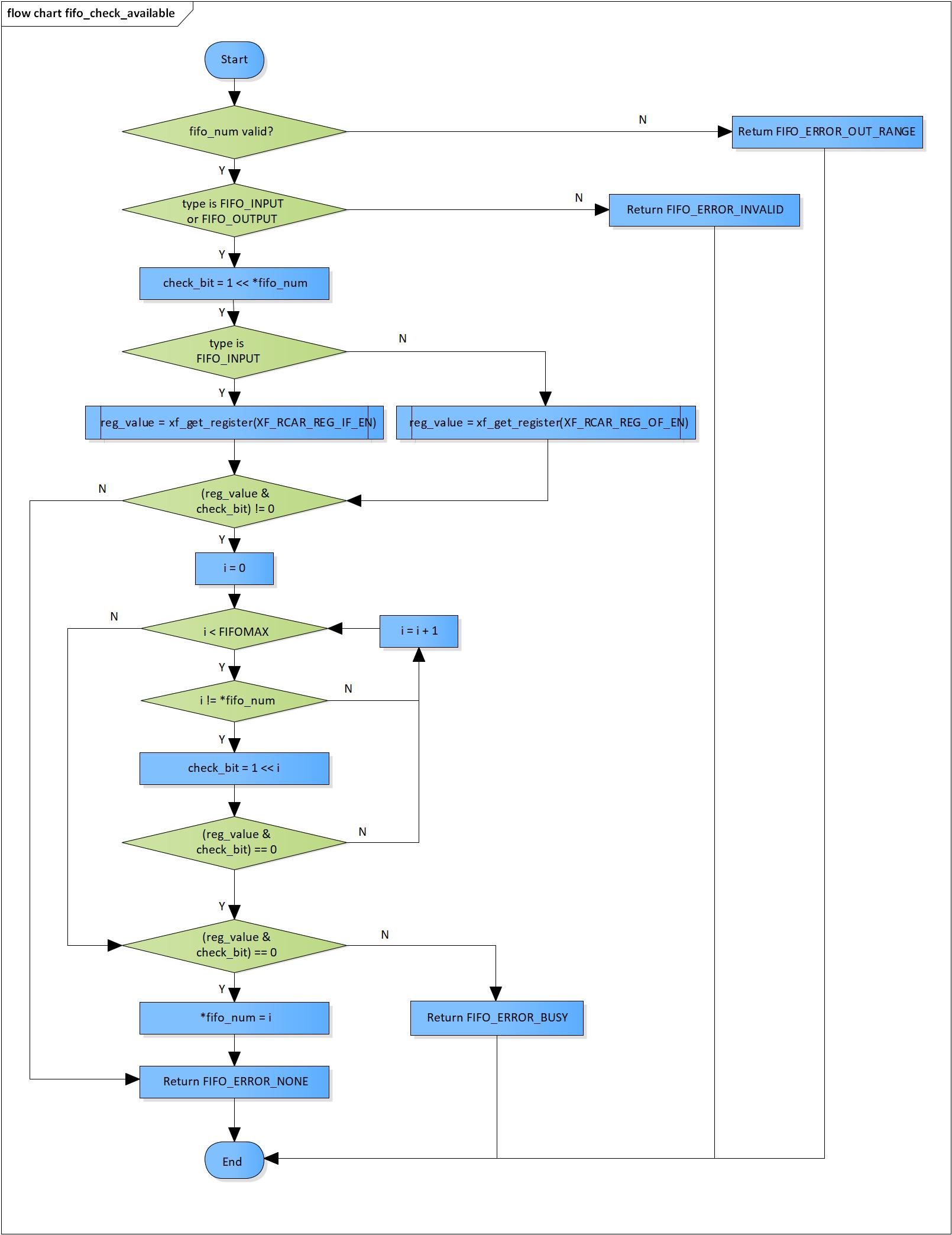


Figure 3‑11 fifo\_check\_available flowchart

# Revision history

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Version** | **Date** | **Page** | **Content** | **Approved** | **Changed** |
| 1.0.0 | Nov 14 2018 | - | First Edition issued | Vu Phan | Vu Phan |
| 1.1.0 | Dec 10 2018 | - | Add traceability ID | Vu Phan | Ngu Pham |
| 1.2.0 | Jan 03, 2019 | - | Add range for input parameters | Vu Phan | Tien Tran |