			VERIFICATION PLAN				Create by: Nguyen Van Huy
Section 1.	Main Title Register test Read default value of register	Sub Tile	Description 1. Walt for reset and clock stable.	Testname	Method	Status	Remak
			2. Read value for register: MDR, DLL, DLH, LCR, IER, FSR, TBR, RBR Pass condition: data matching with default value	uartip_read_default_value_test	Direct	PASS	
1.2	Write and Read function for reg	jister	What for reset and clock stable. Write and read 1's and 5's in each bit of the registe. For registent(D, DLL, DLH, DCR, EER. Pass condition: data matching between value write and value read	uartip_reg_scan_test	Direct	PASS	
1.3	Write and read function for rsvd	d register	Wait for reset and clock stable. Write and read Reserved region register from address 0X020-0X3FF Pass condition: data read match value 32°FFFF_FFFF	uartip_rw_rsvd_reg_test	Direct	PASS	
12	Write and read function for FSR	R register	I Wall for reseal and clock stable. 2. Coordings the segues for the IX poor of the LUART IP by receive data. 3. Coorlings and LUART IP and LUART IV with different purely bit settings foo simulate a purely bit enror). 5. Seria research case in the PRO, poor of the LUART IV in the LUA	uarip_FSR_rog_loot	Direct	FAIL	
2.4	Transmission test Baud rate with 16x and 13x oversampling test	baud rate 2400 and 16x, 13x oversampling	Setting clock: Mode x16, baud rate 2400,4900,9900,19200,39400,76900,115200. Setting uarf frame: No/Even/Odd parity, 1/2stop bit, 5/6/7/6 data bit.	uartip_trans_baudrate2400_test	Direct, Checker	PASS	
		baud rate 4800 and 16x, 13x oversampling	Walt for reset and clock stable. Configure mode for UART sampling in register MDR(Mode x16). Configure divisor value in register DLL and register DLH (baurate cases a second sec	uartip trans baudrate4800 test	Direct. Checker	PASS	
		baud rate 9600 and 16x ,13x oversampling	Enable based generator at bit 5 (BGE) in register LCR. Corriguer UART PRAME in register LCR. Write data to buffer in register TBR	uarlip_trans_baudrate9600_test	Direct, Checker	PASS	
		baud rate 19200 and 16x, 13x oversampling	Second transfer 7. Corfigure mode for UART sampling in register MDR(Mode x13) 8. Corfigure divisor value in register DLL and register DLL H (baurate (200.0 4800,0800,1000,03400,7800),1000,1000,000,000,000,000,000,000,00				
		baud rate 38400 and 16x, 13x oversampling	Charles	uartip_trans_baudrate19200_test	Direct, Checker	PASS	
		baud rate 76800 and 16x, 13x oversampling	**Litting best sating environity shi compere data check partly bit check stop bit check start bit check **Litting best environity agent unit more boad rate check **Litting best environity agent unit more boad rate check **Litting best detect difference config	uartip_trans_baudrate38400_test	Direct, Checker	PASS	
		baud rate 115200 and 16x, 13x oversampling		uartip_trans_baudrate76800_test	Direct, Checker	PASS	
21	Uart IP basic function	1 stop bil. No parity bil. 5 data bit	Setting clock: Mode x16, baud rate 9600.	uartip_trans_baudrate115200_test	Direct, Checker	PASS	
2.5			Setting uart frame: No/Even/Odd parity, 1/2stop bit, 5/6/7/8 data bit.	uartip_trans_1stopbit_noparitybit_5databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, No parity bit, 6 data bit	Walt for reset and clock stable. Configure mode for LIART sampling in register MDR	uartip_trans_1stopbit_noparitybit_6databit_test	Direct, constrain random, checker	PASS	
1	1	1 stop bit, No parity bit, 7 data bit	Fest trainable 1. Wast for need and clock stable. 2. Corfigue mode for UART sampling in register MDR. 3. Corfligue of since value in register DLL and register DLH. 4. Enable baud generated in 5 (EGE) in register DLR. 5. Corfligue UART FERM MB in register DLR.	uartip_trans_1stopbit_noparitybit_7databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, No parity bit, 8 data bit	5. Configure UART FRAME in register LCR.	uartip_trans_1stopbit_noparitybit_8databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, Even parity bit, 5 data bit	e. write cara to buffer in register TBR (data causes the parity bit to be set to 1 or 0) Second transfer (checking No parity bit Not apply)	uartip trans 1stopbit evenparitybit 5databit test	Direct, constrain random, checker	FAIL	
	1	1 stop bit, Even parity bit, 6 data bit	Write data to buffer in register TBR (data causes the parity bit to be set to 1 or 0) Second transfer (checking No parity bit Not apply) Twite data to stiffer in register TBR (data causes the parity bit to be set to 0 or 1) Pass conditions: data Uart IP mathching Uart VIP, correct Start bit, Stop bit, Parity bit from transmission for			FAIL	
	1	1 stop bit, Even parity bit, 7 data bit	Checker	uartip_trans_1stopbit_evenparitybit_6databit_test	Direct, constrain random, checker	_	
			+ Uartip_test.uartip_env.uartip_sb: compere_data_check, parity_bit_check, stop_bit_check, start_bit_check + Uartip_test: detect_difference_config	uartip_trans_1stopbit_evenparitybit_7databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Even parity bit, 8 data bit		uartip_trans_1stopbit_evenparitybit_8databit_test	Direct, constrain random, checker	FAIL	
	1	1 stop bit, Odd parity bit, 5 data bit		uartip_trans_1stopbit_oddparitybit_5databit_test	Direct, constrain random, checker	FAIL	
	1	1 stop bit, Odd parity bit, 6 data bit		uartip_trans_1stopbit_oddparitybit_6databit_test	Direct, constrain random, checker	FAIL	
	1	1 stop bit, Odd parity bit, 7 data bit	1	uartip_trans_1stopbit_oddparitybit_7databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Even parity bit, 8 data bit	-	uartip_trans_1stopbit_oddparitybit_8databit_test	Direct, constrain random, checker	FAIL	
		2 stop bit, No parity bit, 5 data bit				PASS	
		2 stop bit. No parity bit. 6 data bit		uartip_trans_2stopbit_noparitybit_5databit_test	Direct, constrain random, checker	_	
				uartip_trans_2stopbit_noparitybit_6databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, No parity bit, 7 data bit		uartip_trans_2stopbit_noparitybit_7databit_test	Direct, constrain random, checker	PASS	
	1	2 stop bit, No parity bit, 8 data bit		uartip_trans_2stopbit_noparitybit_8databit_test	Direct, constrain random, checker	PASS	
	1	2 stop bit, Even parity bit, 5 data bit]	uartip_trans_2stopbit_evenparitybit_5databit_test	Direct, constrain random, checker	FAIL	
		2 stop bit, Even parity bit, 6 data bit	1	uartip_trans_2stopbit_evenparitybit_6databit_test	Direct, constrain random, checker	FAIL	
		2 stop bit, Even parity bit, 7 data bit	1	uartip trans 2stopbit evenparitybit 7databit test	Direct, constrain random, checker	FAIL	
	1	2 stop bit, Even parity bit, 8 data bit	1			_	
		2 stop bit, Odd parity bit, 5 data bit	-	uartip_trans_2stopbit_evenparitybit_8databit_test	Direct, constrain random, checker	PASS	
			-	uartip_trans_2stopbit_oddparitybit_5databit_test	Direct, constrain random, checker	FAIL	
		2 stop bit, Odd parity bit, 6 data bit		uartip_trans_2stopbit_oddparitybit_6databit_test	Direct, constrain random, checker	FAIL	
		2 stop bit, Odd parity bit, 7 data bit		uartip_trans_2stopbit_oddpantybit_7databit_test	Direct, constrain random, checker	FAIL	
		2 stop bit, Even parity bit, 8 data bit		uartip_trans_2stopbit_oddparitybit_8databit_test	Direct, constrain random, checker	PASS	
	FIFO test	FIFO full	1. VIM for resist and dock stable. 2. Configure mode for VIM Energing in legislar MIDE. 2. Configure mode for VIME Energing in legislar MIDE. 4. Enable bad generation at this S(BES) in regislar LCR. 5. Configure MIMET PRISAL in regislar LCR. WIMET PRISAL IN THE SECOND STABLE STABL	uardip_trans_2stophit_oddpartlybit_8databit_test	Direct	FAIL	
3.4	Reception test Baud rate with 16x and 13x	baud rate 2400 and 16x oversampling	Setting clock: Mode x16, baud rate 2400,4800,9600,19200,38400,76800,115200. Setting uset frame: No/Even/Odd parity, 1/2slop bit, 5/67/8 data bit.				
	oversampling test			uartip_recep_baudrate2400_test	Direct, Checker	PASS	
		baud rate 4800 and 13x oversampling	1. Wals for reset and clock stable. 2. Corfugne mode for URAT sampling in register MDR(Mode x16). 3. Corfugne divisor value in register DLL and register DLH bazariae (2004,0460 9060;1903,0460 7060;1905). 4. Enable baud persenter at this (80E) in register LCR. 5. Corfugne ULART PARME in register LCR.	uartip_recep_baudrate4800_test	Direct, Checker	PASS	
		baud rate 9600 and 16x oversampling	 Send random data to the RX port of the UART IP (data causes the parity bit to be set to 1 or 0). Read data from the RBR register. Second transfer 	uartio receo baudrate/9500 test	Direct. Checker	PASS	
		baud rate 19200 and 13x oversampling	Configure mode for UART sampling in register MDR/Mode x13. Configure vincor value in register DLL and register DLH (baurate (2400,4800,9800,19200,38400,78800,115200). Sent random data to the RX port of the UART IP (data causes the parity bit to be set to 0 or 1). Read data from the RRB register.	-			
		baud rate 38400 and 16x oversampling	11. Neuto data il mili de Not regisser Pasa conditions data Usar le mathoring Uart VIP. Checker: - Uartip_test.uartip_env.uartip_sb: compere_data_check. + Uartip_test_debet_difference_config	uartip_recep_baudrate19200_test	Direct, Checker	PASS	
		baud rate 76800 and 13x oversampling		uartip_recep_baudrate38400_test	Direct, Checker	PASS	
				uartip_recep_baudrate76800_test	Direct, Checker	PASS	
2.5	Uart IP basic function	1 stop bit, No parity bit, 5 data bit	Setting clock: Mode x16, baud rate 9600. Setting uart frame: No/Even/Odd partly, 1/2stop bit, 5/6/7/8 data bit. First transfer	uartip_recep_1stopbit_noparitybit_5databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, No parity bit, 6 data bit	1 Walt for reset and clock stable	uartip_recep_1stopbit_noparitybit_6databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, No parity bit, 7 data bit	Configure mode for UART sampling in register MDR. Configure divisor value in register DLL and register DLH.	uartip_recep_1stopbit_noparitybit_7databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, No parity bit, 8 data bit	4. Enable baud generator at bit 5 (BGE) in register LCR. 5. Configure UART FRAME in register LCR. 6. Send random data to the RX port of the UART IP.	uartip_recep_1stopbit_noparitybit_8databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, Even parity bit, 5 data bit	7. Read data from the RBR register	uartip_recep_1stopbit_evenparitybit_5databit_test	Direct, constrain random, checker	PASS	
	1	1 stop bit, Even parity bit, 6 data bit	Second transfer (checking No parity bit Not apply) 8. Send random data to the RX port of the UART IP. B. Dand dath from the PBP projetter.	uartip_recep_1stopbit_evenparitybit_6databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Even parity bit, 7 data bit	Read data from the RBR register Pass conditions: data Uart IP mathching Uart VIP, correct Start bit, Stop bit, Parity bit from transmission for ILIART VIP.	uartip_recep_1stopbit_evenparitybit_7databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Even parity bit, 8 data bit	UART VIP: Checker: + Uartip_test_uartip_env.uartip_sb: compere_data_check, parity_bit_check, stop_bit_check, start_bit_check	uartip_recep_1stopbit_evenparitybit_8databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Odd parity bit, 5 data bit	+ Uartip_test.uartip_enr.uartip_sb: compere_data_check, parity_bit_check, stop_bit_check, start_bit_check + Uartip_test: detect_difference_config			_	
		1 stop bit, Odd parity bit, 5 data bit	-	uartip_recep_1stopbit_oddparitybit_5databit_test	Direct, constrain random, checker	PASS	
			-	uartip_recep_1stopbit_oddparitybit_6databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Odd parity bit, 7 data bit		uartip_recep_1stopbit_oddparitybit_7databit_test	Direct, constrain random, checker	PASS	
		1 stop bit, Odd parity bit, 8 data bit		uartip_recep_1stopbit_oddparitybit_8databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, No parity bit, 5 data bit		uartip_recep_2stopbit_noparitybit_5databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, No parity bit, 6 data bit		uartip_recep_2stopbit_noparitybit_6databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, No parity bit, 7 data bit		uartip_recep_2stopbit_noparitybit_7databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, No parity bit, 8 data bit	1	uartip_recep_2stopbit_noparitybit_8databit_test	Direct, constrain random, checker	PASS	
	1	2 stop bit, Even parity bit, 5 data bit	1	uartip_recep_2stopbit_evenparitybit_5databit_test	Direct, constrain random, checker	PASS	
1	1	2 stop bit, Even parity bit, 6 data bit	1	uartip_recep_2stopbit_evenparitybit_6databit_test	Direct, constrain random, checker	PASS	
	1	2 stop bit, Even parity bit, 7 data bit	1		Direct, constrain random, checker Direct, constrain random, checker	PASS	
	1	2 stop bit. Even parity bit. 8 data bit	-	uartip_recep_2stopbit_evenparitybit_7databit_test		_	
			-	uartip_recep_2stopbit_evenparitybit_8databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, Odd parity bit, 5 data bit	1	uartip_recep_2stopbit_oddparitybit_5databit_test	Direct, constrain random, checker	PASS	
	1	2 stop bit, Odd parity bit, 6 data bit		uartip_recep_2stopbit_oddparitybit_6databit_test	Direct, constrain random, checker	PASS	
	1	2 stop bit, Odd parity bit, 7 data bit		uartip_recep_2stopbit_oddparitybit_7databit_test	Direct, constrain random, checker	PASS	
		2 stop bit, Even parity bit, 8 data bit]	uartip_recep_2stopbit_oddparitybit_8databit_test	Direct, constrain random, checker	PASS	
_						-	

3.4	Transmission and Reception to Baud rate with 16x and 13x	st baud rate 2400 and 16x oversampling	Setting clock: Mode x16, baud rate 2400,4800,9600,19200,38400,76800,115200. Setting uart frame: No/Even/Odd parity, 1/2stop bit, 5/6/7/8 data bit.				
	oversampling test		Setting uart frame: No/Even/Odd parity, 1/2stop bit, 5/6/7/8 data bit. First transfer 1. Walf for reset and clock stable.	uartip_trans_and_recep_baudrate2400_test	Direct	PASS	
		baud rate 4800 and 13x oversampling	2 Configure mode for LIART complex in mainter MDR/Mode v16)				
		Date and the second of the second	Configure for value in register DLL and register DLH (baurate (2400, 4800, 5800, 19200, 3400, 78800, 115200). 4. Enable baud generator at bit 5 (GEG) in register LCR. 5. Configure UART FRAME in register LCR.	uartip_trans_and_recep_baudrate4800_test	Direct	PASS	
			Configure UART FRAME in register LCR. Milita John to buffer in register LCR.				
		baud rate 9600 and 16x oversampling	Write data to buffer in register TBR Send random data to the RX port of the UART IP. Read data from the RBR register	uartio trans and recep baudrate9600 test	Direct	PASS	
			Second transfer 9. Configure mode for UART sampling in register MDR/Mode x13)	uamp_trans_and_recep_baudrateseuu_test	Direct	PASS	
		baud rate 19200 and 13x oversampling	10. Configure inducer value in register DLL and register DLH (baurate (2400.4800,9600,19200,38400,76800,115200).				
			11. Write data to buffer in register TBR	uartip_trans_and_recep_baudrate19200_test	Direct	PASS	
		baud rate 38400 and 16x oversampling	12. Used relation to the Poly port in Bullet 1. 3. Read data from the RBR register Pass conditions: data User IP mathring User VIP, correct Start bit, Stop bit, Parity bit from transmission for USART VIP. Data is not changed within the bit duration.				
		and the sorto and tox ordinallying		uartip_trans_and_recep_baudrate38400_test	Direct	PASS	
			- Uartip Lest uartip_env.uartip_sb: compere_data_check, parity_bit_check, stop_bit_check, start_bit_check. - Uartip_test.env.uart_agent.uart_mort_baud_rate_check - Uartip_test.env.uart_agent.uart_mort_baud_rate_check - Uartip_test.env.uart_set.env.uar				
		baud rate 76800 and 13x oversampling	+ Uartip_test: detect_difference_config.				
				uartip_trans_and_recep_baudrate76800_test	Direct	PASS	
		baud rate 115200 and 16x oversampling	-				
				uartip_trans_fifo_full_test	Direct	PASS	
25	Uart IP basic function	1 stop bit, No parity bit, 5 data bit	Setting clock Mode v16 haud rate 9600				
1.0		1 stop bit, No parity bit, 6 data bit	Setting uart frame: No/Even/Odd parity, 1/2stop bit, 5/6/7/8 data bit. First transfer	uartip_trans_and_recep_1stopbit_noparitybit_5databit_test	Direct	PASS	
		1 1 1	Walt for reset and clock stable. Configure mode for UART sampling in register MDR.	uartip_trans_and_recep_1stopbit_noparitybit_6databit_test	Direct	PASS	
		1 stop bit, No parity bit, 7 data bit	Configure divisor value in register DLL and register DLH.	uartip_trans_and_recep_1stopbit_noparitybit_7databit_test	Direct	PASS	
		1 stop bit, No parity bit, 8 data bit	So Configure UART FRAME in register LCR. So Configure UART FRAME in register LCR. Send nandom data to the RX port of the UART IP. Read data from the RBR register	uartip_trans_and_recep_1stopbit_noparitybit_8databit_test	Direct	PASS	
		1 stop bit, Even parity bit, 5 data bit	7. Read data from the RBR register 8. Send random data to the RX port of the UART IP.	uartip_trans_and_recep_1stopbit_evenparitybit_5databit_test	Direct	FAIL	
		1 stop bit, Even parity bit, 6 data bit		uartip_trans_and_recep_1stopbit_evenparitybit_6databit_test	Direct	FAIL	
		1 stop bit, Even parity bit, 7 data bit	Second transfer (checking No parity bil Not apply) Second transfer (checking No parity bil Not apply) Second transfer of the PKP port of the UART IP. I. Read data from the RBR register	uartip trans and recep 1stopbit evenparitybit 7databit test	Direct	PASS	
		1 stop bit, Even parity bit, 8 data bit	11. Read data from the RBX register 12. Send random data to the RX port of the UART IP. 13. Read data from the RBR register	uartip trans and recep 1stopbit evenpantlybit 8databit test	Direct	FAIL	
		1 stop bit, Odd parity bit, 5 data bit	Pass conditions: data Uart IP mathching Uart VIP, correct Start bit, Stop bit, Parity bit from transmission for UART VIP.		Direct	FAIL	
		1 stop bit, Odd parity bit, 6 data bit	Checker: + Uartip_test.uartip_env.uartip_sb: compere_data_check, parity_bit_check, stop_bit_check, start_bit_check	uartip_trans_and_recep_1stopbit_oddparitybit_5databit_test		_	
		1 stop bit, Odd parity bit, 7 data bit	+ Uartip_test.uartip_env.uarip_so: compere_data_cneck, parity_bit_cneck, stop_bit_cneck, start_bit_cneck + Uartip_test: detect_difference_config	uartip_trans_and_recep_1stopbit_oddparitybit_6databit_test	Direct	FAIL	
			_	uartip_trans_and_recep_1stopbit_oddparitybit_7databit_test	Direct	PASS	
		1 stop bit, Odd parity bit, 8 data bit		uartip_trans_and_recep_1stopbit_oddparitybit_8databit_test	Direct	FAIL	
		2 stop bit, No parity bit, 5 data bit		uartip_trans_and_recep_2stopbit_noparitybit_5databit_test	Direct	PASS	
		2 stop bit, No parity bit, 6 data bit	7	uartip_trans_and_recep_2stopbit_noparitybit_6databit_test	Direct	PASS	
		2 stop bit, No parity bit, 7 data bit	1	uartip_trans_and_recep_2stopbit_noparitybit_7databit_test	Direct	PASS	
		2 stop bit, No parity bit, 8 data bit	1	uartip_trans_and_recep_2stopbit_noparitybit_8databit_test	Direct	PASS	
		2 stop bit, Even parity bit, 5 data bit	-	uarip trans and recep_stopole reparitybit 5databit test	Direct	FAIL	
		2 stop bit. Even parity bit. 6 data bit				-	
		2 stop bit, Even parity bit, 7 data bit	-	uartip_trans_and_recep_2stopbit_evenparitybit_6databit_test	Direct	FAIL	
				uartip_trans_and_recep_2stopbit_evenparitybit_7databit_test	Direct	FAIL	
		2 stop bit, Even parity bit, 8 data bit		uartip_trans_and_recep_2stopbit_evenparitybit_8databit_test	Direct	PASS	
		2 stop bit, Odd parity bit, 5 data bit		uartip_trans_and_recep_2stopbit_oddparitybit_5databit_test	Direct	FAIL	
		2 stop bit, Odd parity bit, 6 data bit		uartip_trans_and_recep_2stopbit_oddparitybit_6databit_test	Direct	FAIL	
		2 stop bit, Odd parity bit, 7 data bit		uartip_trans_and_recep_2stopbit_oddparitybit_7databit_test	Direct	FAIL	
		2 stop bit, Even parity bit, 8 data bit	1	uartip_trans_and_recep_2stopbit_oddparitybit_8databit_test	Direct	PASS	
	Error handling test Access reserved address	•					
0.1							
			Write and read Reserved region register from address 0X020-0X3FF Pass condition: HRESP signal equa to 1		Direct	PASS	
			Water for reset and circle states. 2. Write and read Reserved region register from address 0X020-0X3FF Pass condition: HRESP signal equa to 1		Direct	PASS	
	Interrupt and FIFO status test	Even parity error	Write and read Reserved region register from address 0X020-0X3FF Pass condition: HRESP signal equa to 1		Direct	PASS	- The Internuct and Parthy Error: Status of the FSR are not working and remain at their
		Even parity error	2. Write and made Reserved region register from address 0XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		Direct	PASS	- The Interrupt and Parthy. Error. Status of the FSR are not working and remain at their default values. The Interrupt and Parthy. Error, Status are always 0
	Interrupt and FIFO status test	Even parity error	2. With a and rade Reserved region register from address 01000-0100FF Pass condition. PRESP singlet register for maddress 01000-0100FF 1. Configure the register for the RX port of the UARET IP to receive data. 2. Configure the ER Register for Examinary parties of the RASE of the		Direct	PASS	-The Interrupt and Party_Error_Status of the FSR are not working and remain at their default-values. The Interrupt and Party_Error_Status are always 0
	Interrupt and FIFO status test	Even parity error	2. With a and rade Reserved region register from address 01000-0100FF Pass condition. PRESP singlet register for maddress 01000-0100FF 1. Configure the register for the RX port of the UARET IP to receive data. 2. Configure the ER Register for Examinary parties of the RASE of the	uarigo interrupat enable everspountly foot	Direct Direct, Checker	PASS	The Internet and Party, Error, States of the FSR are not working and remain all their ordinal values. The Internet and Party, Error, States are always 0
	Interrupt and FIFO status test	Even parity error	2. With a set of used Received region register from address ORCOD-DCFF Person condition (FRSE) gaingle state 1 1 Codingue the register for the DC part of the LURET IP to accorde data. 2. Codingue the Earl register for Enable parity smort Hardware interrupt. 3.1. CRECK is interrupt and parity remore than shorted LURET IP to accorde data. 3.1. CRECK is interrupt and parity remore states before LURET IP revolves data. 3.1. CRECK is interrupt and parity remove states before LURET IP revolves data. 3.1. CRECK is interrupt and parity remove states and the control parity with to be set to 1 and 0; 3.1. CRECK is interrupt and parity remove states. 3.2. CRECK is interrupt and parity remove states. 3.3. CRECK is interrupt and parity remove states. 3.4. Resident and the states of the states. 3.5. CRECK is interrupt. 3.6.	usify_intempt_enable_everpasity_lost			-The Internet and Party _Eron _State of the FSR and not exciting and remain at their oldest house. The Internet and Party_Stinz_State are always to
	Interrupt and FIFO status test	Even parity error	2. With a set of used Received region register from address ORCOD-DCFF Person condition (FRSE) gaingle state 1 1 Codingue the register for the DC part of the LURET IP to accorde data. 2. Codingue the Earl register for Enable parity smort Hardware interrupt. 3.1. CRECK is interrupt and parity remore than shorted LURET IP to accorde data. 3.1. CRECK is interrupt and parity remore states before LURET IP revolves data. 3.1. CRECK is interrupt and parity remove states before LURET IP revolves data. 3.1. CRECK is interrupt and parity remove states and the control parity with to be set to 1 and 0; 3.1. CRECK is interrupt and parity remove states. 3.2. CRECK is interrupt and parity remove states. 3.3. CRECK is interrupt and parity remove states. 3.4. Resident and the states of the states. 3.5. CRECK is interrupt. 3.6.	uartig_relampe_entable_everpartiy_test			-The interrupt and Purity. Error, Status of the FSR are not working and remain at their odd and visites. The interrupt and Purity. Error, Status are always 0.
	Interrupt and FIFO status test	Even pashly entor	2. With a cert of used Researced region register from address ORCODO-DICFF Process condition. PRESS goal of early in 1 1. Configure the register for the IXX port of the LARST IP to receive data. 2. Configure the Register to Exclude parity more Hardware interrupt. 3. Event contained the Register to Exclude parity more Hardware interrupt. 3. Event contained and parity, more statement before LARST IP processed data. 3. Event contained and parity, more statement before LARST IP proceeds data. 3. Event contained and parity, more statement LARST IP proceeds data. 3. Event contained and parity, more statement LARST IP proceeds and the REGIST Proceeds AND Proceeds and the REGIST Proceeds AND Proceeds and the REGIST Proceeds AND Procee	sarting_relatingst_entables_everparting_last			The Internet and Party, Error, States of the FSR are not working and remain all their ordinal volume. The Internet and Party, Error, States are always 0
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6.1	listened and FFO status lest Enable Parky bit error	Odd partly error FiFO empty	2. Within an of under Beasened region register from address ORDOD-OLOFF Prices condition. PIPES grad drugs to 1. 1.Configure the register for the DX port of the LUART IF to receive data. 2.Configure the register for the DX port of the LUART IF to receive data. 2.Configure the register for the DX port of the LUART IF to receive data. 2.2. Configure the ER register for Ending be partly error. Exhaust enterprise the prices of the LUART IF to receive data. 2.3. Bord various makes to the RX port of the LUART IF the class causes the partly bit to be set to 1 and 0). 3.4. Road data from the SRIF register for called and the DX FPF CL. 4.4. Road data from the SRIF register for called and the DX FPF CL. 4.4. Source controls that is the RX port of the LUART IF place causes the partly bit to be set to 1 and 0). 4.4. Source controls called the DX PX port of the LUART IF place causes the partly bit to be set to 1 and 0). 4.4. Source controls called the RX port of the LUART IF place causes the partly bit to be set to 1 and 0). 4.4. Source controls called the RX port of the LUART IF place causes the partly bit to be set to 1 and 0). 4.4. Fine data from the RX Riff register for called the partly genery. Settled the RX port of the LUART IF place causes the partly bit to be set to 1 and 0). 4.4. Fine data from the RXIF register to called the RX PX FEO. 4.7. Fine data from the RXIF register to called the RX FEF CO settled to the RX PX FEO. 4. Ludge place the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive data. 2. Configure the RX port of the LUART IF to receive da	uarity_interrupt_evable_oddparity_test	Direct, Checker Direct, Checker	FAIL	The Internet and Party, Error, States of the FSR are not working and remain all their odd and values. The Internet and Party, Error, States are always 0 or an extension of the Internet and Party, Error, States are always 0. The Internet Internet on Commonly, but the rx persy, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx empty, states of the FSR is functioning incomestly. The rx empty and 0 when the FFO contains data.
6.1	listened and FFO status lest Enable Parky bit error	Odd partly error FiFO empty	2. Within an of under Beasened region register from address ORDOD-OLOFF Process condition. PEPES grad or gas 1. 1. Configure the register for the RX port of the LUART IF to receive data. 2. Configure the register for the RX port of the LUART IF to receive data. 2. Configure the register for the RX port of the LUART IF to receive data. 3. Event invariance and part and part and part to the receiver of the LUART IF to receive data. 3. Event invariance and part and part and part to the receiver of the LUART IF the case the part to the part to be set to 1 and 0). 3. Event invariance and part and part and part to the RX port of the LUART IF the case the part to the part to the part of the LUART IF the case the part to the part to the part of the LUART IF the case the part to the part to the part of the LUART IF the part to the RX port of the LUART IF the case the part to the part to the part of the part of the LUART IF the part to the RX port of the LUART IF the part to the RX port of the LUART IF the case the part to the part of the part of the LUART IF the case the part of the luar to the RX port of the LUART IF the case the part of the luar to the l	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The Internet and Party, Error, States of the FSR are not working and remain all their odd and values. The Internet and Party, Error, States are always 0 or an extension of the Internet and Party, Error, States are always 0. The Internet Internet on Commonly, but the rx persy, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx empty, states of the FSR is functioning incomestly. The rx empty and 0 when the FFO contains data.
6.1	listened and FFO status lest Enable Parky bit error	Odd partly error FiFO empty	2. Within and noted Researced region register from address ORCOS-DICKET Researced Control (PECE) grade of year 1. 1. Configure the register for the RX port of the LMRT IF to receive data. 2. Configure the register for the RX port of the LMRT IF to receive data. 2. Configure the register for the RX port of the LMRT IF to receive data. 3. Executive control of the LRT register to Exclude partly receive the register of the LMRT IF the control of the LMRT IF the control of the LMRT IF THE LMRT	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The Internet and Party, Error, States of the FSR are not working and remain all their odd and values. The Internet and Party, Error, States are always 0 or an extension of the Internet and Party, Error, States are always 0. The Internet Internet on Commonly, but the rx persy, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx empty, states of the FSR is functioning incomestly. The rx empty and 0 when the FFO contains data.
6.1	listened and FFO status lest Enable Parky bit error	Odd partly error FiFO empty	2. With an of under Beasened region register from address ORDOD-DOCFF Process condition. PIPES grad upon to 1 1.Configure the register for the RX port of the LUART IP to receive data. 2.Configure the register for the RX port of the LUART IP to receive data. 2.Configure the RT register for Ending partly more Handbase intering. 3.2. South cruismon data to the RX port of the LUART IP to receive data. 2.3. South cruismon data to the RX port of the LUART IP to receive data. 3.2. South cruismon data to the RX port of the LUART IP to receive data. 3.2. South cruismon data to the RX port of the LUART IP to date causes the partly bit to be set to 1 and 0). 3.3. Receive data to the RX port of the LUART IP to the causes the partly bit to be set to 1 and 0). 4. Receive data to the RX port of the LUART IP to the RX port of the RX p	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The Internet and Party, Error, States of the FSR are not working and remain all their odd and values. The Internet and Party, Error, States are always 0 or an extension of the Internet and Party, Error, States are always 0. The Internet Internet on Commonly, but the rx persy, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx, empty, states of the FSR is functioning incomestly, the rx, empty, states of the FSR is functioning incomestly. The rx empty, states of the FSR is functioning incomestly. The rx empty and 0 when the FFO contains data.
6.1	listened and FFO status lest Enable Parky bit error	Odd partly error FiFO empty	2. With an of horse description project from address ORDDO-DOFF Process condition. PERPS grad upon to 1 1.Configure the register for the RX port of the LMRT IF to receive data. 2.Configure the register for the RX port of the LMRT IF to receive data. 2.Configure the register for the RX port of the LMRT IF to receive data. 3.2. Exercit received and the RX port of the LMRT IF to receive data. 3.3. Exercit received and the RX port of the LMRT IF the class causes the pulmp like to be set to 1 and 0). 3.3. Exercit received and the RX port of the LMRT IF the class causes the pulmp like to be set to 1 and 0). 3.4. For the class cause of the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the pulmp like the RX port of the LMRT IF the class causes the LMRT IF the received hexapter causes the LMRT IF the received hexapter causes the LMRT IF the received hexapter causes the LMRT IF the received data. 1.Configure the register for the RX port of the LMRT IF the received data. 1.Configure the register for the RX port of the LMRT IF the received data. 1.Configure the register for the RX port of the LMRT IF the received data. 1.Configure the register for the RX port of the LMRT IF the received data. 2.Configure the register for the RX port of the LMRT IF the received data. 3.Configure the register for the RX port of the LMRT IF the received data. 4.Configure the r	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The interrupt and Party_Error_States of the FSRI are not working and remain all their obtaint values. The interrupt and Party_Error_States are always 0. The interrupt functions consensity, but the no energy_states of the FSRI is functioning incommonly. The no energy_states by these for function invented it is 1 when the FPC0 is empty and 0 when the FPC0 contains data. The interrupt and the FRI, FIAL States of the FSRI function connectly, but the experiments of the FRI is the interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI. Energy_States has changed over thought the bit was not created.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an of under Beasened region register from address ORDOD-DOCFF Prices condition. PIPES yeard days to 1. 1.Configure the register for the DX port of the LUART IF to receive data. 2.Configure the register for the DX port of the LUART IF to receive data. 2.Configure the Register for Ending be partly error. Falled are interested. 3.2. Sent invalidation and the EX port of the LUART IF to receive data. 3.2. Sent invalidation and the DX port of the LUART IF to receive data. 3.2. Sent invalidation and the DX port of the LUART IF the class causes the partly bit to be set to 1 and 0). 3.3. Report common time IRST register to End and the DX PIPE. 4. Report LUART IF and LUART IF the different partly bit in this play. 4. Sent control and the DX port of the LUART IF the class causes the partly bit to be set to 1 and 0). 4. Sent control and the DX port of the LUART IF the class causes the partly bit to be set to 1 and 0). 4. Sent control and the DX port of the LUART IF the Cause causes the partly bit to be set to 1 and 0). 4. Sent control and the DX port of the LUART IF the causes the partly bit to be set to 1 and 0). 4. The date of the DX port of the LUART IF the causes the partly bit to be set to 1 and 0). 4. Find causes the partly and the DX port of the LUART IF the causes the partly bit to be set to 1 and 0). 4. Find cause the DX port of the LUART IF the causes the partly bit to be set to 1 and 0). 4. Find cause the DX port of the LUART IF the and the DX port of the LUART IF the received of the DX port of the LUART IF the received of the DX port of the LUART IF the received of the DX port of the DX por	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The Internet and Party, Error, States of the FSR are not working and remain all their odd and values. The Internet and Party, Error, States are always 0 or an extension of the Internet and Party, Error, States are always 0. The Internet Internet on Commonly, but the rx persy, states of the FSR is functioning incomestly. The rx persy, states of the FSR is functioning incomestly, the rx persy, states of the FSR is functioning incomestly. The rx persy, states of the FSR is functioning incomestly, the rx persy, states of the FSR is functioning incomestly. The rx persy, states of the FSR is functioning incomestly. The rx persy, states of the FSR is functioning incomestly. The rx persy and 0 when the FFO contains data.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an of used Reserved region register from address ORCOD-DICOPE Process condition. PRESS grad of use in 1. 1.Configure the register for the IXX part of the LUART IP to receive data. 2.Configure the register for the IXX part of the LUART IP to receive data. 2.Configure the register for from the IXX part of the LUART IP to receive data. 3.2 Early controls on the IXX part of the LUART IP to receive data. 3.2 Early controls on the IXX part of the LUART IP to receive data. 3.2 Early controls on the IXX part of the LUART IP to receive data. 3.3 Early controls on the IXX part of the LUART IP to receive data. 4.3 Early controls on the IXX part of the LUART IP to receive data. 4.3 Early controls on the IXX part of the LUART IP to receive data. 4.3 Early controls on the IXX part of the LUART IP (data causes the parts) bit to be set to 1 and 0). 4.3 Early controls on the IXX part of the LUART IP (data causes the parts) bit to be set to 1 and 0). 4.4 EMECH for the interpret parts grad parts green; subside the IXXIV IP received and 0. 4.5 Early controls on the IXX part of the LUART IP (data causes the parts) bit to be set to 1 and 0). 4.6 EMECH parts, green; data. 4.6 EMECH parts, green; data. 5.6 EMECH parts, green; data. 5.6 EMECH parts, green; data. 6.7 EMECH parts, green; green; green; data. 6.7 EMECH parts, green; g	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The interrupt and Party_Error_States of the FSRI are not working and remain all their obtaint values. The interrupt and Party_Error_States are always 0. The interrupt functions consensity, but the no energy_states of the FSRI is functioning incommonly. The no energy_states by these for function invented it is 1 when the FPC0 is empty and 0 when the FPC0 contains data. The interrupt and the FRI, FIAL States of the FSRI function connectly, but the experiments of the FRI is the interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI. Energy_States has changed over thought the bit was not created.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an of used Reserved region register from address ORCOD-DICOPE Process condition. PRESS grad of use in 1. 1.Configure the register for the IXX part of the LUART IP to receive data. 2.Configure the register for the IXX part of the LUART IP to receive data. 2.Configure the register for from the IXX part of the LUART IP to receive data. 3.2 Early controls on the IXX part of the LUART IP to receive data. 3.2 Early controls on the IXX part of the LUART IP to receive data. 3.2 Early controls on the IXX part of the LUART IP to receive data. 3.3 Early controls on the IXX part of the LUART IP to receive data. 4.3 Early controls on the IXX part of the LUART IP to receive data. 4.3 Early controls on the IXX part of the LUART IP to receive data. 4.3 Early controls on the IXX part of the LUART IP (data causes the parts) bit to be set to 1 and 0). 4.3 Early controls on the IXX part of the LUART IP (data causes the parts) bit to be set to 1 and 0). 4.4 EMECH for the interpret parts grad parts green; subside the IXXIV IP received and 0. 4.5 Early controls on the IXX part of the LUART IP (data causes the parts) bit to be set to 1 and 0). 4.6 EMECH parts, green; data. 4.6 EMECH parts, green; data. 5.6 EMECH parts, green; data. 5.6 EMECH parts, green; data. 6.7 EMECH parts, green; green; green; data. 6.7 EMECH parts, green; g	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The interrupt and Party_Error_States of the FSRI are not working and remain all their obtaint values. The interrupt and Party_Error_States are always 0. The interrupt functions consensity, but the no energy_states of the FSRI is functioning incommonly. The no energy_states by these for function invented it is 1 when the FPC0 is empty and 0 when the FPC0 contains data. The interrupt and the FRI, FIAL States of the FSRI function connectly, but the experiments of the FRI is the interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI. Energy_States has changed over thought the bit was not created.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an of under Beasened region register from address ORCORD-DICKET Process condition. PICES grad of up to 1. 1.Cortigate the register for the EX port of the LUART IF to receive data. 2.Cortigate the register for the EX port of the LUART IF to receive data. 2.Cortigate the EX register for Exchange partly error. Handbase interior, 3.2. Best of various makes to the EX port of the LUART IF to receive data. 2.3. Best of various makes to the EX port of the LUART IF the cases the partly but to be set to 1 and 0; 3.2. Best of various makes to the EX port of the LUART IF the cases the partly but to be set to 1 and 0; 4.Percy server. 4. Read data from the EXT register to Exclude the LUART IF the cases the partly but to be set to 1 and 0; 4. Read data from the EXT register to Exclude the LUART IF the cases the partly but to be set to 1 and 0; 4. Sec of control makes to the EX port of the LUART IF the cases the partly but to be set to 1 and 0; 4. Sec of control makes to the EX port of the LUART IF the cases the partly but to be set to 1 and 0; 4. Sec of control makes to the EX port of the LUART IF the cases the partly but to be set to 1 and 0; 4. Sec of control makes to the EX port of the LUART IF the cases the partly but to be set to 1 and 0; 4. Sec of control makes to the EX port of the LUART IF the section the partly stope to the LUART IF the received the partly stope to the LUART IF the received stope th	uartip jirternejit, enable, oddpusty, test uartip jirternejit, enable, jirdilolul, test uartip jirternejit, enable, jirdilolul, test	Direct, Checker Direct, Checker	FAIL	The interrupt and Party_Error_States of the FSRI are not working and remain all their obtaint values. The interrupt and Party_Error_States are always 0. The interrupt functions consensity, but the no energy_states of the FSRI is functioning incommonly. The no energy_states by these for function invented it is 1 when the FPC0 is empty and 0 when the FPC0 contains data. The interrupt and the FRI, FIAL States of the FSRI function connectly, but the experiments of the FRI is the interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI. Energy_States has changed over thought the bit was not created.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an on from Selection of the Country of the LART IP to receive data. 1.Configure the register for the EX port of the LART IP to receive data. 2.Configure the register for the EX port of the LART IP to receive data. 2.Configure the register for the EX port of the LART IP to receive data. 2.Configure the ER register for Ending partly more Handware internet. 3.2. Sent crustom data to the EX port of the LART IP to receive data. 2.3. Sent crustom data to the EX port of the LART IP (data causes the party) bit to be set to 1 and 0). 3.2. Sent crustom data to the EX port of the LART IP (data causes the party) bit to be set to 1 and 0). 4.Party sent LART IP and LART IP with offering party late of their interpretation. 4.2. Sent crustom data to the EX port of the LART IP (data causes the party) bit to be set to 1 and 0). 4.3. Sent crustom data to the EX port of the LART IP (data causes the party) bit to be set to 1 and 0). 4.3. Sent crustom data to the EX port of the LART IP (data causes the party) bit to be set to 1 and 0). 4.4. Selection data to the EX port of the LART IP (data causes the party) bit to be set to 1 and 0). 4.6. CREAT party, error, data. 4.6. CREAT party, error, data. 4.6. CREAT party, error, data. 5.6. Registed on one one for the Register for clear data in the EX PETO. 5. Registed on one one for the Register for clear data in the EX PETO. 5. Registed one one one of our data in the EX PETO. 6. CREAT party, error, data. 6. CREAT party, error, data is a 1 when Party error. 6. Larter, error,	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The interrupt and Party_Error_States of the FSRI are not working and remain all their obtaint values. The interrupt and Party_Error_States are always 0. The interrupt functions consensity, but the no energy_states of the FSRI is functioning incommonly. The no energy_states by these for function invented it is 1 when the FPC0 is empty and 0 when the FPC0 contains data. The interrupt and the FRI, FIAL States of the FSRI function connectly, but the experiments of the FRI is the interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI. Energy_States has changed over thought the bit was not created.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an of under Beasened region register from address ORDOD-DICKET Process condition. PICES grad of ups in 1. 1.Cortigate the register for the DX port of the LUART IF to receive data. 2.Cortigate the register for the DX port of the LUART IF to receive data. 2.Cortigate the ER register for Ending partly more Fastdown internet. 3.2. Sort or universal control of the LUART IF to receive data. 2.3. Sort or universal control or the LUART IF the sections the partly but to be set to 1 and 0; 3.2. Sort or universal control or the LUART IF the sections the partly but to be set to 1 and 0; 4. Red data from the ERR register to Ending from LUART IF process data 3.2. Sort or universal control or the LUART IF the sections the partly but to be set to 1 and 0; 4. Red data from the ERR register to End or the LUART IF place causes the partly but to be set to 1 and 0; 4. Sort or control or the LUART IF the Sort or the LUART IF the sections the partly but to be set to 1 and 0; 4. Sort or control or the Sort or the LUART IF the sections the partly but to be set to 1 and 0; 4. Sort or control or the Sort or the LUART IF the sections the partly but to be set to 1 and 0; 4. Sort or control or the Sort or the Sort or the LUART IF the sections the partly but to be set to 1 and 0; 4. Sort or control or the Sort or	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSRI are not working and remain all their obtaint value. The Internet and Party, Error, Status are always 0. The Internet Societies consocily, but the in, anyth, plates of the FSRI is territoring incorrectly. The internet consocily, but the in, anyth, plates of the FSRI is trained the FPFO is empty, and 0 when the FPFO contains data. The Internet Societies consocily, but the internet invented it is it when the FPFO is empty, and 0 when the FPFO contains data.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Old purity error PIFO amply FIFO MI	2. With an of under Beasened region register from address ORDOD-DOCFF Process condition. PERPS grid or gas in 1. 1. Configure the register for the RX port of the LUART IP to receive data. 2. Configure the register for the RX port of the LUART IP to receive data. 2. Configure the register for the RX port of the LUART IP to receive data. 3. Exercit variation data to the RX port of the LUART IP to receive data. 3. Exercit variation data to the RX port of the LUART IP to receive data. 3. Exercit variation data to the RX port of the LUART IP to receive the pulsey that be set to 1 and 0). 3. Exercit variation data to the RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. For exercit variation of the RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. Configure the RX port of RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. Configure the RX port of RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. Configure the RX port of RX port of the LUART IP of the pulsey that the LUART IP occupies floorpoint. 4. Configure the RX port of RX port of the LUART IP occupies floorpoint. 4. Configure the RX port of RX port of the LUART IP to receive the floorpoint. 4. Fine dates from the RX port of the LUART IP to receive the floorpoint. 4. Fine dates from the RX port of the LUART IP to receive date. 5. Configure the RX port of the RX port of the LUART IP to receive date. 5. Configure the RX process to exclusive the RX port of the LUART IP to receive date. 6. Configure the RX process to exclusive the RX port of the LUART IP to receive date. 6. Configure the RX process to exclusive the RX port of the LUART IP to receive date. 7. CHICATO the between the rate of the RX port of the LUART IP to receive date. 8. Configure the register to exclusive the RX PX PVO comply between interno. 9. CHICATO the between the RX port of the LUART IP to receive date. 9. Configure the RX process to exclusive the RX PX PVO contain da	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Interrupt and Tip Fifty States of the FSR are not working and remain all their odd and vastes. The Interrupt and Party _Error_State are always 0 The Interrupt Annother connectly, but the rx_empty_states of the FSR is in functioning empty and 0 when the FFFO contains data. The Interrupt and the RX_FM_States of the FSR tended connectly, but the FFFO is empty, graded and the RX_Empty_States has changed even though this bit was not employed. The Interrupt and Tip_FM_States of the FSR are not excellent, and the EMPC is empty. The Interrupt and Tip_FM_States of the FSR are not excellent, and employed even though this bit was not employed. The Interrupt and Tip_FM_States of the FSR are not excellent, and employed even default values. The Interrupt and Tip_FM_States of the FSR are not excellent, and employed even default values.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Closs partity error FIFO empty	2. With an of under Beasened region register from address ORDOD-DOCFF Process condition. PERPS grid or gas in 1. 1. Configure the register for the RX port of the LUART IP to receive data. 2. Configure the register for the RX port of the LUART IP to receive data. 2. Configure the register for the RX port of the LUART IP to receive data. 3. Exercit variation data to the RX port of the LUART IP to receive data. 3. Exercit variation data to the RX port of the LUART IP to receive data. 3. Exercit variation data to the RX port of the LUART IP to receive the pulsey that be set to 1 and 0). 3. Exercit variation data to the RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. For exercit variation of the RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. Configure the RX port of RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. Configure the RX port of RX port of the LUART IP of the causes the pulsey that be set to 1 and 0). 4. Configure the RX port of RX port of the LUART IP of the pulsey that the LUART IP occupies floorpoint. 4. Configure the RX port of RX port of the LUART IP occupies floorpoint. 4. Configure the RX port of RX port of the LUART IP to receive the floorpoint. 4. Fine dates from the RX port of the LUART IP to receive the floorpoint. 4. Fine dates from the RX port of the LUART IP to receive date. 5. Configure the RX port of the RX port of the LUART IP to receive date. 5. Configure the RX process to exclusive the RX port of the LUART IP to receive date. 6. Configure the RX process to exclusive the RX port of the LUART IP to receive date. 6. Configure the RX process to exclusive the RX port of the LUART IP to receive date. 7. CHICATO the between the rate of the RX port of the LUART IP to receive date. 8. Configure the register to exclusive the RX PX PVO comply between interno. 9. CHICATO the between the RX port of the LUART IP to receive date. 9. Configure the RX process to exclusive the RX PX PVO contain da	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The interrupt and Party_Error_States of the FSRI are not working and remain all their obtaint values. The interrupt and Party_Error_States are always 0. The interrupt functions consensity, but the no energy_states of the FSRI is functioning incommonly. The no energy_states by these for function invented it is 1 when the FPC0 is empty and 0 when the FPC0 contains data. The interrupt and the FRI, FIAL States of the FSRI function connectly, but the experiments of the FRI is the interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI interrupt and the FRI. FIAL States of the FSRI function connectly, but the experiments of the FRI. Energy_States has changed over thought the bit was not created.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Old purity error PIFO amply FIFO MI	2. Within and noted Researced region register from address ORCOS-DICKET Researced Control (PECE) paged on gas to 1 1. Configure the register for the RX port of the LUART IF to receive data. 2. Configure the register for the RX port of the LUART IF to receive data. 2. Configure the register for the RX port of the LUART IF to receive data. 3. Secrit various makes the RX port of the LUART IF to receive data. 3.2. Secrit various makes to the RX port of the LUART IF to receive data and the secret data. 3.2. Secrit various makes to the RX port of the LUART IF the class causes the pulmp bit to be set to 1 and 0). 3.3. Read data from the RSR register to be date from IRX PX PX process of the RX port of the LUART IF receives the pulmp bit to be set to 1 and 0). 4.1. Configure the RX port of the LUART IF the class causes the pulmp bit to be set to 1 and 0). 4.3. CREACT the returned and pulmp years, such and the LUART IF receives the Received At 1 and 0). 4.4. CREACT the returned and pulmp years, such and the LUART IF receives the Received At 1 and 0). 4.4. CREACT the returned and pulmp years, such as the LUART IF received the Received At 1 and 0). 4.4. CREACT the returned and pulmp years, such as the LUART IF received the Received At 1 and 0). 4.4. CREACT the returned and pulmp years, such as the LUART IF received the Received At 1 and 0). 4.4. CREACT the returned and pulmp years, such as the LUART IF received the Received At 1 and 0). 4.5. The storage single is 1 and pulmp years, such as the LUART IF the received the RATE IN the RATE IN THE RECEIVED AT 1 and 1 a	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSR are not working and remain all their ordinal volume. The Internet and Party, Error, Status are always 0. The Internet Status or connectly, but the in, empty, plates of the FSR is further the FFFO in empty and 0 when the FFFO contains disks. The Internet and the RX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1. The Internet and TX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1.
6.1	Internet and EPO status test. Enable Partly bit drover Enable RX FIFO test.	Old purity error PIFO amply FIFO MI	2. With an of used Reserved region register from address ORCOD-DICOFF Press condition. PRESS yeard of the LIART IF to receive data. 2. Configure the register for the EX port of the LIART IF to receive data. 2. Configure the register for the EX port of the LIART IF to receive data. 2. Configure the Register for Excellent plant plant press of the LIART IF to receive data. 3. Event continued that to the EX port of the LIART IF the data causes the party bit to be set to 1 and 0). 3. Event continued that to the EX port of the LIART IF (data causes the party bit to be set to 1 and 0). 3. Event continued that to the EX port of the LIART IF the data causes the party bit to be set to 1 and 0). 4. First data causes the limit of the LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the limit of LIART IF the causes the party bit to be set to 1 and 0). 4. First data causes the limit of LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the limit of LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the limit of LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the LIART IF and LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the LIART IF (data causes the party bit to be set to 1 and 0). 4. First data causes the liart IF (data causes the party bit to be set to 1 and 0). 4. First data causes the liart IF (data causes the party bit to be set to 1 and 0). 4. First data causes the liart IF (data causes the party bit to be set to 1 and 0). 4. First data causes the liart IF (data causes the party bit to be set to 1 and 0). 4. First data causes the liart IF (data causes the liart IF (data causes the liart IF (data causes). 4. First data causes the liart IF (data causes the liart IF (data causes). 5. First data causes the	uartip_interrupt_enable_coldquartiy_best uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSR are not sorbing and remain all their ordinal volume. The Internet and Party, Error, Status are always 0. The Internet Standard connectly, but the in, anyty, plates of the FSR is further the FFFO is empty, and to when the FFFO contains data. The Internet and the RX, FM, Status of the FSR function connectly, but the experiment of the FSR is an end on the FSR in the Internet and the EX_Errory_Status has charged one frought to the aim are consider. The Internet and TX, FM, Status of the FSR are not sorbing and remain at their default values. The Internet is always 1, and TX, FM, Status as always 1. The Internet and TX, FM, Status of the FSR are not sorbing and remain at their default values. The Internet is always 1, and TX, FM, Status as always 1.
6.1	Internet and EPO status text. Enable Partly bit drord Enable RX FIFO text.	Old purity error PIFO amply FIFO MI	2. With an on force Reserved region register from address ORCOD-DICOFF Prices condition. PRICES price of upon 1.1 1.Corfigure the register for the EX port of the LIART IF to receive data. 2.Corfigure the register for the EX port of the LIART IF to receive data. 2.Corfigure the register for from EX port of the LIART IF to receive data. 3.2 Sent crustom data to the EX port of the LIART IF the receive data. 3.2 Sent crustom data to the EX port of the LIART IF prices causes the party bit to be set to 1 and 0). 3.3 Sent crustom data to the EX port of the LIART IF the causes the party bit to be set to 1 and 0). 4.Party sent of LIART IP and LIART IV the different purely be strong be included as party to the set to 1 and 0. 4.Party sent LIART IP and LIART IV the different purely be strong be included as a party bit to be set to 1 and 0. 4.3 Sent data come for PER register to Cause the law IP party sent of LIART IP and LIART IV the different purely be strong be included as a party bit to 1 and 0. 4.3 Sent data come for PER register to Cause the party sent of LIART IP and LIART IV the Cause the party bit to 1 and 0. 4.6 CEACT purily, every data. 4.6 CEACT purily, every data. 5.6 Registed on once more than did not the cause the party sent of LIART IP and LIART IV the Cause the party sent of LIART IP and LIART IV the Cause the party sent of LIART IP and LIART IV the Cause the Cause the LIART IP and LIART IV the Cause the Cause the LIART IP and LIART IV the Cause the Cause the LIART IV the Cause the C	uatip_interrupt_enable_oxtopunty_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test uatip_interrupt_enable_oxtofold_test	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSR are not working and remain all their ordinal volume. The Internet and Party, Error, Status are always 0. The Internet Status or connectly, but the in, empty, plates of the FSR is further the FFFO in empty and 0 when the FFFO contains disks. The Internet and the RX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1. The Internet and TX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1.
6.1	Internet and EPO status text. Enable Partly bit drord Enable RX FIFO text.	Old purity error PIFO amply FIFO MI	2. With an office of the Description of the LIART IP to receive data. 1.Configure the register for the RX port of the LIART IP to receive data. 2.Configure the register for the RX port of the LIART IP to receive data. 2.Configure the register for the RX port of the LIART IP to receive data. 3.2. Event variation data to the RX port of the LIART IP to receive data. 3.3. Event variation and the the RX port of the LIART IP to receive data. 3.3. Event variation and the the RX port of the LIART IP to receive data. 3.4. Event variation and the the RX port of the LIART IP to receive the period by the best to 1 and 0). 3.5. Event variation and the the RX port of the LIART IP to receive the period by the best to 1 and 0). 4.1. Event variation and the RX port of the LIART IP to receive the period by the the set to 1 and 0). 4.1. Event variation and the RX port of the LIART IP to receive the period by the received and the RX port of the LIART IP to receive the RX port of the LIART IP to receive the RX port of 0. 4.1. Event variation and the RX port of the LIART IP to receive the RX port of 0. 4.1. Event variation and the RX port of the LIART IP to receive the Rx port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 5. Event variation and the RX port of 0. 5. Event variation and the RX port of 0. 5. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of	uartip_interrupt_enable_coldquartiy_best uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSR are not working and remain all their ordinal volume. The Internet and Party, Error, Status are always 0. The Internet Status or connectly, but the in, empty, plates of the FSR is further the FFFO in empty and 0 when the FFFO contains disks. The Internet and the RX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1. The Internet and TX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1.
6.1	Internet and EPO status text. Enable Partly bit drord Enable RX FIFO text.	Old purity error PIFO amply FIFO MI	2. With an office of the Description of the LIART IP to receive data. 1.Configure the register for the RX port of the LIART IP to receive data. 2.Configure the register for the RX port of the LIART IP to receive data. 2.Configure the register for the RX port of the LIART IP to receive data. 3.2. Event variation data to the RX port of the LIART IP to receive data. 3.3. Event variation and the the RX port of the LIART IP to receive data. 3.3. Event variation and the the RX port of the LIART IP to receive data. 3.4. Event variation and the the RX port of the LIART IP to receive the period by the best to 1 and 0). 3.5. Event variation and the the RX port of the LIART IP to receive the period by the best to 1 and 0). 4.1. Event variation and the RX port of the LIART IP to receive the period by the the set to 1 and 0). 4.1. Event variation and the RX port of the LIART IP to receive the period by the received and the RX port of the LIART IP to receive the RX port of the LIART IP to receive the RX port of 0. 4.1. Event variation and the RX port of the LIART IP to receive the RX port of 0. 4.1. Event variation and the RX port of the LIART IP to receive the Rx port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 4.1. Event variation and the RX port of 0. 5. Event variation and the RX port of 0. 5. Event variation and the RX port of 0. 5. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of 0. 6. Event variation and the RX port of	uartip_interrupt_enable_coldquartiy_best uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSR are not working and remain all their ordinal volume. The Internet and Party, Error, Status are always 0. The Internet Status or connectly, but the in, empty, plates of the FSR is further the FFFO in empty and 0 when the FFFO contains disks. The Internet and the RX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1. The Internet and TX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1.
6.1	Internet and EPO status text. Enable Partly bit drord Enable RX FIFO text.	Old purity error PIFO amply FIFO MI	2. With an on force Reserved region register from address ORCOD-DICOFF Prices condition. PRICES price of upon 1.1 1.Corfigure the register for the EX port of the LIART IF to receive data. 2.Corfigure the register for the EX port of the LIART IF to receive data. 2.Corfigure the register for from EX port of the LIART IF to receive data. 3.2 Sent crustom data to the EX port of the LIART IF the receive data. 3.2 Sent crustom data to the EX port of the LIART IF prices causes the party bit to be set to 1 and 0). 3.3 Sent crustom data to the EX port of the LIART IF the causes the party bit to be set to 1 and 0). 4.Party sent of LIART IP and LIART IV the different purely be strong be included as party to the set to 1 and 0. 4.Party sent LIART IP and LIART IV the different purely be strong be included as a party bit to be set to 1 and 0. 4.3 Sent data come for PER register to Cause the law IP party sent of LIART IP and LIART IV the different purely be strong be included as a party bit to 1 and 0. 4.3 Sent data come for PER register to Cause the party sent of LIART IP and LIART IV the Cause the party bit to 1 and 0. 4.6 CEACT purily, every data. 4.6 CEACT purily, every data. 5.6 Registed on once more than did not the cause the party sent of LIART IP and LIART IV the Cause the party sent of LIART IP and LIART IV the Cause the party sent of LIART IP and LIART IV the Cause the Cause the LIART IP and LIART IV the Cause the Cause the LIART IP and LIART IV the Cause the Cause the LIART IV the Cause the C	uartip_interrupt_enable_coldquartiy_best uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest uartip_interrupt_enable_colfoolut_trest	Direct, Checker Direct, Checker Direct, Checker	FAIL FAIL FAIL	The Internet and Party, Error, Status of the FSR are not working and remain all their ordinal volume. The Internet and Party, Error, Status are always 0. The Internet Status or connectly, but the in, empty, plates of the FSR is further the FFFO in empty and 0 when the FFFO contains disks. The Internet and the RX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1. The Internet and TX, FM, Status of the FSR are not working and remain at their disflusions. The Internet is always 1, and TX, FM, Status is always 1.