CSC 137 Sample Midterm

Due No due date **Points** 0 **Questions** 16 **Time Limit** None
Allowed Attempts Unlimited

Instructions

Example of what the midterm will look like. Note that the midterm will not have fill-in-the-blank questions. I left these in the sample midterm because it is good practice.

Taking the sample midterm is optional, no credit will be given.

Take the Quiz Again

Attempt History

	Attempt	Time	Score
KEPT	Attempt 2	1,234 minutes	0 out of 0 *
LATEST	Attempt 2	1,234 minutes	0 out of 0 *
	Attempt 1	8,307 minutes	0 out of 0 *

* Some questions not yet graded

Submitted Mar 18 at 10:14am

Question 1 — 0 / 0 pts

A *decoder* decodes a binary input to a unary output.

Correct!

- (•) True
- ( ) False

Question 2

0 / 0 pts

A *multiplexor* chooses one of multiple input as its single output.

Correct!

- (●) True
- ( ) False

Question 3

0 / 0 pts

To program a Verilog code module that performs the boolean function *AB+CD*, a minimum of 5 logic-gate statements are needed.

Correct!

- ( ) True
- (●) False

Question 4

0 / 0 pts

If a multiplexor is given *k* select input signals, it can only select one output from this many input: *2 times k*.

Correct!

- ( ) True
- (●) False

Question 5

0 / 0 pts

When input to a *decoder* is 101_2, then the output would be `00001000`.

- True
- False

Correct!

Question 6

0 / 0 pts

Which below is not in a *Full Adder*:

Correct!

- a overflow bit
- a sum bit
- a carry-in bit
- a carry-out bit
- two bits in input to sum

Question 7

0 / 0 pts

How many components are there in the BC CPU that write to the common bus?

Correct!

- 7
- 5

6

8

9

Question 8

0 / 0 pts

An "Indirect" memory-reference instruction has extra work at the clock cycle *T (number?)*

Correct!

- (selected) 3
- 0
- 1
- 2
- 4

Question 9

0 / 0 pts

The CPU is controlled by this component (two words):

Correct!

control unit

orrect Answers

Control Unit

Question 10

0 / 0 pts

The Control Units function is to generate (two words):

Correct!

control signals

orrect Answers

Control Signals

Question 11

0 / 0 pts

The timing device in the control unit is called (two words):

Correct!

sequence counter

orrect Answers

Sequence Counter

Question 12

0 / 0 pts

The Sequence Counter has how many binary bits?

Correct!

4

orrect Answers

4

Question 13

0 / 0 pts

The Sequence Counter can indicate a total of how many T-steps:

Correct!

16

orrect Answers

16

Question 14

0 / 0 pts

D0 through D7 are decoded results from this CPU register:

Correct!

Instruction Register

orrect Answers

IR

Instruction Register

Unanswered

Question 15

Not yet graded / 0 pts

Given the Bus Diagram (Figure 5-4, p. 130) and the Control functions and Microoperations (Table 5-6, p. 159), derive the control signals needed to each of the CPU instructions. (Similar to exercise questions.)

Your Answer:

selected instA: do-X, do-Y, ...
selected instB: do-X, do-Z, ...
selected instC: do-W, do-Y, ...

From this question: Given the Bus Diagram (Figure 5-4, p. 130) and the Control functions and Microoperations (Table 5-6, p. 159), derive the

control signals needed to each of the CPU instructions. (Similar to exercise questions.)

> selected instA: do-X, do-Y, ...
> selected instB: do-X, do-Z, ...
> selected instC: do-W, do-Y, ...
> ...

> **Derive timing for each of control signal derived from above. (similar to exercise questions)**

You might be given a question like this:

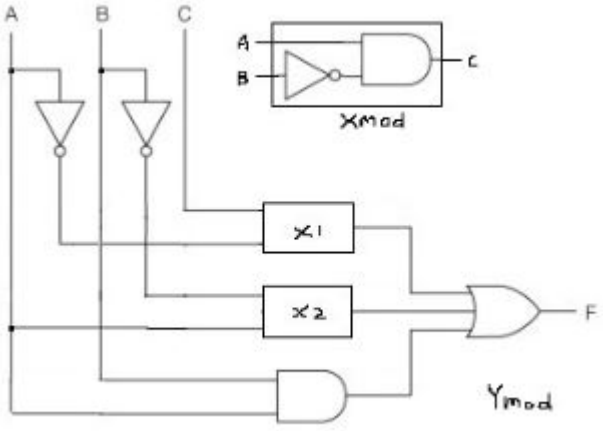
Given code of a Verilog module, draw out the circuit diagram.

Unanswered

Question 16

Not yet graded / 0 pts

Given this gate-logic diagram, write Verilog code for this module. (No Test module needed. Arrays usage may be required.)



Your Answer:

```
module Xmod(A, B, C);
   input A, B;
   output C;
   wire invB;
   not(invB, B);
   and(C, A, invB);
endmodule
module Ymod(A, B, C, F);
   input A, B, C;
   output F;
   wire invA, invB, X1out, X2out, andAB;
   not(invA, A);
   not(invB, B);
   Xmod X1(C, invA, X1out);
   Xmod X2(invB, A, X2out);
   and(andAB, A, B);
   or(F, X1out, X2out, andAB);
endmodule
```