-A decoder decodes 011_2 to 00010000_1	=>A decoder decodes 0112 to 000100001 => false, It depends on decoding technique
-A multiplexer selects two data points as output	=> A multiplexer selects two data points as output => true
-An input event has a higher priority over an ouput event when they are checked	multiplexer (or mux) is a device that combines several analog or digital input signals and forwards them into a single output line
-With an adder-subtracter the first carry-in is set to 0 for adding and 1 for subtracting	=>An input event has a higher priority over an ouput event when they are checked= False
-To subtract 5 from 7, it to add 0111_2 with 11011_2	=>With an adder-subtracter the first carry-in is set to 0 for adding and 1 for subtracting => True
-The highest number of T-Cycles is 16 but it is never used	=>To subtract 5 from 7, it to add 01112 with 110112 => fasle
-The memory addressed by AR directly, not through the bus	=>The highest number of T-Cycles is 16 but it is never used=> true
-A control signal does not need to be defined when it is not involved	=> The memory addressed by AR directly, not through the bus=> true, because Memory takes its address from AR Register
-To write to the memory, the location address is first given through the bus	=>A control signal does not need to be defined when it is not involved=> true
-The BC computer can handle another I/O event while currently servicing one	=>To write to the memory, the location address is first given through the bus=> true
-To encode for the bus control s0 = x1 + x3 +x5 + x7	=> The BC computer can handle another I/O event while currently servicing one=>true
-A multiplexor selects from k Data points would need k^2 select signals	=> To encode for the bus control s0 = x1 + x3 +x5 + x7 =>false
-The input event is checked first before the output event in the BC	=>A multiplexor selects from k Data points would need k^2 select signals=> true => The input event is checked first before the output event in the BC=> true

-In a 5-bit adder/subtractor : the first carry-in is set 0 to do subtraction	=>In a 5-bit adder/subtractor : the first carry-in is set 0 to do subtraction=> true
-To transfer from DR register to AC register, it goes through Adder Logic	=> To transfer from DR register to AC register, it goes through Adder Logic=> true
-To fetch a data, the write signal is needed	=> To fetch a data, the write signal is needed=> false
-The Instructions ISZ requires the largest number of T Cycles.	=>The Instructions ISZ requires the largest number of T Cycles. False
-A decoder decodes a binary input to a unary output.	=>To transfer from DR register to AC register, it goes through Adder Logic a unary output. False
-A multiplexor chooses one of multiple input as its single output.	=> A multiplexor chooses one of multiple input as its single output. => true
-To program a Verilog code module that performs the boolean function AB+CD, a minimum of 5 logic-gate statements are needed.	A multiplexer of 2^n inputs has n selected lines, are used to select which one input line to send to the output =>To program a Verilog code module that performs the boolean function AB+CD, a minimum of 5 logic-gate statements are needed.
-If a multiplexor is given k select input signals, it can only select one output from this many input: 2 times k.	=>If a multiplexor is given k select input signals, it can only select one output from this many input: 2 times k.=> false
-When input to a decoder is 1012, then the output would be 00001000.	A multiplexer of 2^n inputs has n selected lines => When input to a decoder is 1012, then the output would be 00001000.=> false