CSC137 Midterm

Started: Mar 18 at 3:34pm

Quiz Instructions

Hello Students,

This is an open book and notes mid-term. Find a quiet spot and take the exam individually.

Thank you,

Chris

Question 1 — 1 pts

To encode for the bus control: $s0 = x1 + x3 + x5 + x7$

- ◯ True
- ◯ False

Question 2 — 1 pts

The memory is addressed by the AR register through the bus.

- ◯ True
- ◯ False

Question 3 — 1 pts

The instruction ISZ requires the largest number of T cycles.

- ◯ True

- ◯ False

Question 4 — 1 pts

A multiplexor that selects from k inputs would need k^2 select signals.

- ◯ True
- ◯ False

Question 5 — 1 pts

To subtract 3 from 7, we add binary 00111_2 with 11101_2.

- ◯ True
- ◯ False

Question 6 — 1 pts

The input event is checked first before the output event in the basic computer.

- ◯ True
- ◯ False

Question 7 — 1 pts

In a 5-bit adder: the first carry-in is 0.

- ◯ True
- ◯ False

Question 8 — 1 pts

To transfer from DR register to AC register, it goes through Adder Logic.

- ◯ True
- ◯ False

Question 9 — 1 pts

DeMorgan's Theorem states that x'y'=(x'+y)'

- ◯ True
- ◯ False

Question 10 — 1 pts

The BC can handle another I/O event while currently servicing one.

- ◯ True
- ◯ False

Question 11

1 pts

The 2nd to last instruction in the I/O Program should be:

- ION
- IOF
- INC
- HLT

Question 12

1 pts

AC = 8E0A hex, E = 1. After 'CIL', AC = ?

- 8E09
- E0A8
- 8E0B
- 1351
- 1C15

Question 13

1 pts

Which about the 'interrupt handling' is NOT true:

- it synchronize I/O usage among processes
- it speeds up the CPU clock cycles
- it protects the I/O channels

- ◯ it protects the OS space
- ◯ it enhances performance by not busy polling

Question 14

1 pts

The Memory requires the AR register to be:

- ◯ 8 bits
- ◯ 12 bits
- ◯ 32 bits
- ◯ 10 bits
- ◯ 20 bits

Question 15

1 pts

Instruction 'BSA 300' would pair with the instruction:

- ◯ 2 BUN 300
- ◯ BUN 301
- ◯ BUN 300
- ◯ I BUN 301
- ◯ I BUN 300

Question 16

1 pts

The total number of Carry wires in a 10-bit adder should be:

- ◯ 10
- ◯ 20
- ◯ 11
- ◯ 2

Question 17 1 pts

When executing ISZ, PC gets incremented if this register becomes zero:

- ◯ DR
- ◯ AR
- ◯ AC
- ◯ IR

Question 18 1 pts

The cycle when the PC register is incremented:

- ◯ T0
- ◯ T1
- ◯ T7
- ◯ T2

Question 19 — 1 pts

The order of different sizes of the registers:

- ◯ AC > AR > TR
- ◯ AR > PC > OUTR
- ◯ IR > AC > AR
- ◯ AC > PC > INPR
- ◯ DR > INPR > AC

Question 20 — 1 pts

To perform an "add," one operand is AC, the other is:

- ◯ IR
- ◯ DR
- ◯ AR
- ◯ Memory
- ◯ TR

Question 21 — 1 pts

The total number of *xor* gates used to create a 5-bit full adder is:

- ◯ 10
- ◯ 5

- ◯ 20
- ◯ 15

Question 22

1 pts

To fetch data from the Memory, the 3-bit signals sent to the Bus are (binary):

- ◯ 111
- ◯ 101
- ◯ 110
- ◯ 011
- ◯ 100

Question 23

1 pts

An instruction at memory location 500 is being executed, and then an I/O event occurs and the CPU executes the I/O program. What is in M[0] at this time?

- ◯ 0
- ◯ 501
- ◯ 500
- ◯ 499
- ◯ 1

Question 24

1 pts

Which is checked first to handle any I/O evnts:

- ◯ FGO
- ◯ IEN
- ◯ FGI
- ◯ OUTR
- ◯ INPR

Question 25

1 pts

At M[100], *BSA 800* is fetched and executed, then PC is changed to:

- ◯ 799
- ◯ 801
- ◯ 99
- ◯ 101

Question 26

20 pts

For these CPU instructions: AND BUN BSA CMA.
a. Translate their microoperations into signals. List alphabetically.
b. For each signal, derive a concise boolean equation. List alphabetically.
(12 signals, 18 occurences. Can use 'rB9' for D7I'T3, 'and' for AND, 'com' for COM)

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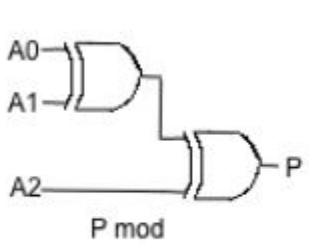
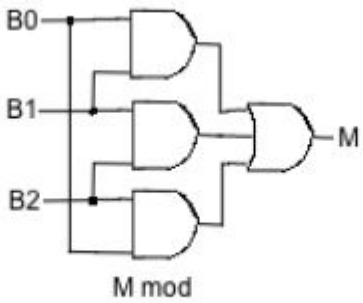
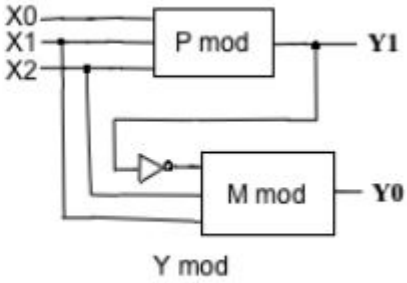
Question 27

20 pts

Program Verilog code for the following modules. Use module compositions and arrays (those with numbers).







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Question 28 10 pts

Find the boolean function for the following k-map

uv \ wx	00	01	11	10
00	1	1	1	0
01	1	1	1	0
11	1	0	0	0
10	1	0	0	0

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