```verilog
wire [31:0] myVec [0:2];
wire [31:0] r1;
wire [31:0] r2;

assign myVec[0] = i1;
assign myVec[1] = i2;
assign myVec[2] = i3;
assign r1 = myVec[addr1];
assign r2 = myVec[addr2];
```