```verilog
always @ (*) begin
   casez(addr)
      addr_1: begin
         b1 = lit_{1,1}
         b2 = lit_{1,2}
            ...
         bn = lit_{1,n}
      end
      addr_2: begin
         b1 = lit_{2,1}
         b2 = lit_{3,2}
            ...
         bn = lit_{3,n}
      end
         ...
end
```