ETRI

# 물품구매계약서

사 본

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계약번호 : EA20052164
계약건명 : LTPE Dielectric AL-CVD 모듈 제작 구매
계약기간 : 2005.09.12~~2006~~2007.11.30
납품장소 : 연구원 지정장소
계약금액 : 549,000,000 원(VAT 포함)

| 계약보증금 | W 54,900,000 | 대금지급계좌내역 | |
|---|---|---|---|
| 지체상금율(1일당) | 1.5/1000 | 지급은행 | |
| 하자보수보증금율 | 5 % | 지 점 명 | |
| 하자보수보증기간 | 2005.12.01~2007.11.30 | 계좌번호 | |
| 대금지급조건 및 결제방법 등 | 카드결제/계좌이체(송금수수료공제)<br>설치검수 완료후지급(1년 무상 A/S) | 예 금 주 | |
| 특 기 사 항 | | | |

위의 계약을 체결함에 있어 갑과 을(연대보증인이 있는 경우 연대)은 입찰유의서, 계약일반조건, 계약특수조건, 현장사양(규격)설명사항, 설계서(시방서)등의 모든 조건이 이 계약의 일부가 됨을 수락하고, 위의 금액으로 계약기한내에 이 계약을 완료할 것을 확약합니다.

2005.09.06

**(갑)**
주 소 : 대전광역시 유성구 가정동 161
상 호 : 한국전자통신연구원
원 장 : 임 주 환 (인)

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주 소 : 경기도 평택시 지제동 33
상 호 : (주)아이피에스
대표자 : 장호승 (인)

**(연대보증인)**
주 소 :
상 호 :
대표자 : (인)

**(연대보증인)**
주 소 :
상 호 :
대표자 : (인)

| 순번 | 물품명세 | 수량 | 단위 | 단가 | 금액 | 비고 |
|---|---|---|---|---|---|---|
| 1 | LTPE Dielectric AL-CVD 모듈 | 1 | Mod | 549,000,000 | 549,000,000 | |

I. General Features : LTPE Dielectric AL-CVD Module

1. LTPE Dielectric AL-CVD Process Module
- Si3N4, SiO2, Si Film Deposition

2. RF Generator & Matching Unit

3. Source & Gas delivery Module

4. Operating Software :
- User interface via NT based computer running the software suite for LTPE Dielectric AL-CVD Module control in Nano AL-CVD Cluster System (자산번호 : 29-04-02041), including test and diagnostic facilities.

5. ETC (Pump, Scrubber, etc.)

6. All system spec. and parts spec. should be equal to standard model one.

II. System Configuration
1. Process Module
1-1. AL-CVD Process Module

- Chamber
Wafer Size : 125mm, 200mm
Wafer Temperature : R.T ~ 650℃
Wafer Temperature Uniformity : < ± 1.5℃ @ 300℃
Wafer Back-side deposition : No
Pump Down Time to base pressure : < 10min @ R.T
Chamber Cleaning Cycle : 5000wafer @ SiN 10nm/wafer
Base Pressure : < 1×10-3 Torr
Leak Rate : < 5×10-3 Torr/min @ 300℃
Process Pressure : 0.1~10 Torr
Valve Switching Time : < 0.1 sec
Built in analysis Port for Process Monitor
Reaction Energy Source : Plasma with thermal energy, Ozone(option)
- Source & Gas Line
Source Line Heating : R.T ~ 200℃
Source Line Temperature Uniformity : ± 2℃ @ 150℃
Gas Curtain to Prevent from Deposition of the Reactor Wall
Separate Reactive Gas Feeding
Source(3) : SiN(Maker recommend), SiO(Maker recommand), Si(Maker recommand)
Gas (7) : Ar, N2, SiH4, H2, NH3, NF3, O3(O2)
Gas Spare. : 1 ea

? Remote plasma cleaning
- Remote plasma chamber cleaning process
Temp. < 500℃, Time < 5min
Particle : < 20ea @ > 0.13um, 8" wafer with 5mm edge exclusion
Pressure : 0.1 ~ 10 Torr
Gas : NF3/Ar
Flow-rate : 1 ~ 10SLPM
Power : 2 ~ 5 KW
Impurity (C, Fe,..) : < 10E10 atoms/cm2 @ 8" wafer surface
Gas Impurity (O2, COX, H2O, ..) : < 10E-13 torr by MS

? Si3N4 Film
- Process condition (After as-depositio

n without curing and other treatment)
Temp. : 200 ~ 500℃
Pressure : 0.1 ~ 10 Torr
Cycle Time : < 10sec
Source : SiN (Maker recommand)
Reation Gas : SiH4, H2, NH3, 03(02)
Purge/Carrier Gas : Ar, N2
Reaction Energy Source : plasma + therm al
- Step coverage
90% @ (aspect ratio > 5, 0.1um line, 10 nm SiN film)
Uniformity
: Within wafer : < 3% (> 5 points), 5mm edge exclusion
: Wafer to wafer : < 2% (> 5 points), 5 mm edge exclusion
- Film Thickness control : < ±5% @ 10n m SiN
- Film Thickness Uniformity : < 2% @ 10 nm SiN, 5mm edge exclusion, >49 points measure
- Film Composition Uniformity : < 3% @ 10nm SiN, 5mm edge exclusion, >49 point s measure
- Added Film Surface Roughness (RMS) : < 1.0Å @ 10nm SiN, 5mm edge exclusion, >49 points measure
- Dielectric constant uniformity
: Within wafer : < 2% (1sigma), 5mm edg e exclusion, >49 points measure
: Wafer to wafer : < 2% (1sigma), 5mm e dge exclusion, >49 points measure
- Particle : < 20ea ( size > 0.13um ) o n 8" wafer, >49 points measure
- Adhesion : No peel off ( to silicon, oxide, gate electrode)
- Film impurity (After as-deposition at 300℃)
: H content : < 2%
: C content : < 2%
: Fe, Cu, Ni content : < 5E10 atoms/cm2

: Cl content : < 1%
- Throughput : > 5 wafers/hour (@ SiN 1 0nm/wafer)

? SiO2 Film
- Process condition (After as-depositio n without curing and other treatment)
Temp. : 200 ~ 500℃
Pressure : 0.1 ~ 10 Torr
Cycle Time : 10sec
Source : SiO(Maker recommend)
Reation Gas : SiH4, NH3, 03(02),
Purge/Carrier Gas : Ar, N2
- Step coverage
> 90% @ (aspect ratio > 5, 0.1um line, 10nm SiO film)
Uniformity
: Within wafer : < 2% (> 49points, 1 si gma), 5mm edge exclusion
: Wafer to wafer : < 2% (>49 points, 1 sigma), 5mm edge exclusion
- Film Thickness control : < ±5% @ 10n m
- Film Thickness Uniformity : < 2% @ 10 nm SiO, 5mm edge exclusion, >49 points measure
- Film Composition Uniformity : < 3% @ 10nm SiO, 5mm edge exclusion, >49 point s measure
- Added Film Surface Roughness (RMS) : <1.0Å @ 10nm SiO, 5mm edge exclusion, >49 points measure
- Dielectric constant uniformity
: Within wafer : < 2% (1sigma), 5mm edg e exclusion, >49 points measure

: Wafer to wafer : < 2% (1sigma), 5mm edge exclusion, >49 points measure
- Particle : < 20ea (size > 0.13um ) on 8" wafer, >49 points measure
- Adhesion : No peel off (to silicon, oxide, nitride, gate electrode)
- Film impurity (After as-deposition at 300℃)
: H content : < 2%
: C content : < 2%
: Fe, Cu, Ni content : < 5E10 atoms/cm2

: Cl content : < 2%
- Throughput : > 5 wafers/hour (@ SiO 10nm/wafer)

? System Reliability
- System reliability
: MTBF ( > 500 hour)
: MTTR ( > 8 hour)
: Up-time ( > 80%)
- Target Film
: SiN, SiO, Si
- Others
: Properly designed for reducing the particle generation and related data should be attached

2-3. Vacuum
- Base Pressure
i. AL-CVD Process module : < 1E-3Torr

- Leak rate
i. AL-CVD Process module : < 0.3mTorr/min

2-4. Gas
- Gas flow
i. MFC over shoot : < ±1% of full scale after 2 sec of flow
ii. Actual flow deviation : < ±1% of full scale
- All gas line with including gas filter (0.01um)
- Gas line purge of all the process gas

2-5. Safety
- Inter-locks to prevent hazardous mixing of gases in hardware and software
- Over temperature should be checked and interlocked
- Gas leak should be monitored by built-in sensor, inter-locked and alarmed.
- Chamber over pressure interlock
- System safety data should be attached

3. Others

3-1. Delivery
- 3.5 months after P.O

3-2. Warrant
- 2 year KAONI_IN_DISABLE labor and parts of hardware after the sign-off of acceptance test
- 2 year KAONI_IN_DISABLE labor and upgrade of software after the sign-off of acceptance test

3-3. Installation
- Within 15 days after system arriving at install site, the final sign-off for acceptance should be done by ETRI responsible person, when installation is completely finished by maker's engineer and all requirements about the equipment performance of ETRI are satisfied.

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|---|---|---|---|---|---|---|
| | - Delayed fee was specified as a 1.5/1000 of total payment for system per day.<br><br>3-4. Training<br>- Two process engineers and two maintenance engineers<br>- Period : Longer than 1weeks<br>- All travel and training expenses should be paid by manufacturer<br>- System should be confirmed by ETRI engineer at manufacture's site<br><br>3-5. Payment<br>- Payment should be available to 100% of the contract amount after acceptance test sign-off.<br><br>3-6. Spare parts<br>- 1 year guaranteed consummables and additional recommended spare parts (list should be attached)<br>- Repair parts (required more than 1 month in delivery, list should be attached)<br><br>3-7. Documents<br>- 2Sets of hard copies (1set for clean room usage)<br>- The manuals of operation and maintenance, drawing of electric circuit and system, full OEM (Original Equipment Manual) set should be included<br>- Software packages for system back-up should be included<br><br>3-8. After Service<br>- Per request, prompt service should be supplied<br><br>3-9. Others<br>- Application engineer should reside at ETRI more than 4 weeks after installation<br>- The acceptance test procedure about each test items should be attached in details | | | | | |