EE-221 DIGITAL LOGIC DESIGN

B.S. ELECTRICAL ENGINEERING
FINAL LAB PROJECT

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ARITHMETIC LOGIC UNIT

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1. DECLARATION:

This report has been prepared based on my work. Where other published and unpublished source materials has been used, these have been acknowledged.

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2. ABSTRACT:

We will design an ALU to implement 12 given functions. This ALU is built using basic electronics components such as logic gates, adders multiplexers etc. This circuit takes two 4-bit binary numbers as input and performs different operations depending upon the combination of select inputs (control) of multiplexers to generate a 4-bit output. Comparator compares two inputs whether both inputs are equal, greater or smaller. The simulation is performed on Proteus, and circuit is implemented on hardware too.

3. OBJECTIVE:

To design and implement a 4-bit Arithmetic Logic Unit (ALU) that can perform various operations as given.

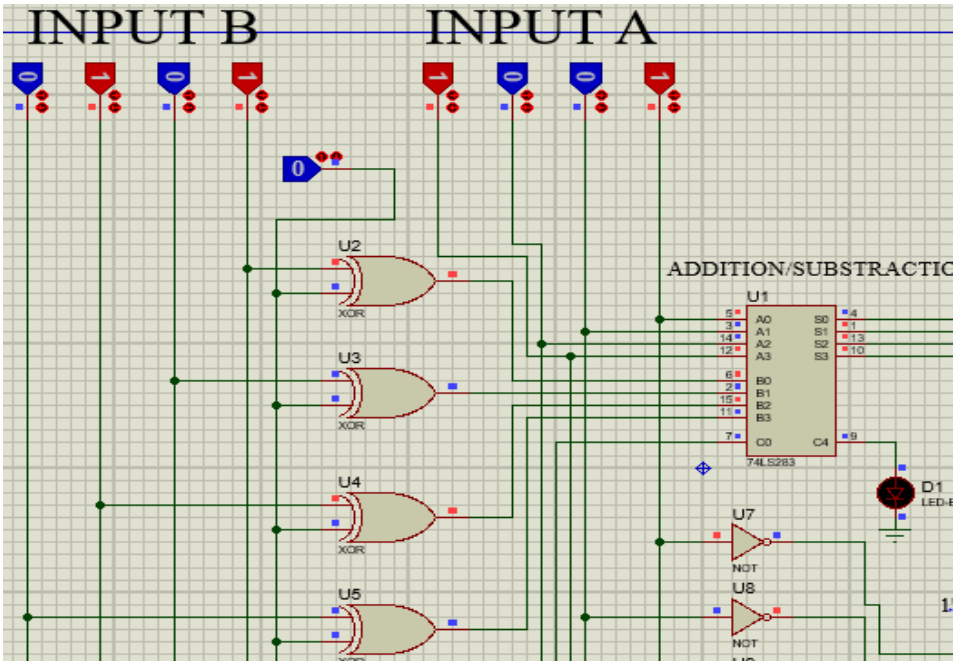
4. INTRODUCTION:

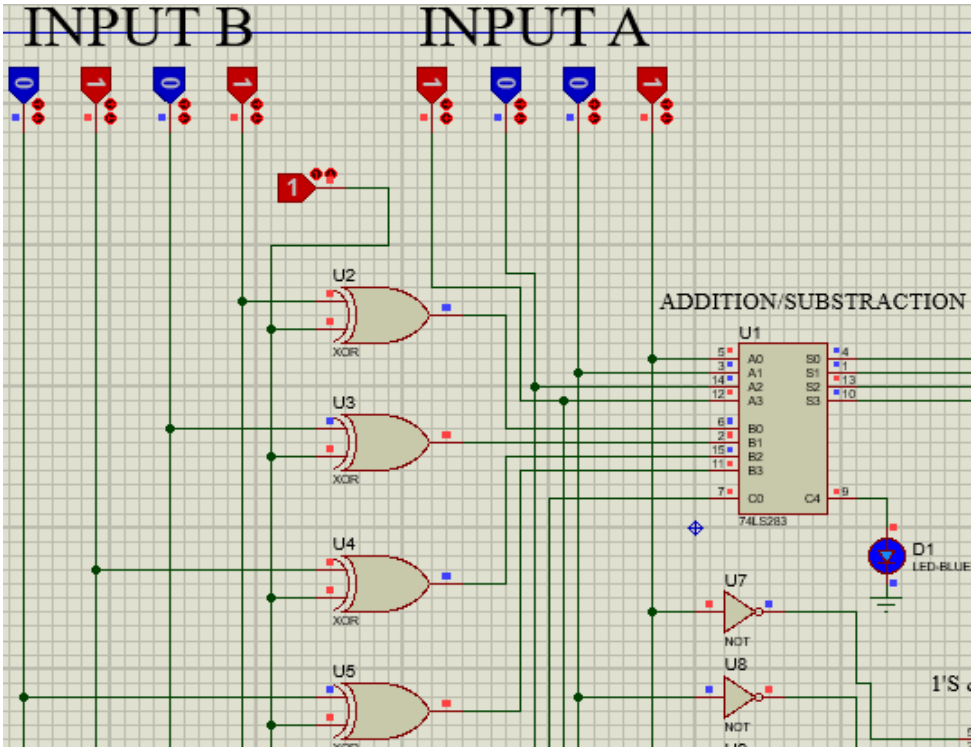
An **Arithmetic Logic Unit** (ALU) is a digital circuit used to perform arithmetic and logic operations. In computing, an arithmetic logic unit is a combinational digital circuit that performs arithmetic and bitwise operations on integer binary numbers.

5. DESIGN PARAMETERS (ARITHMETIC UNIT WORKING)

A. Addition/Subtraction:

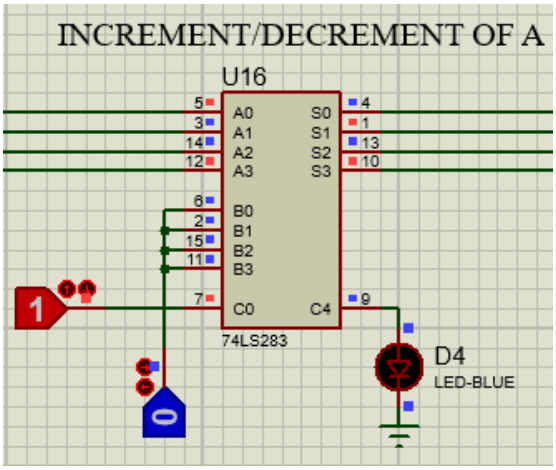
We used one 4-bit adder to add/subtract two 4-bit numbers (A and B). We have also used 4 XOR gate to select operations, whether to perform addition or subtraction. If second input to XOR gates is 0 it will perform addition, if it is 1 subtraction of two inputs will take place. If the carry out comes 1, it is considered as overflow.

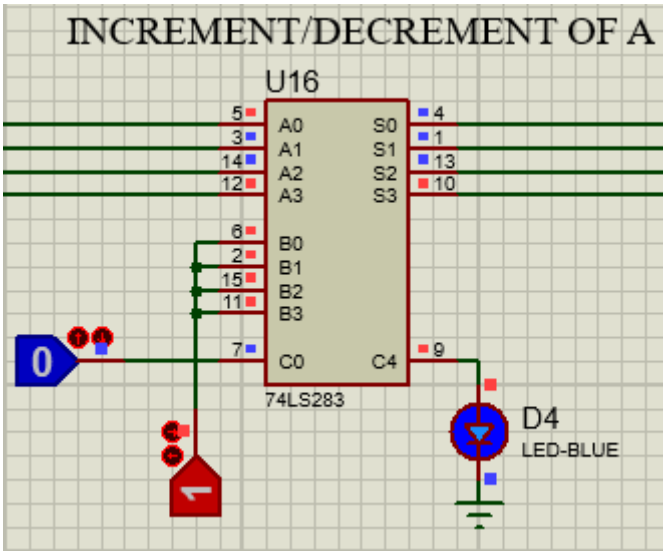




B. Increment/ Decrement:

We used 1 4-bit adder to increment/decrement each 4-bit number (A & B). We have also shorted one of the input and gave a logic state on "Co" to select operations, whether to perform increment or decrement. If logic state is 1 and other input is 0 so it will perform increment, if logic state is 0 and other input is 1, decrement of input will take place. If the carry out comes 1, it is considered as overflow.

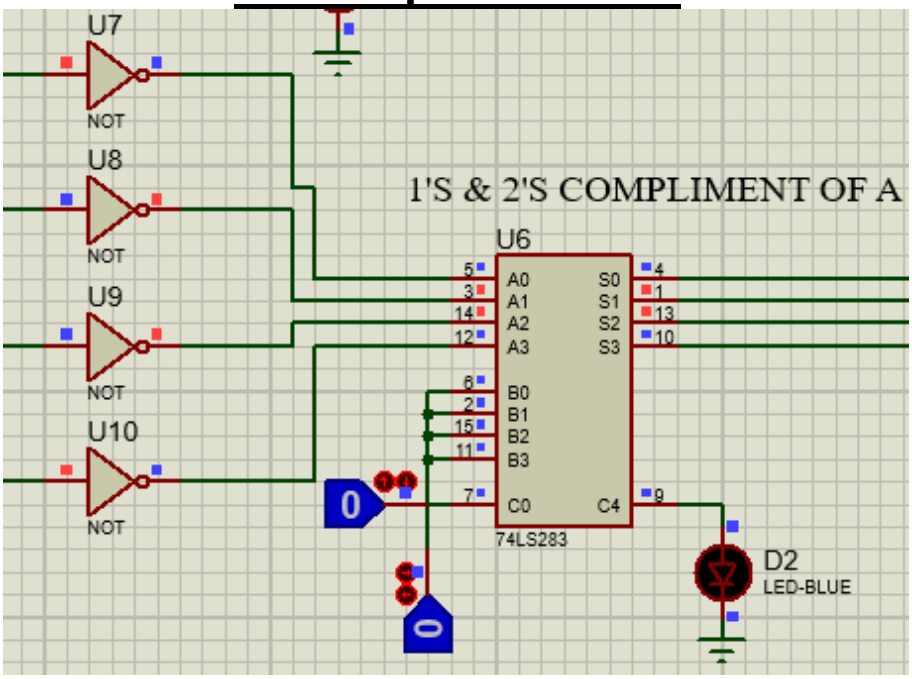




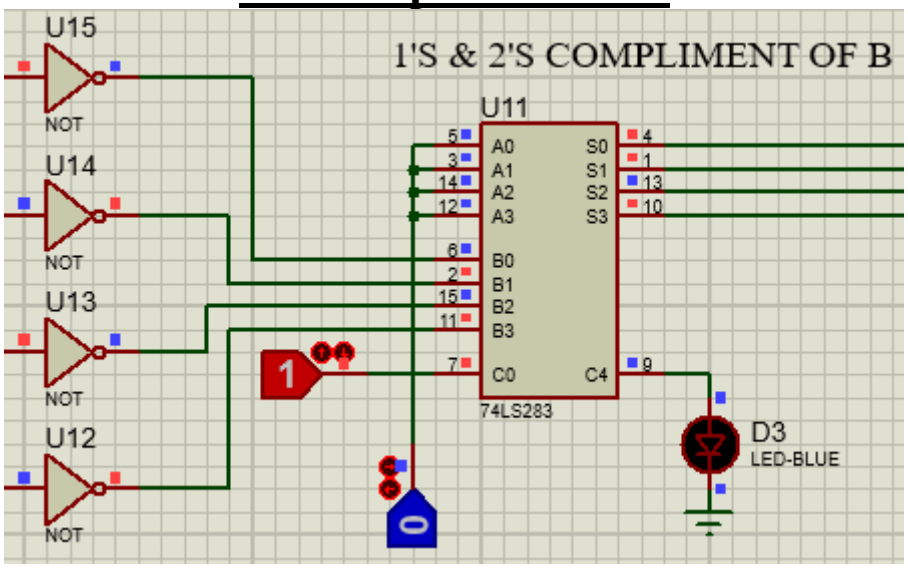
C. 1's/2's Complement:

1's complement is basically bitwise NOT of any number as it inverts all the bits. We have passed the inputs of A through **NOT gate** and B was **Logic Zero**, by changing the logic state of **Co** we got 1's & 2's Complement for A using adder IC 74283. The same procedure implies to input B.

1's Complement Of A

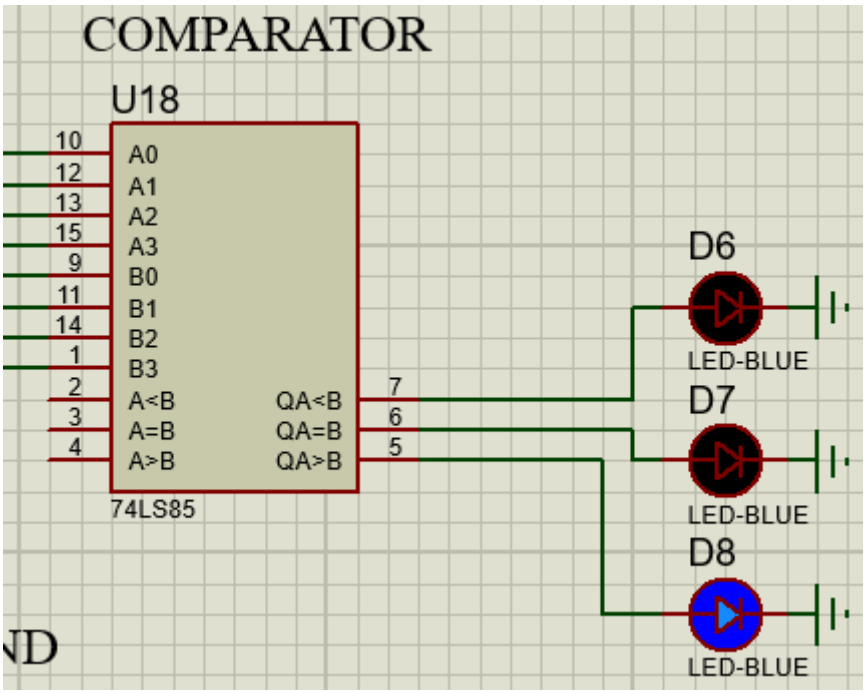


2’s Complement of B



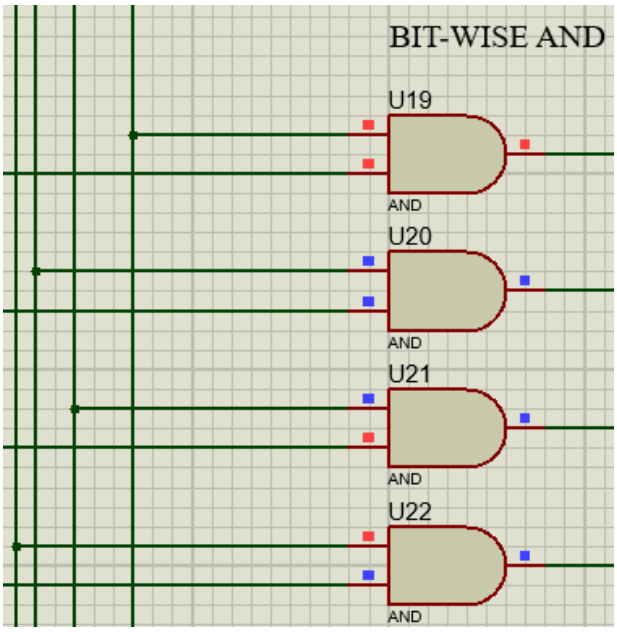
D. Comparator:

We have used comparator IC-7485. When A is greater the B the corresponding LED glows up and vice versa.



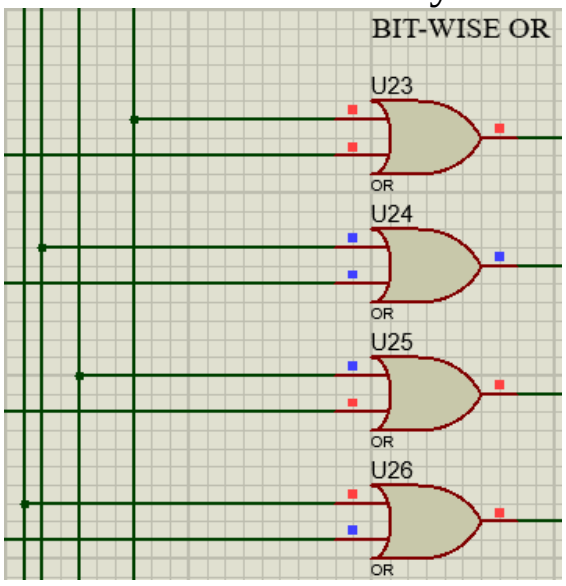
E. Bitwise AND:

This function is used to do bit-wise AND of both 4-bit binary numbers. Four AND gates are used to multiply each bit of the two binary numbers together.



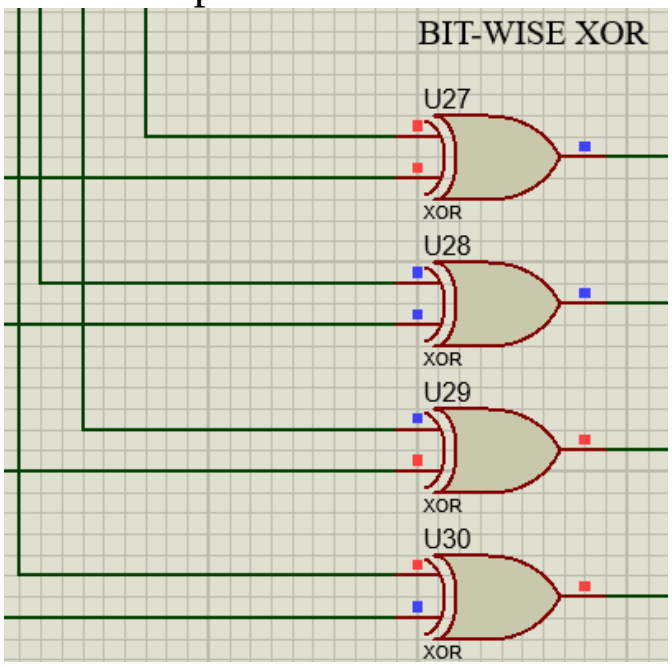
F. Bitwise OR:

This function is used to do bit-wise addition of both 4-bit binary numbers. Four OR gates are used to add each bit of the two binary numbers together.



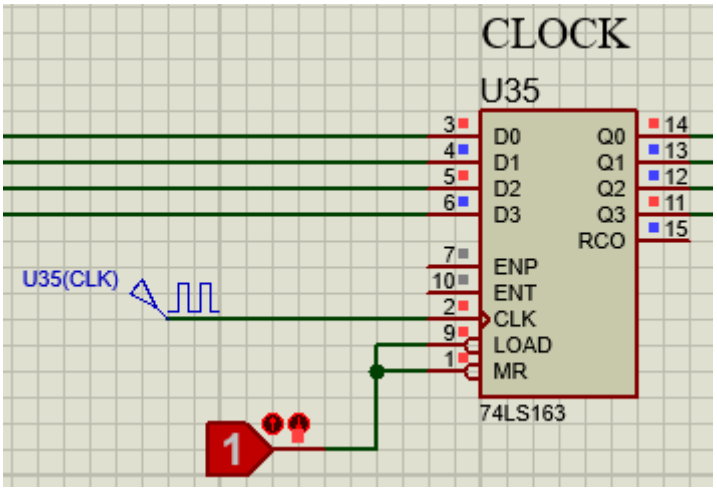
G. Bitwise XOR:

This function is used to do bit-wise XOR of both 4-bit binary numbers. Four XOR gates are used to perform the operation.



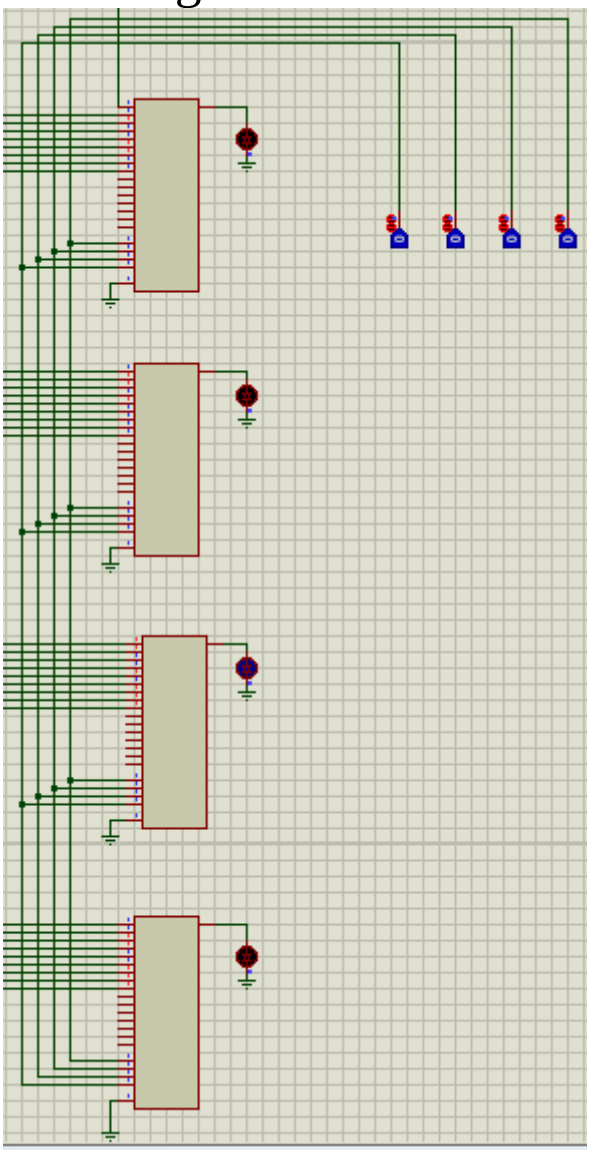
H. Clock:

We can define a clock signal as a particular type of signal that oscillates between a high and low state.



I. MUX:

16X1 Multiplexers have been used in which the select lines are connected on A,B,C,D and the inputs are connected in the same order in each MUX according to M.S.B and L.S.B.



J. LOAD A:

A input was loaded into a 4 bit counter and will load the same input to the output as we will provide it on A.

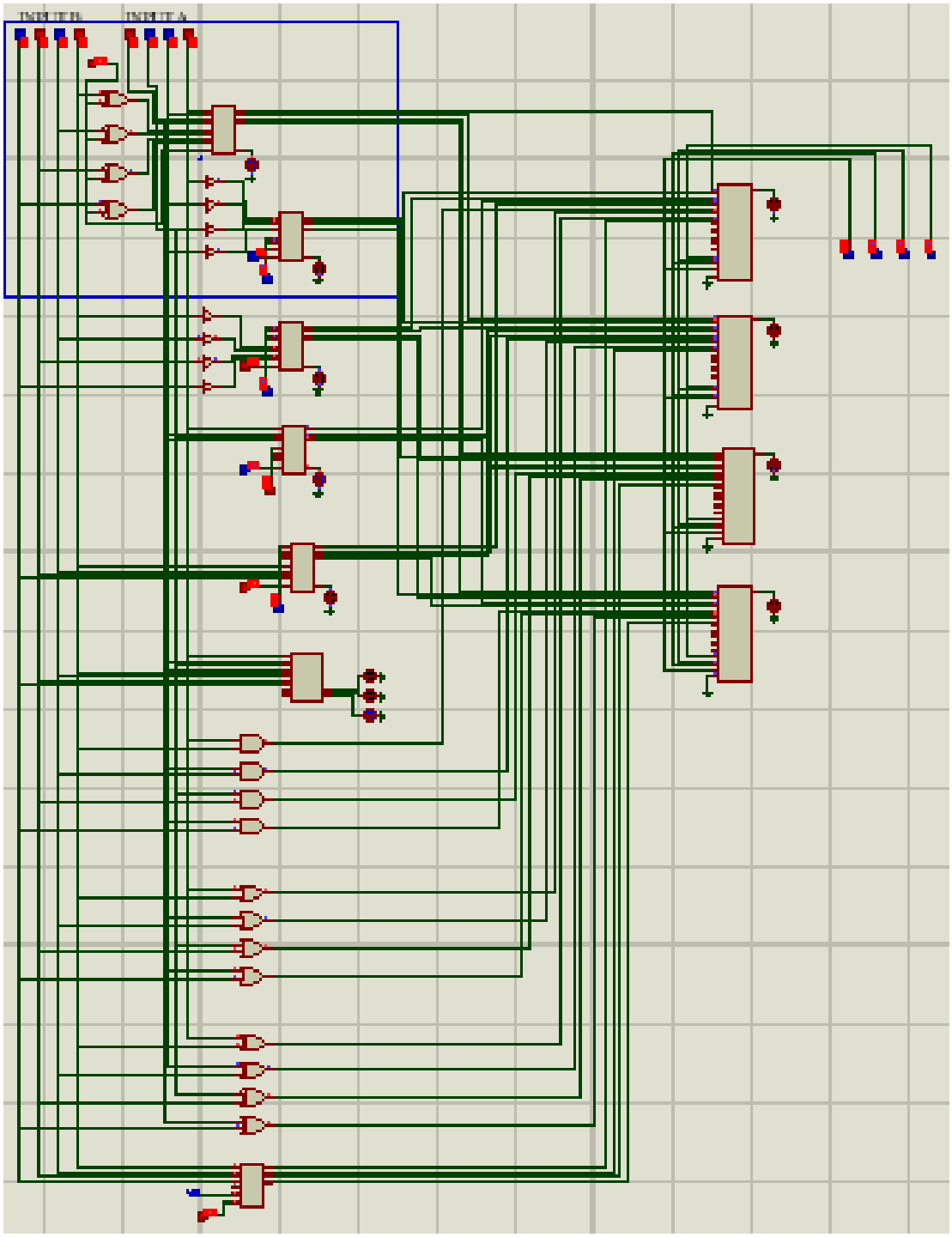
6. APPARATUS:

- Logic Unit.
- IC 74LS283.
- IC 74LS85.
- IC 74LS163.
- IC 7432.
- IC 7408.
- IC 7486.
- 16X1 MUX.
- Dip Switch.
- Jumper Wires.
- Resistors.
- Leds.

7. COMBINATIONS FOR VARIOUS OPERATIONS:

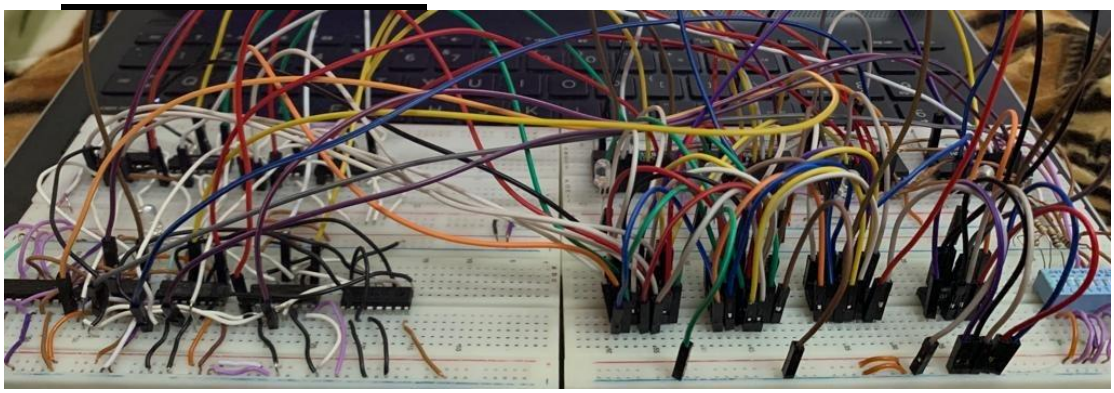
S3	S2	S1	S0	SEL.	OPERATIONS
0	0	0	0	0/1	Sum/Difference
0	0	0	1	0/1	1's & 2's Complement of A
0	0	1	0	0/1	1's & 2's Complement of B
0	0	1	1	0/1	Increment/Decrement of A
0	1	0	0	0/1	Increment/Decrement of B
0	1	0	1	X	Bitwise AND
0	1	1	0	X	Bitwise OR
0	1	1	1	X	Bitwise XOR
1	0	0	0	X	Clock/Load

8. SIMULATION IN “PROTEUS”:

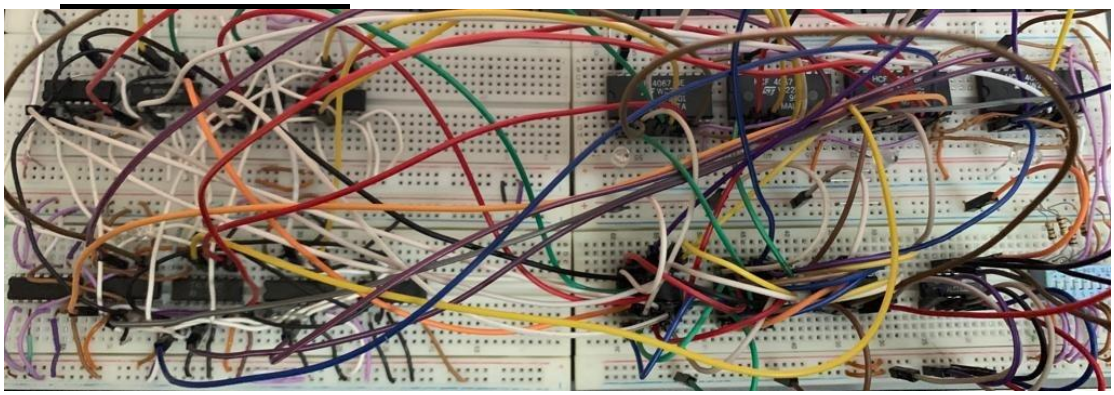


9. HARDWARE:

I. FRONT VIEW:



II.TOP VIEW:



III. SIDE VIEW: