NUST

NATIONAL UNIVERSITY
OF SCIENCES & TECHNOLOGY

PROJECT REPORT

Power Electronics

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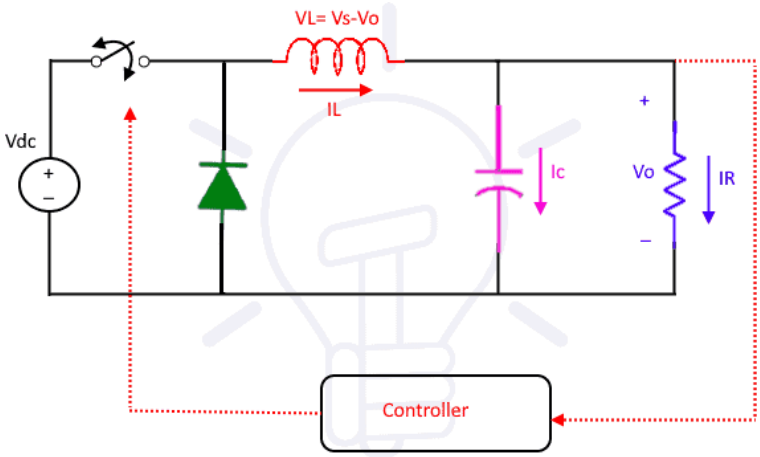
BUCK converter with feedback Design

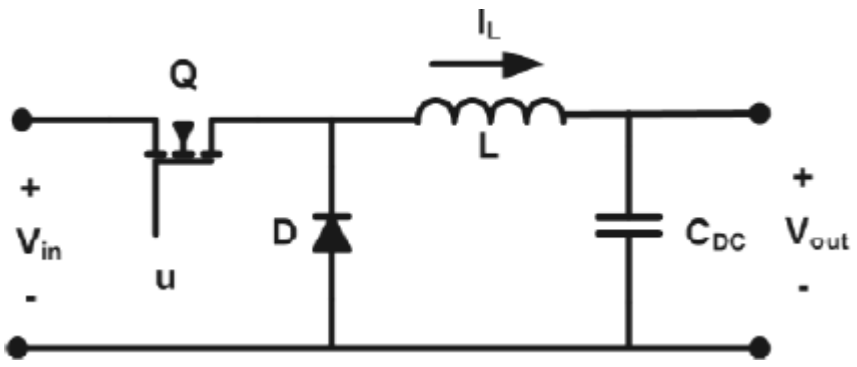


Buck Converter

Theoretical Background:

A buck converter, also known as a step-down voltage regulator, functions as a DC-DC converter by reducing a DC input signal to a lower DC output signal. Its primary advantage lies in its efficiency in power conversion. In contrast to using a voltage divider circuit, which incurs significant power losses, a buck converter offers an efficient means to achieve the desired step-down voltage.

The basic configuration of a buck converter, as illustrated in Figure 1, comprises a voltage source representing the input voltage to be reduced and a switching device, which can be a MOSFET, BJT, or similar component. This configuration is adaptable for both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), with the mode of operation contingent on the values of the inductor and capacitor in the circuit.

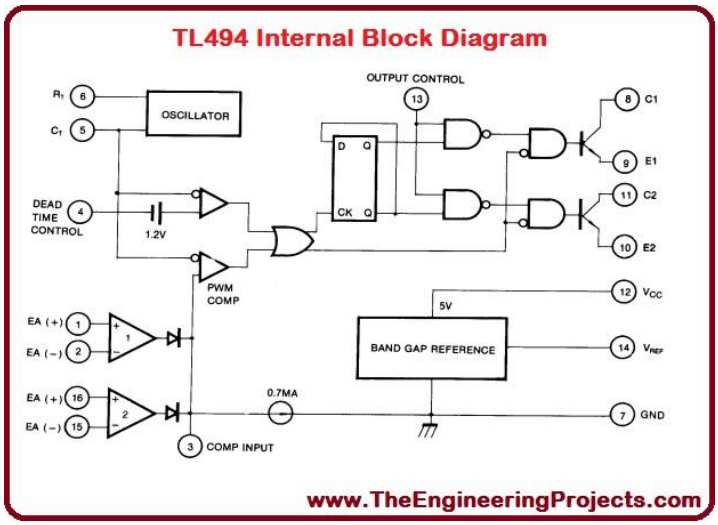


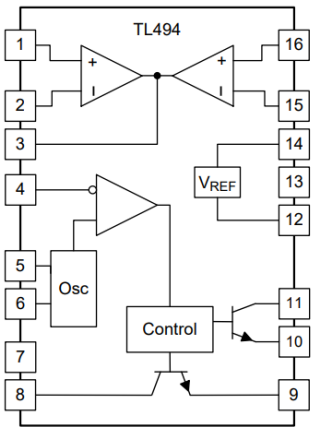
In Continuous Conduction Mode (CCM), the current through the inductor remains continuous, while in Discontinuous Conduction Mode (DCM), the current is non-continuous. The determination of the mode relies on the specific values of the inductor and capacitor, with critical values defined by corresponding formulas.

The duty cycle (D) of the Pulse Width Modulation (PWM) signal, applied to the control terminal of the switching device, is a key parameter in regulating the output voltage. The duty cycle is computed using the formula provided, where Vo represents the output voltage, and Vs represents the source voltage.

$$D = \frac{V_O}{V_S}$$

To generate the required PWM signal, a dedicated PWM generation Integrated Circuit (IC) such as the TL494 is commonly employed. The TL494 block diagram depicts its internal components and functionality, serving as a pivotal component in achieving precise control over the duty cycle and consequently, the output voltage level in the buck converter circuit.





The internal oscillator is responsible for controlling the frequency of PWM signal. The frequency of PWM signal is given by,

$$f = \frac{1}{RT * CT}$$

Two op-amps are also present which could be used in case of a controller design.

Feedback Design:

Our objective is to devise a feedback control loop responsible for handling input disturbances, namely variations in voltage and current. The output of this control loop is intended to be the duty cycle, serving as the gate signal for the MOSFET switch in the buck converter. The overall control system design is illustrated in Figure 3.

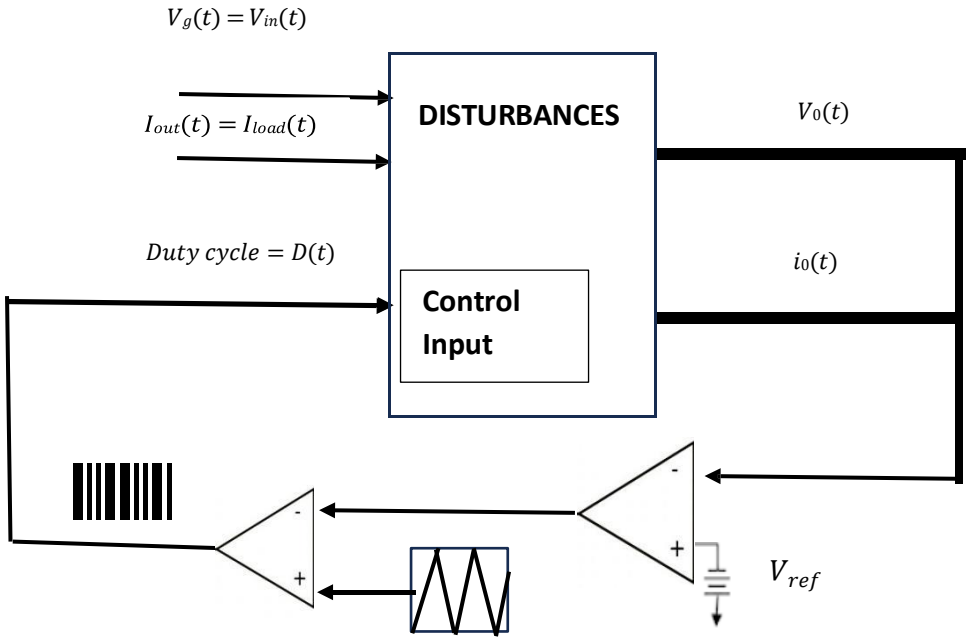


Figure 3 Control Feedback LOOP

The design incorporates an error amplifier functioning in saturation mode with an open gain. The subsequent operational amplifier (op-amp) is employed for frequency modulation. The error signal is then compared with a triangular waveform to generate the duty cycle, which acts as the control input for the system. The output voltage is subsequently utilized as feedback.

Control voltages necessary for the system are generated using a Proportional-Integral-Derivative (PID) or a modified PID controller. The implementation of this controller involves the use of operational amplifiers (op-amps). Our approach involves determining the open-loop transfer function for the buck converter. Following the establishment of the transfer function, the design of controller values will be carried out using the SISO tool. This tool aids in the systematic design and analysis of single-input, single-output (SISO) control systems, ensuring the optimal performance of the buck converter under various operating conditions.

Design:

For the design of the system, we must find the loop gain. In the process of designing the system, it is crucial to determine the loop gain, **which represents the cumulative gain around a**

feedback loop expressed either as a ratio or in decibels. The input signal is applied to the system with an open-loop gain denoted as A, and the output is fed back. Key requirements for the loop gain are outlined as follows:

- **High Gain at Low Frequencies:**

Requirement: The gain at low frequencies should be high.

Rationale: To ensure effective amplification and responsiveness to low-frequency input signals.

- **Dynamic Performance and Crossover Frequency Slope:**

Requirement: A better dynamic performance with a slope at the crossover frequency of -20 dB/dec, and a large stability bandwidth.

Rationale: To achieve a smoother transition between low and high frequencies, enhancing stability and overall system performance.

- **Faster Response at High Frequencies:**

Requirement: Faster response at high frequencies, with a slope ideally exceeding -20 dB/dec.

Rationale: To ensure robustness and quick adaptation to rapid changes in high-frequency input signals.

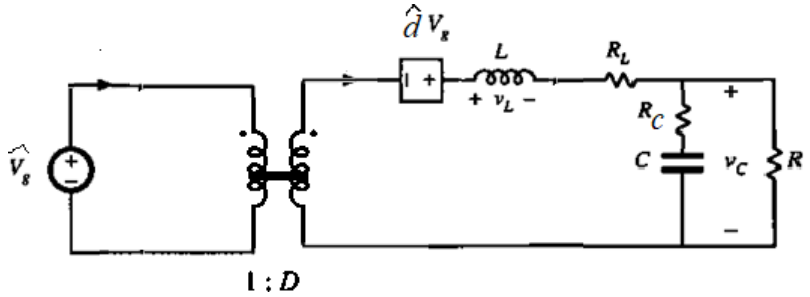
- **High Phase Margin:**

Requirement: Achieve as high a phase margin as possible.

Rationale: A higher phase margin is desired to minimize overshooting and oscillations, contributing to stable and controlled system behavior.

<u>Transfer Function:</u>

The transfer function for the open-loop system, which is fundamental for analyzing and determining the loop gain, is represented by a mathematical expression that has not been provided in the current context. To proceed with the design process, the specific transfer function would be required to assess the loop gain characteristics in accordance with the outlined requirements.



$$G_{vd}(s) = \left.\frac{\hat{v_0}(s)}{\hat{d}(s)}\right|_{\hat{v_{in}}=\hat{i}_{load}=0} \qquad \hat{v_o}(s) = \frac{R \,||\, Z_C}{Z_L + R \,||\, Z_C}\,\hat{d}(s)V_{in}$$

$$G_{vd} = \frac{\hat{v_o}(s)}{\hat{d}(s)} = \frac{R \parallel Z_C}{Z_L + R \parallel Z_C} V_{in}$$

Procedure:

For the design of the controller, we are using the SISO tool of MATLAB. For the design of the controller in SISO tool we have the open loop transfer function of the system that has been imported in workspace by the following code:

```
Vin=24;
Vo=9;
D=Vo/Vin
R=10;
Iout=Vo/R
rc=0.01;
C=47e-6;
L=3.0e-3;
rL=0.1;
fs=20e3;
Lcri=(Vo*(1-D))/(2*Iout*fs)
Ccri=(Iout)/(8*Vo*fs)
Vm=5;
s=tf('s');
zc=rc+1/(s*C);
zrc=R*zc/(R+zc);
Ztotal=rL+s*L+zrc;
Sz=1/(C*rc);
wo=sqrt(1/(L*C));
Q=1/(wo*(L/R+C*rc));
Qdb=20*log(Q);
fo=wo/2/pi();
vod=Vin*zrc/Ztotal
vodzpk=zpk(vod);
margin(vod);
voin=D/Vin*vod;
voinzpk=zpk(voin);
```

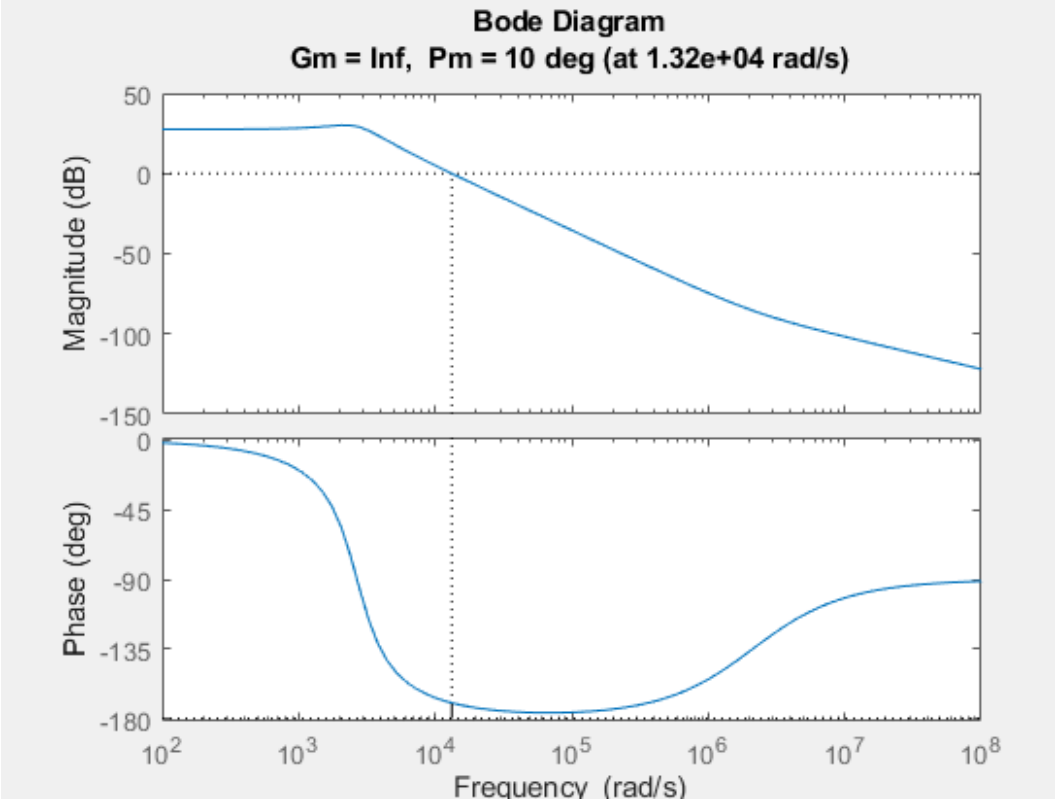
The open loop transfer function (vod) is as:

```
vod =

          1.172e-16 s^4 + 2.497e-10 s^3 + 5.302e-07 s^2
  ------------------------------------------------------------
  1.467e-18 s^5 + 6.289e-15 s^4 + 1.724e-11 s^3 + 2.231e-08 s^2

Continuous-time transfer function.
```

And the bode diagram of the above T/F looks like the figure below. The phase plot have not reached 180° due to the zero at high frequency in the transfer of the converter, we aim to design the PID controller for the phase margin greater than 70°.



Now we must design the PID controller. PID controller has two zeros and one pole at origin as integrator. As given:

$$C(s) = K_p + \frac{Ki}{s} + K_d s = = \frac{K_p s + K_i + K_d s^2}{s}$$

$$\begin{aligned} Where \quad & K_p = proportional\ gain \\ & K_i = integral\ gain \\ & K_d = derivative\ gain \end{aligned}$$

The controller design involves a series of steps to meet specific requirements and address challenges in the system. The outlined steps and modifications for the PID controller design are as follows:

1. **Addition of Integrator:**

- Purpose: Introduce an integrator to induce a change in DC gain at low frequencies, resulting in a -20dB/dec slope. However, this adjustment comes at the cost of reduced gain and phase margins along the crossover frequency.

2. **Multiplication of DC Gain:**
    - Purpose: Multiply the DC gain to shift the magnitude plot upwards, without altering gain and phase margins, crossover frequency, and system instability.
3. **Placement of Zero before Resonance Frequency:**
    - Purpose: Introduce a zero before the resonance frequency to enhance gain margin along the crossover frequency. This, however, leads to a decrease in phase margin.
4. **Placement of Second Zero after Resonance Frequency:**

    Purpose: Ensure system stability by introducing a second zero after the resonance frequency. This configuration results in a high phase margin, minimizing overshoot and ringing.
5. **Challenge with High-Frequency ESR Zero:**
    - Identified Problem: The presence of a high-frequency ESR zero causing a deviation in the magnitude plot from the desired -20dB/dec slope, impacting system stability.
6. **Modified PID Controller Design:**

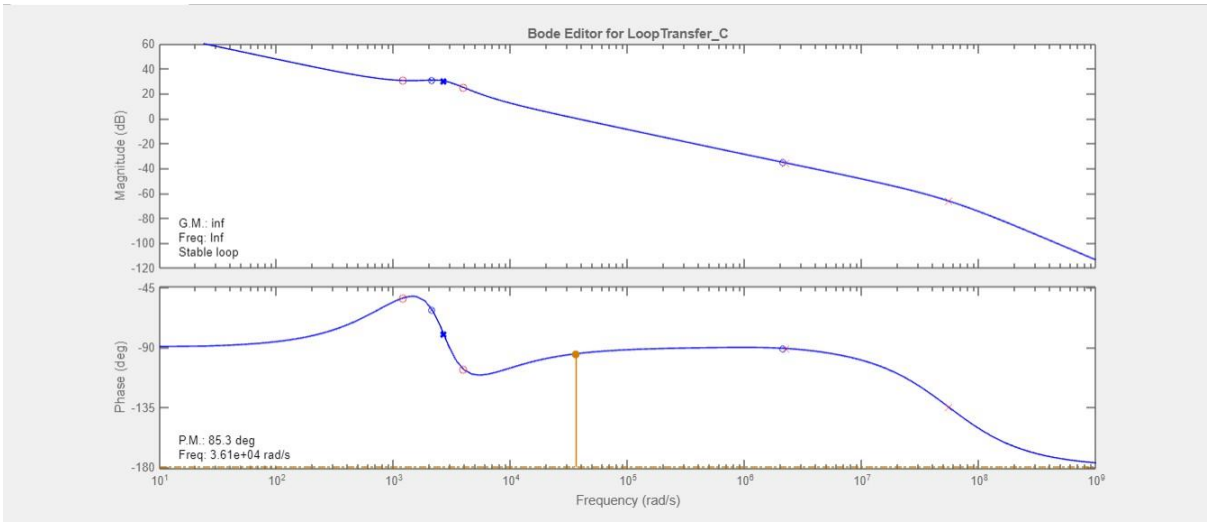
- Components:
    - An integrator for high DC gain.
    - Two zeros below the loop gain crossover frequency (fc) to compensate for excessive phase lag due to the integrator and the power stage complex pole pair.
    - Two high-frequency poles:
        - Purpose: Attenuate high-frequency noise, ensure magnitude decrease below 0dB, and minimize phase lag due to the poles at the crossover frequency.
    - Introduction of a 1st pole exactly at the high-frequency zero to cancel its effect.
    - Placement of a 2nd pole at a high frequency.

These modifications in the PID controller aim to fulfill design requirements, including achieving a desired magnitude slope at high frequencies, minimizing phase lag, and ensuring stability across the system's operational range. The finalized PID design integrates these elements for improved performance in the control loop.

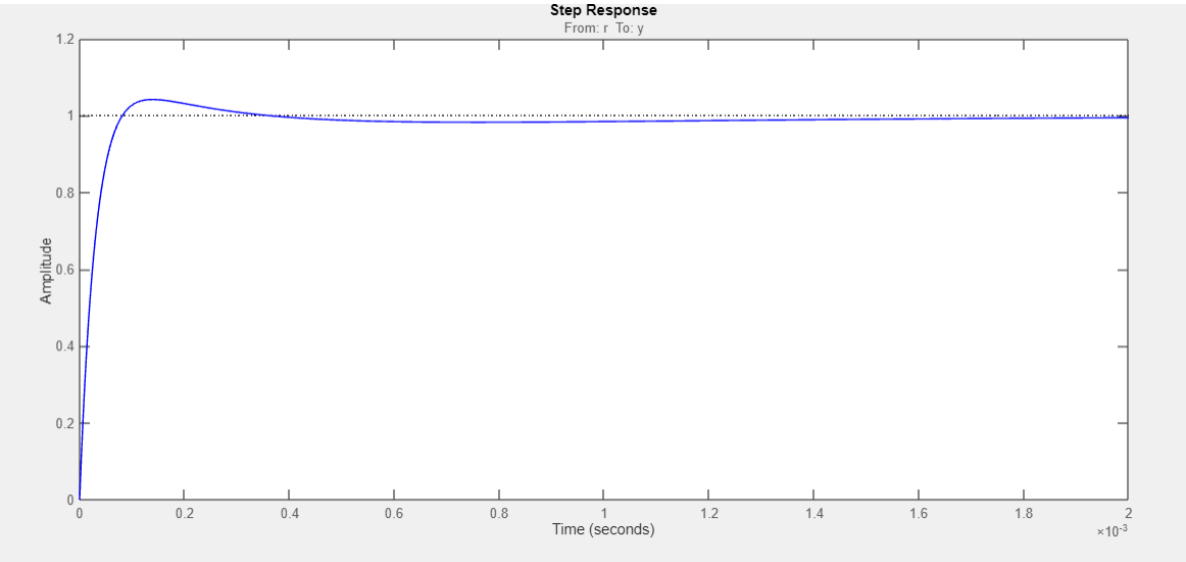
The designed controller is as given:

```
Tunable Block
Name: C
Sample Time: 0
Value:
  2.6061e10 (s+1207) (s+3943)
  ---------------------------
  s (s+2.257e06) (s+5.494e07)
```

The magnitude and phase plot for the controller is given as:

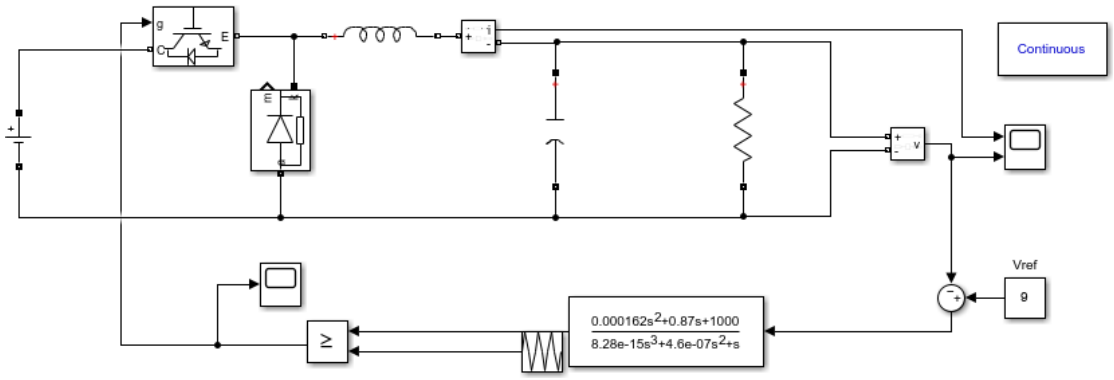


The step response is as follows:



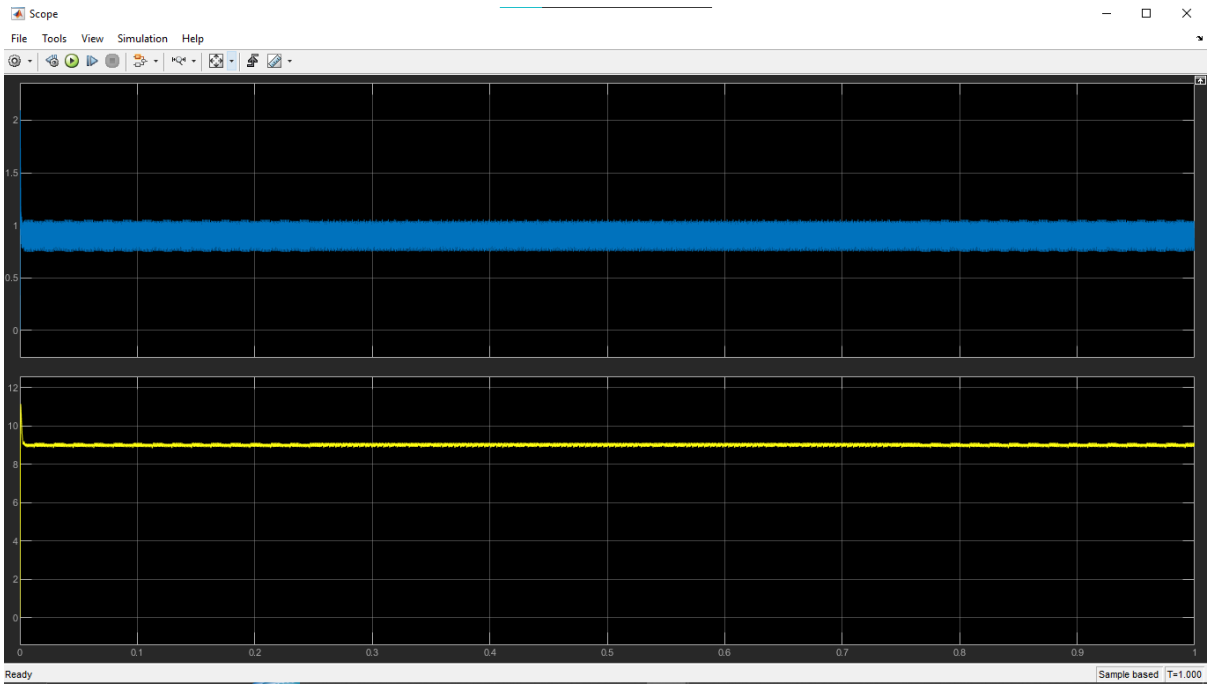
Circuit with feedback:

The overall circuit after the implementation of the designed modified PID controller for feedback is shown. The controller transfer function id written is feedback of the converter.

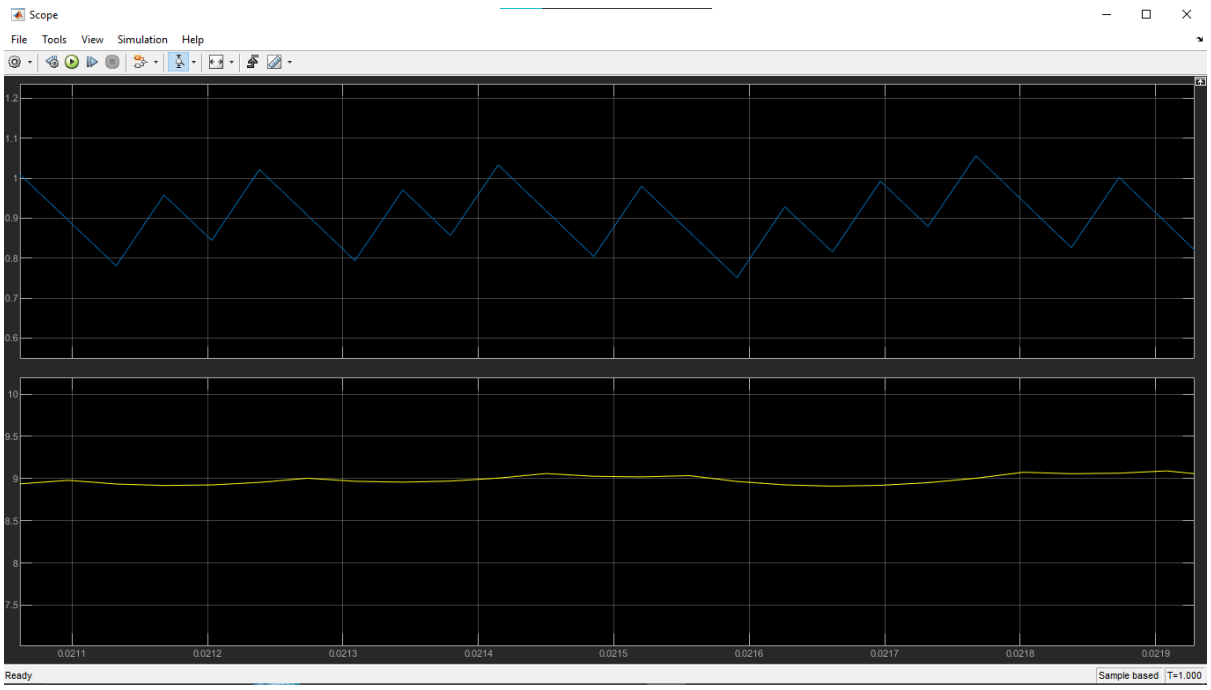


Output:

The output of the scope is as given:



Ripples:

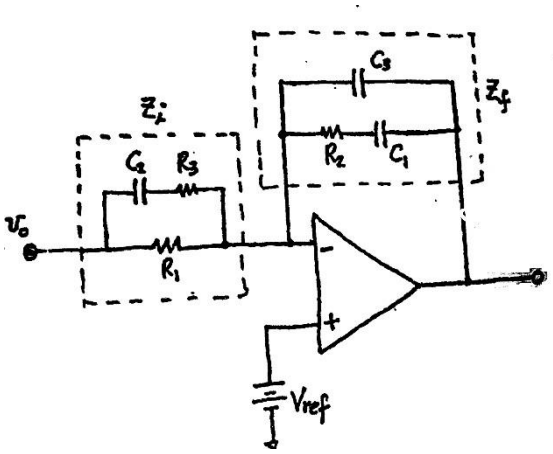


Current ripples from 0.815 to 1.05 A. While the steady state value is 9A. While the voltage ripples from 8.89 to 9.2 V and the steady state value is 9V.

PID with Op-amps:

Now we want implementations of modified PID using op-amp. The following is the figure of the op-amp circuit whose transfer function is identical to the controller T/F of the PID controller. Hence, we can implement the controller using the given relation.

The op-amp and it's transfer function:



$$\frac{\mathbf{v}_c}{\mathbf{v}_0} = -\frac{z_f}{z_i}$$

$$z_i = R_1 \| \left(\frac{1}{sC_2} + R_3 \right)$$

$$Z_f = \frac{1}{sC_3} \| \left(\frac{1}{sC_1} + R_2 \right)$$

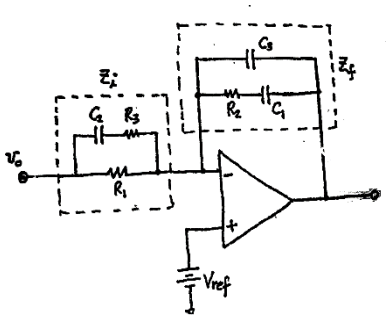
The modified controller has the following T/F:

```
Tunable Block
Name: C
Sample Time: 0
Value:
  2.6061e10 (s+1207) (s+3943)
  ---------------------------
  s (s+2.257e06) (s+5.494e07)
```

Thus, we can compare both to get the values for Rs and Cs.

For $C_1 >> C_3$, $R_1 >> R_3$

$$\frac{\mathbf{V}_c}{V_0} = -\frac{\omega_i}{s}\frac{(1+s/\omega_{Z1})(1+s/\omega_{Z2})}{(1+s/\omega_{p1})(1+s/\omega_{P2})}$$



$$\omega_{z1} = \frac{1}{R_2 C_1}, \quad \omega_{z2} = \frac{1}{C_2 (R_1 + R_3)}$$

$$\omega_1 = \frac{1}{R_1 (C_1 + C_3)} \quad \omega_{P1} = \frac{1}{R_3 C_2}, \quad \omega_{P2} = \frac{1}{R_2 \cdot \frac{C_1 C_3}{C_1 + C_3}}$$

We can compare the equation of controller and the above op-amp equation as we know the poles and zeros frequency from the controller transfer function. We have used the below MATLAB code to get the values for Rs and Cs:

```
clc
clear all;
wi=1000;
wz1=1207;
wz2=3943;
wp1=2.25e6;
wp2=5.49e07;
C1=1e-06;
R1=1/(C1*wi)
C2=1/(R1*wz2)
R2=1/(C1*wz1)
R3=1/(C2*wp1)
C3=1/(R2*wp2)
```

Following are the values of Rs and Cs:

```
R1 =

        1000


C2 =

   2.5361e-07


R2 =

  828.5004


R3 =

    1.7524


C3 =

   2.1985e-11
```

The next step is to implement this circuit using TL-494.

Specifications:

Following are the specifications for the Buck converter:

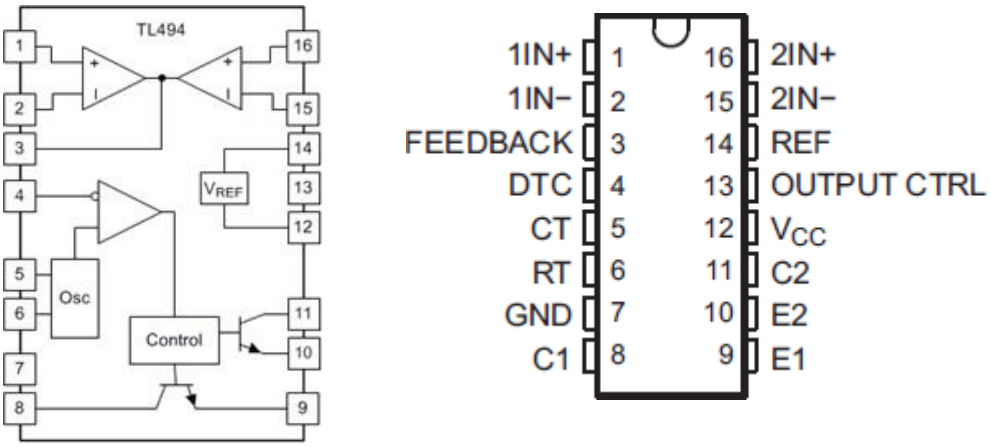
fs	**Vout**	**Vin**	**Vr(p-p)**	**RL**
20 kHz	*12 V*	*24 V*	*< 5%*	*20*

Components:

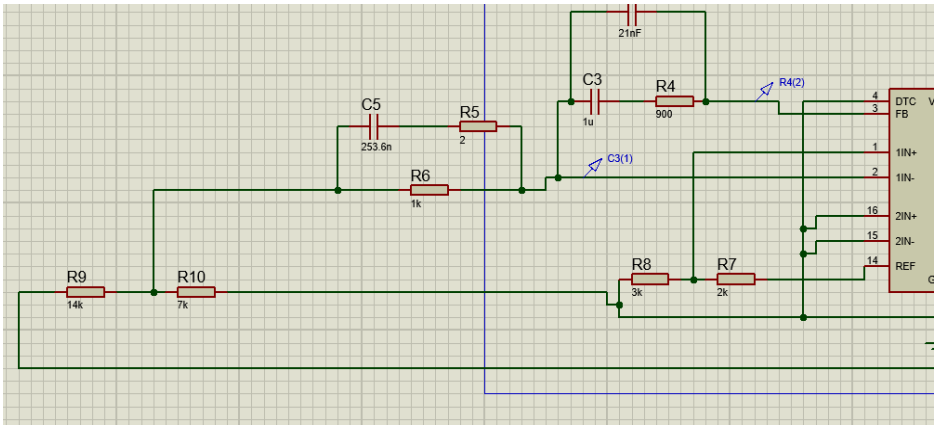
1. TL494
2. MOSFET-1RF530
3. Capacitors
4. Inductors
5. Resistors
6. Power Supply

Implementation using TL-494:

We are doing to use the internal op-amp of the IC TL-494 with feedback pin (1,2,3,15,16 pin) to implement the controller on hardware and proteus. The internal op-amp of TL-494 looks like the figure given below.

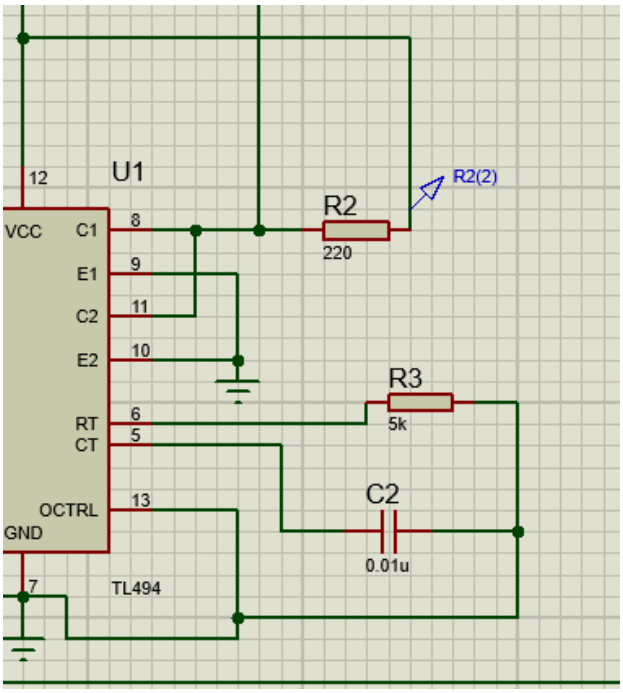


In the above figure we can see that the IC has 2 op-amps. We can use only one op-amp to implement the controller i.e. pin 1,2,3 where pin 3 acts as a feedback pin. The implemented circuit using the pin 1,2,3 is as shown:



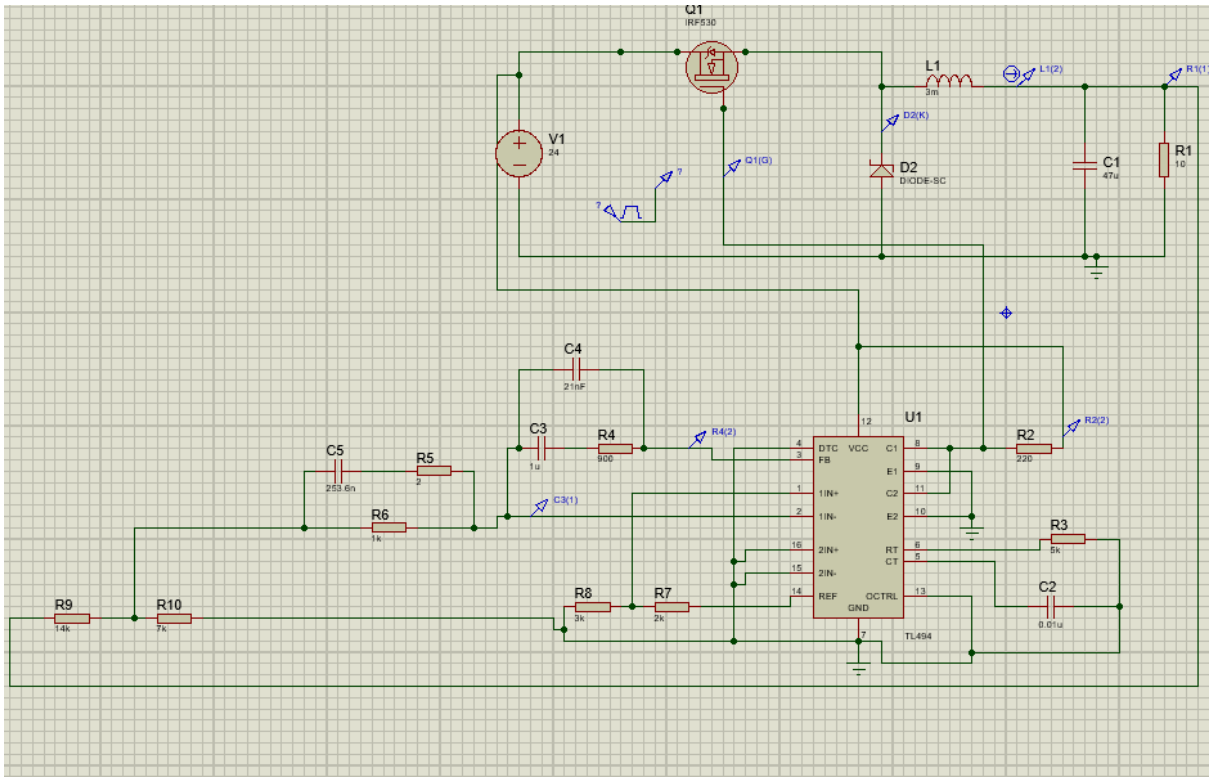
Here, we have used pin 1 to give the reference and pin 2 for the output feedback from buck converter. At pin 2 and pin 3 pin we have implemented the same circuit of controller. We have used voltage dividers at pin 1 and pin 2 to prevent the feedback pin 3 from voltage higher than 3V. At pin 2 and pin 1 we have stepped down the voltage.

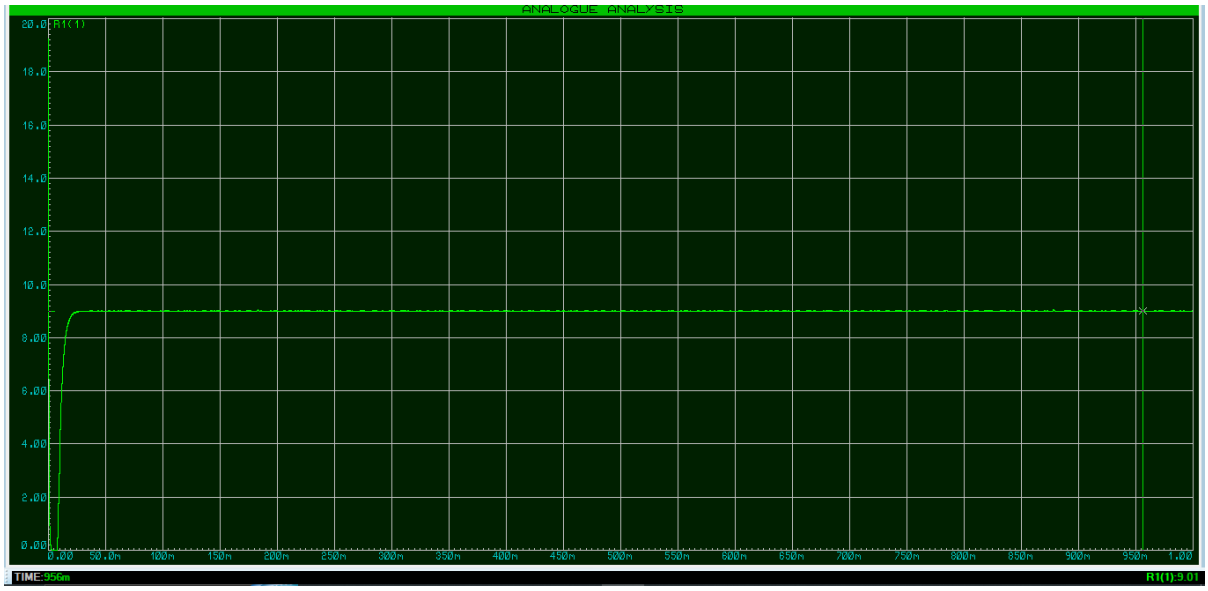
We then grounded pin 13 of the TL-494 for single ended mode. Using RT and CT pins we have set the switching frequency to 20Khz. We are using the internal BJTs of the IC in common Emitter configuration for better β stability.



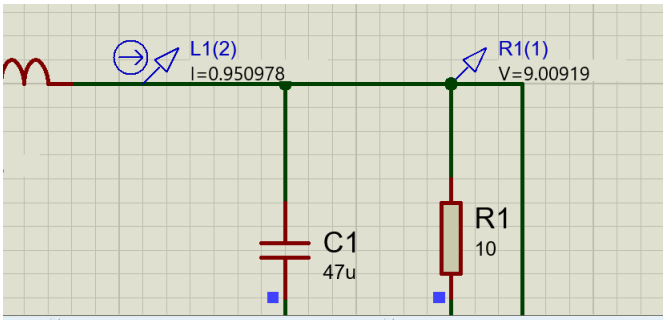
Final Stimulation:

The overall circuit of the buck converter with feedback is as follows:



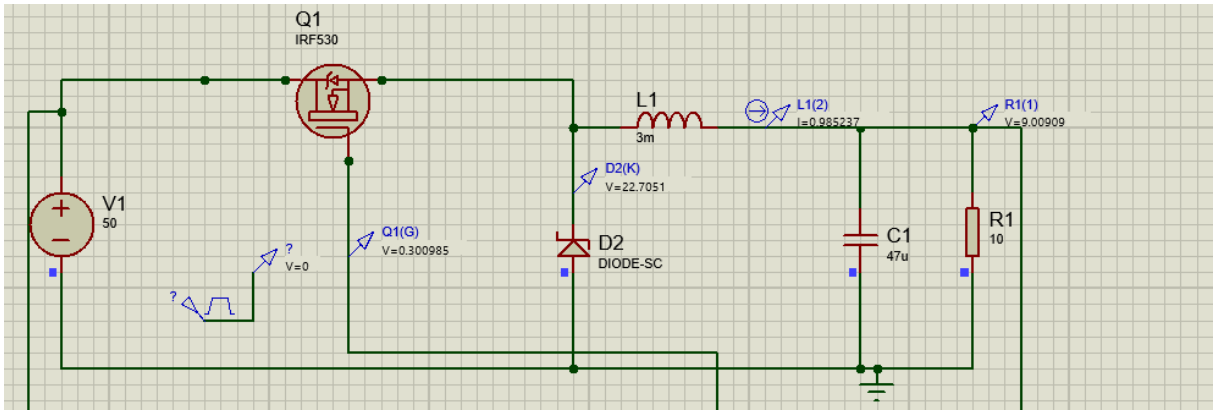


The output voltage and current are as:

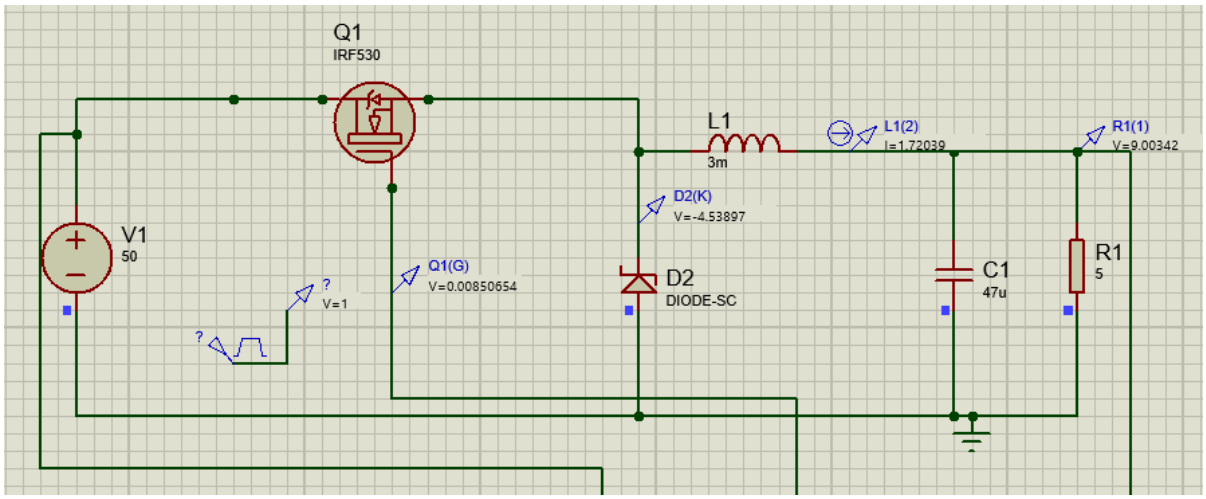


Robustness Test:

By increasing the input voltages from 24 to 50 we will test the controller efficiency to maintain the output voltage to 9V. The schematics of the circuit is attached:



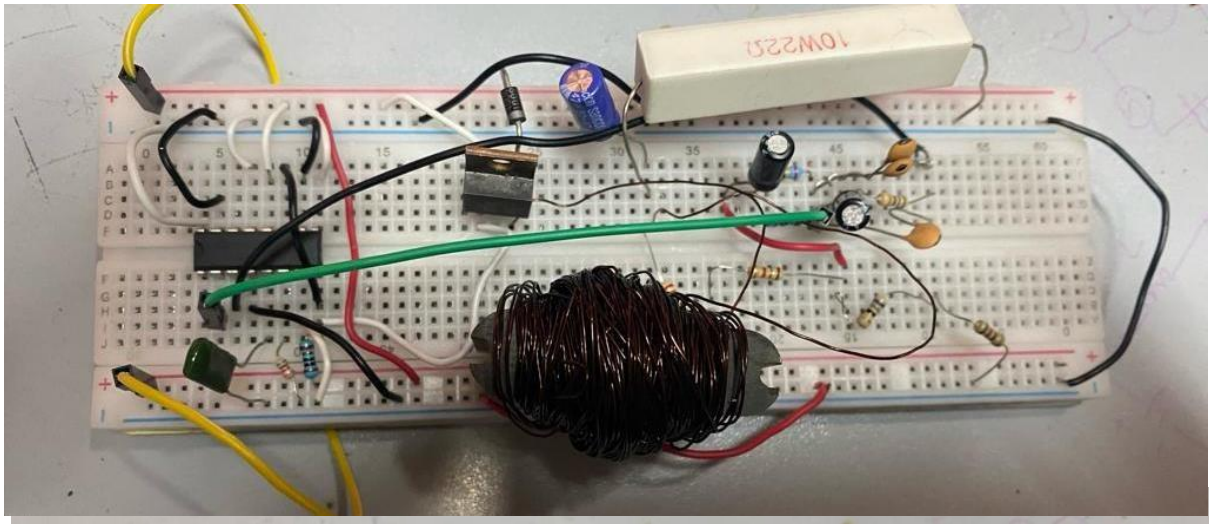
As we can see, the output voltage is still 12V. We can also alter the load resistance to see if the circuit still works well or not.

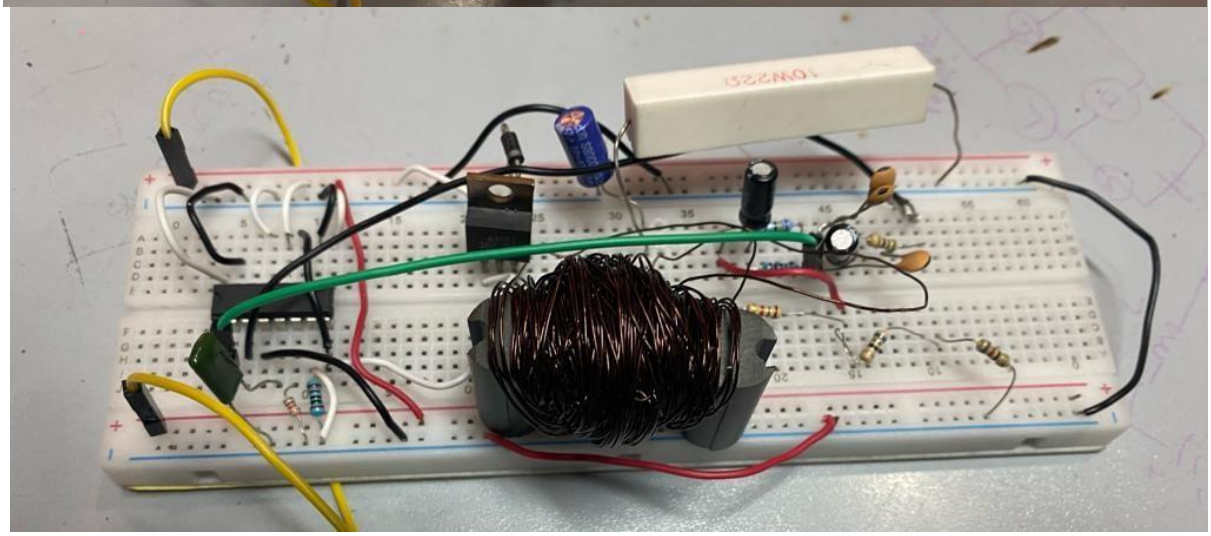


Changing the load resistance and input voltages has no effect on the output voltages that verify the robustness of controller design.

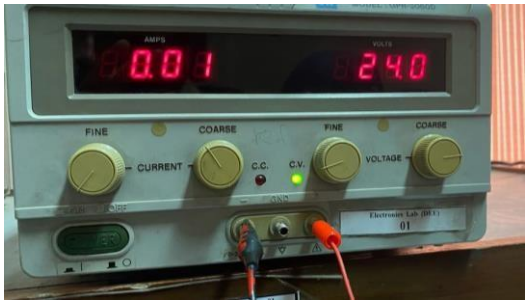
Hardware Implementation:

We have implemented the above circuit on hardware the results and circuit are attached:





Input voltagess:



Reference at IN- ***Input Signal***

Output:

The output was shown on DMM:

Conclusion:

We have successfully implemented and designed the feedback control of the buck converter. The feedback loop consists of the TK-494 IC with feedback from the output voltages. We have achieved the required results on the hardware as well.