The Past, Present, and Future of Silicon Photonics

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(Invited Paper)

***Abstract*—The pace of the development of silicon photonics has quickened since 2004 due to investment by industry and government. Commercial state-of-the-art CMOS silicon-on-insulator (SOI) foundries are now being utilized in a crucial test of 1.55-μm monolithic optoelectronic (OE) integration, a test sponsored by the Defense Advanced Research Projects Agency (DARPA). The preliminary results indicate that the silicon photonics are truly CMOS compatible. R&D groups have now developed 10–100-Gb/s electro-optic modulators, ultrafast Ge-on-Si photodetectors, efficient fiber-to-waveguide couplers, and Si Raman lasers. Electrically pumped silicon lasers are under intense investigation, with several approaches being tried; however, lasing has not yet been attained. The new paradigm for the Si-based photonic and optoelectric integrated circuits is that these chip-scale networks, when suitably designed, will operate at a wavelength anywhere within the broad spectral range of 1.2–100 μm, with cryocooling needed in some cases.**

***Index Terms*—CMOS, electroabsorption, Ge photodetectors, GeSn, optoelectronic integrated circuits, photonic crystals (PhCs), photonic integrated circuits (PICs), plasmonics, SiGeSn, silicon lasers.**

I. Introduction

The goal of this paper is to set the stage for the invited and contributed papers in this issue by reviewing the history, the present status, and the future prospects of silicon photonics. This work emphasizes what has been done on the key components and their optoelectronic (OE) integrations. An attempt will be made to identify the emerging trends and remaining challenges.

Works in this special issue represent the leading edge of the photonics field. The topics covered include Raman lasers, photonic crystals (PhC), fast modulators, light-emitting diodes (LEDs), photodetectors, microresonators, plasmon optics, quantum-cascade structures, photonic-circuit integration, and OE integration. I shall touch briefly on these topics, and will add a few words about the quest for electrically pumped silicon lasers, electric field effect modulators, and photonic integrated circuits (PICs) for the mid-wave, long-wave, and far-infrared regions.

II. Propitious Times for Silicon Photonics

The years 2004 and 2005 were propitious for silicon photonics—and the prospects for 2006 and beyond look quite bright. The year 2004 marked the launch of the First International Conference on Group IV Photonics (GFP), sponsored by the IEEE Lasers and Electro-Optics Society. This conference, convened initially in Hong Kong, is the first ongoing global meeting devoted solely to silicon photonics. The year 2004 also witnessed the ramping up of the investment in silicon photonics research and development by government and industry, as mentioned here. The investment led to a surge of activity as new R&D groups engaged themselves in the silicon mission. The pace of the progress accelerated during 2004–2005. That momentum persists today. In 2004, the European Union started its Silicon Heterostructure Intersubband Emitter (SHINE) program, a three-year team effort to develop silicon-based SiGe/Si quantum-cascade structures emitting at a wavelength in the range of 8–120 μm. SHINE was created several years after the 1999–2003 Defense Advanced Research Projects Agency (DARPA) terahertz technology program that sponsored two SiGe/Si quantum-cascade laser projects [1], [2]. University teams began work this year on a three-year project to make room-temperature electrically pumped 1.55-μm silicon-based lasers. This work is funded by the Air Force Office of Scientific Research, an office that has sponsored silicon photonics research since 2002 through grants and the small-business technology transfer program.

In the beginning of December 2004, the DARPA microelectronics technology office made a major investment in 1.55-μm silicon photonics with its four-year project on electronic and photonic integrated circuits (EPIC) in silicon. The principal goal of EPIC (website: www.darpa.mil/mto/epic) is the monolithic integration of silicon very large scale integration (VLSI) electronics with silicon nanophotonics on a single silicon chip in a commercial state-of-the-art CMOS silicon-on-insulator (SOI) production plant (foundry). The seamless photonics–electronics interface will piggyback upon CMOS infrastructure and progress.

III. A Glance at History

G. Reed has presented a fine, detailed history of this field [3], and I shall only add a few remarks to his, beginning with a comment on wavelength. Silicon photodiodes are excellent detectors at wavelengths shorter than 1.2 μm (near IR, visible, UV); however, telecommunication occurs beyond 1.2 μm. The integrated photonics field began after it was recognized that the transparency of silicon at $\lambda > 1.2$ μm would allow silicon itself to be a waveguide medium for the 1.3- and 1.55-μm fiber-optic transmission wavelengths—the silicon photonic chip thus an adjunct to the fiber-optic network. Later, it became clear that the silicon substrate can also be a platform for the visible and 850-nm waveguiding using the silica-on-silicon "planar lightwave circuit" approach (Ge-doped silica on silica on Si) or the

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silicon-nitride waveguide approach (silicon oxynitride on silica on Si). Since the beginning, OE integration upon silicon has been a prime motivation.

After this integrated photonics field was founded in about 1985 [4], [5], the questions that were addressed included the following.

1) What is the optimum construction of the waveguides (materials, index contrast)?
2) How is low-loss propagation achieved?
3) Geometrically, what is the single-mode condition?
4) How will efficient fiber-to-waveguide couplers be built?
5) How can ultrafast, high-responsivity detectors of 1550 nm be made on silicon?
6) Can the free-carrier effect be used for fast electromodulation?
7) What is the way to make good filters, resonators, couplers, electrooptical switches, and wavelength division multiplexers?
8) Which strained-layer heterostructures are useful?

Practical answers to most of these questions were found during the 1990s. Progress on heterogeneous and monolithic OE integration was made during 1990–2003, although the scale of integration was small. PhC structures in silicon, both two-dimensional (2-D) and three-dimensional (3-D), came strongly onto the photonics scene after 2000. Plasmonics in Si is a recent addition.

Following K. Wang's early work on SiGe/Si infrared sensors and the band-offsets in these heterostructures, the properties of the SiGe/Si strained-layer system were explored by many others who looked at light emission, detection, waveguiding, switching, and the formation of multiple quantum wells (MQWs). Later, crystal SiGeC and SiC alloys were used for some of these functions. That was followed by the development of crystalline GeSn upon Ge or Si. Silicon-based quantum dots of SiGe, Ge, and SiSn were developed, although the early dots had a pancake shape.

Radiative recombination of electrons and holes across the indirect bandgap of bulk crystal silicon is weak and the consequent lack of the efficient silicon LEDs and electrically pumped silicon lasers has been a serious deficiency of this photonics field because, without these light sources, a complete suite of the photonic components is not available for monolithic on-chip integration. Some people have regarded the emitter deficiency as a basis for skepticism, saying that silicon photonics will never be viable or practical. Others said that the deficiency represented a scientific challenge, a light-emitter problem that could be solved with ingenuity and creativity, thereby enabling a revolutionary silicon OE technology. It should be added that silicon photonics in its present state—without on-chip Si laser diodes—is still excellent in the sense that the chip can be "actuated" by an off-chip III–V laser serving as a "photon supply" analogous to the dc electrical supply that powers electronics. Heterogeneous on-chip integration of III–V laser diodes is another strategy.

Nanocrystals have entered the light-emission picture along with quantum wells (QWs) and quantum dots. Porous-silicon light emission is a unique, although probably unstable, approach. Years ago, taking a cue from Er-doped fiber amplifiers, the doping of Si with erbium ions was found to be a good approach to 1550-nm emission; however, the emission from Er in amorphous layers is actually stronger than that from Er-implanted crystal.

In my review papers [6]–[10], I have pointed out that silicon photonics is a multidisciplinary field that requires new physics, materials science, and several kinds of engineering—a wide-ranging field that, in principle, offers low-cost, reliable, chip-scale "systems" for the applications listed in Section IV.

IV. Present Achievements

The recent explosion in Si photonics is driven mainly by the development of high-volume optoelectronic integrated circuit (OEIC) chips and secondarily by the development of practical photonic ICs (both in SOI). It has been demonstrated that one OEIC chip can contain essentially all of the electronic and photonic components that are necessary to make a fast, bidirectional optical communication link with another OEIC chip (or to make links within one chip). That is why I believe that the silicon OEIC is the best platform for optical interconnects. Optical interconnects are being developed in a hierarchy that ranges from rack-to-rack, board-to-board, and chip-to-chip, down to intra-chip. Photonic interconnects for a new generation of computers are probably the most important applications of silicon photonics—however, in addition, the OEIC has the potential for new applications and technologies because the cost-effective, intimate integration of complex photonics with electronics can solve technical problems that neither microelectronics nor conventional photonics could handle alone. There is an on-chip OE "synergy" that opens up new functionality and higher levels of performance.

If we look across the range of present and potential uses of silicon photonics, we can identify applications in photonic interconnects, data communication, telecommunication, specialized signal processing, switched networks, imaging, displays, radio frequency/wireless photonics, electronic warfare, photonics for millimeter-wave/microwave/radio-frequency systems, laboratory-on-a-chip, medical diagnosis, spectrometer-on-a-chip, photonic sensing of chemical/biological/physical variables, sensor fusion, neural networks, bionics, analog-to-digital conversion, optical storage, optical logic, electrooptical logic, and testing of CMOS circuits. (Regarding the CMOS testing, whether some transistors in an IC are defective can be determined either from their emission of visible light, or by probing them with 1064-nm laser light [11].)

A. Electronic and Photonic Integration

The organizations currently investigating electronic and photonic integration under DARPA EPIC are the BAE Systems team (electronic warfare application-specific EPIC), the Luxtera team (CMOS photonics technology), the Lincoln Laboratory team (high-resolution optical sampling technology), California Institute of Technology (optical signal amplification in silicon), UCLA (nonlinear silicon photonics), Translucent (low-cost buried photonic layer beneath CMOS), University of Michigan (CMOS-compatible quantum dot lasers grown

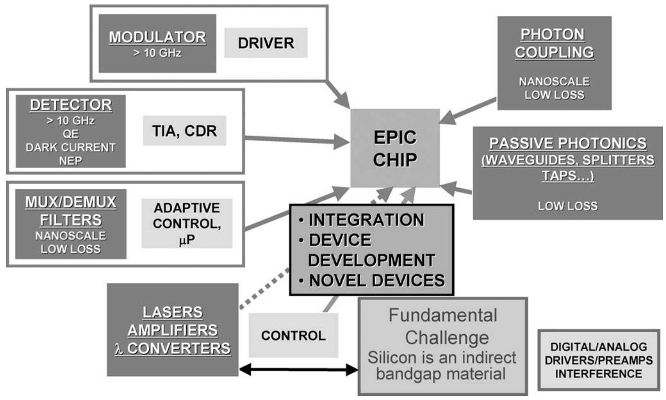

Fig. 1. EPIC challenge (reprinted courtesy Dr. J. Shah).

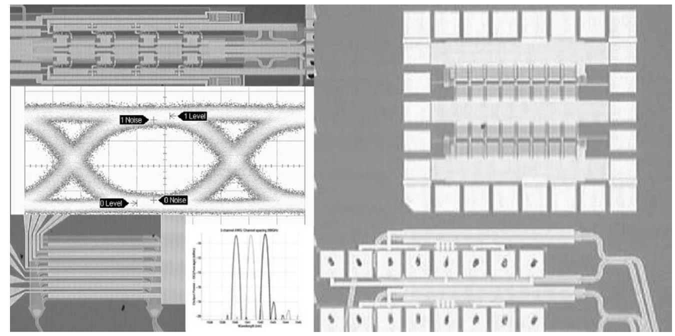

Fig. 2. Top view of 10-Gb/s 1.55-μm electrooptical modulator with its eye diagram (*upper left*), electrically trimmed wavelength division multiplexing filter with its spectral response (*lower left*), RF amplifier (*upper right*), and two 1×2 electro-optical switches for 1.55 μm (*lower right*) (reprinted courtesy Dr. C. Gunn).

directly on Si/SiGe), Stanford University (germanium quantum wells on silicon substrate for optical modulation), and Brown University (all-silicon periodic nanometric superlattices toward a silicon laser). Because EPIC has become an important force shaping the future of silicon photonics, I shall briefly summarize a few EPIC results from 2004 to 2006. As illustrated in Fig. 1, the EPIC vision [12], [13] is to demonstrate a complete suite of high-performance nanophotonic devices in an application-specific EPIC chip. The BAE Systems team is developing chips in their 90-nm radiation-hardened SOI CMOS foundry, while the Luxtera team is using the 130-nm SOI CMOS foundry of Freescale Semiconductor for fabrication of their OE chips.

The BAE team has already constructed an analog-signal 300 MHz through 2.2-GHz RF/photonic receiver-on-a-chip that can intercept and monitor individual RF emitters in the environment. Compared to prior channelizers, the 18-GHz BAE Phase-3 chip will offer a $4.5\times$ increase in the instantaneous bandwidth, $95\times$ size reduction, $80\times$ weight reduction, $5\times$ power reduction, and $100\times$ cost reduction. BAE as well as Luxtera are now creating open-architecture optical component libraries. These automated photonic-design tools (software linked to experimental results) are compatible with commercial CMOS processing.

Luxtera has developed a 10-Gb/s fiber-optic transceiver OE chip that includes a silicon 10-Gb/s modulator, a flip-chip-bonded 1.55-μm III–V laser diode, a high-speed Ge-on-Si photodiode, a low-speed photodiode, and an efficient fiber-to-waveguide coupler. The active devices are monolithically joined to CMOS drivers, controllers, and transimpedance amplifiers. Luxtera is also developing wavelength-division-multiplex scaling of its transceivers to achieve 100-Gb/s performance. As of early 2006, Luxtera has built and tested monolithic OE chips containing about 100 photonic components and 200 000 transistors. At present, the silicon transceiver (intended mainly for the box-to-box interconnects) is the most "real" and economically important photonic interconnect chip.

Gunn [14], [15] has described the Luxtera components that were integrated in a single "film" of silicon. Several of these are illustrated in Fig. 2. The company made an experimental test of 1.55-μm optical coupling between single-mode fiber and SOI strip waveguide, as shown in Fig. 3. The fiber in Fig. 3 is

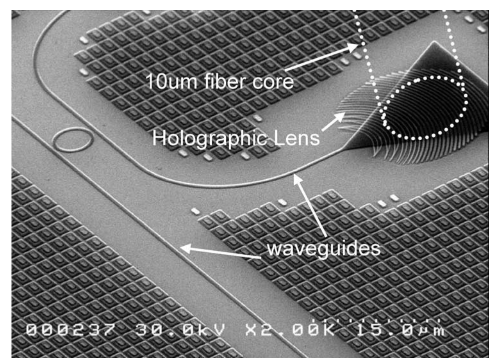

Fig. 3. Microscope photographs of SOI integrated-photonic test network including microring filter and fiber-to-waveguide coupler (reprinted courtesy Dr. C. Gunn).

joined at a normal incidence to the photonic network plane, and the holographic grating gives efficient coupling of the fiber light into the silicon waveguide. An alternative endfire (butt coupling) technique has been developed by the BAE team using Si strip waveguides that are tapered down to subwavelength dimensions. They found that the mode expansion in the taper provided single-mode fiber-to-chip coupling at an unpolished saw-cut silicon surface [16]. Coupling was spectrally broad and polarization-independent with low insertion loss. Both BAE and Luxtera favor Ge-on-Si photodiodes for high-volume manufacturing. The chemical vapor deposited 1.55-μm Ge photodetectors are fast [17], responsive, efficient, and waveguide-integrated.

Elsewhere in this issue, L. Kimerling presents the vision of the optical and electronic "convergence" on silicon developed by the MIT Microphotonics Center in conjunction with its many industrial partners [18]–[20]. Their Si OE Communications Technology Roadmap, which goes out to 2030, is synergistic with that of DARPA and emphasizes the commercial rather than the military perspective. They say that the standardized optical carrier utilization will ignite a change from information transmission (telecommunication) to information processing (computing and imaging) that will open high-volume applications [21]. MIT, in conjunction with its BAE-Systems partner, has made prototype chips that employ two vertically stacked photonic circuits on top of the CMOS to obtain sophisticated OE integration [16]. The waveguides at upper levels are dense-nanocrystalline-deposited silicon. Jalali and coworkers at UCLA have experimentally proven an alternative approach in which the photonic layer (containing, for example, an inplane-coupled microdisk resonator) is buried beneath the silicon CMOS layer in a subterranean fashion [22]. An advantage of the MIT approach is the dense 3-D integration of the photonic components within a small footprint. The single-layer approach of Luxtera is also quite practical because they have solved the problem of "preserving" the transistors beneath the photonics. The UCLA approach offers simple fabrication, however, they must control the transistor processing temperatures so as not to injure the active photonic materials below the CMOS.

B. Silicon Raman Lasers

The papers in this special issue reveal the progress that has been made in the fields of Raman lasers, PhCs, fast modulators, LEDs, photodetectors, microresonators, plasmon optics, quantum-cascade structures, photonic-circuit integration, and OE integration. The development of the silicon Raman laser, mainly by the groups at UCLA [23] and Intel Corporation [24], was a dramatic milestone in the history of silicon photonics. Although this laser has low gain per unit length in its initial versions, the device is fully integrateable and offers tunability by design, that is, by the choice of alloy composition x in the waveguide core made of $Si_{1-x}Ge_x$, or by the use of higher order Raman shifts in the resonator. Looking to the future, it seems likely that performance improvements will be made in lowering the intensity threshold for optically pumped lasing and in migrating the wavelength of the operation toward the 3–5-μm region. The main drawback of this laser is its need for optical pumping (it takes a laser to make a laser). Electrically pumped lasers are usually more desirable in OE chips. Such pumping is discussed below.

C. Erbium–Silicon Lasers

Barrios and Lipson have simulated the 1550-nm emitting properties of an electrically driven resonant-cavity LED consisting of Er-doped SiO_2 situated in the central slot of a rib-waveguided microring resonator [25]. Biasing of lateral P^+-doped regions inside and surrounding the ring gives MOS excitation of the active slot material. These authors predict efficient electroluminescence coupled into the adjacent SOI channel waveguides, and they say the device has potential for lasing.

When rare-earth ions are implanted into an amorphous SiO_2 layer containing Si nanocrystals, an efficient LED can be made by injecting electrons into the oxide using biased P- and N-silicon layers sandwiching the thin film [26]. The researchers at ST Microelectronics boosted the directionality of Er:Si LEDs to attain laser-like 1540-nm emission from a vertical, resonant-cavity LED employing Si/SiO_2 distributed Bragg reflectors [26]. They say the laser is within reach.

Physically, the rare-earth doping is an "extrinsic" or guest–host effect whose strength is limited by the concentration of ions. Extrinsic is a disadvantage because the number of rare-earth ions per cubic centimeter is much less than the number of Si atoms per cubic centimeter. Having said that, it should be noted that A. Polman has achieved 1550-nm lasing in Er-doped (2×10^{19} cm^{-3}) 15-μm diameter SiO_2-toroids mounted on silicon, although this laser was optically pumped at 1480 nm [27]. The remaining technical challenges in making an electrically pumped room-temperature Er:Si laser are: 1) obtaining adequate electrical conductivity in the oxide/Si-nanocrystal medium and 2) constructing an ultrahigh-Q laser resonator. Because considerable talent is focused on these problems, the challenges will probably be met.

D. Ultrafast Group IV Electrooptical Modulators

Because the cubic $\underline{4}3$m lattice of the crystal Si and Ge lacks inversion symmetry, the second-order nonlinear electrooptical modulation effect—the Pockels electric-field effect—vanishes in the bulk crystal (although this effect, as well as second-harmonic generation, exists in layered SiGe superlattices and in ordered Group IV alloys [28]). The Franz–Keldysh redshift of the absorption spectrum, a third-order field effect, exists in bulk Group IV crystals. An "electric current" effect, the free-carrier plasma effect due to the electrons and holes in Group IV materials [29] has been quite successful in producing electrooptical modulation of both the real and imaginary parts of the refractive index.

The rise and fall times of index change produced by the injection of electrons and/or holes were felt to be in the nanosecond range due to the minority carrier lifetime, typically several nanoseconds. Free-carrier Shockley–Reed–Hall recombination determines the minority lifetime. Almeida *et al.* [30] showed that an optically driven SOI plasma-effect modulator, whose free-carrier lifetime was 1.4 ns, could be modulated at 20-ps rates using two-photon absorption in a highly asymmetric Mach–Zehnder inferometer. Gan and Kaertner [31] are working on a carrier-injected split-ridge waveguided modulator in double SOI. This device has a corner frequency up to 24 GHz when the minority carrier lifetime in the ridges is reduced to 10 ps by means of the ion bombardment and special doping in the intrinsic region of the p-i-n structure.

Ultrafast response times, of the order of picoseconds, can be attained in diode-waveguide devices (such as those containing a PN junction) in which an applied electric field causes a carrier-depletion region to widen or narrow. The electric field sweeps the majority carriers—and this is a fast effect. Offering a foundation to present devices, depletion modulation was discussed in a 1989 patent [32] and a 1994 paper [33]. Picoseconds response also occurs when the electric field drives carrier accumulation at a MOS gate. The pioneering 1-Gb/s modulator of Intel Corporation employed MOS accumulation of electrons and holes on the top and bottom sides, respectively, of a thin oxide film within a Si rib [34]. Later, Intel made a much-improved device with 6–10-Gb/s data transmission [35]. Simulations by Gardes *et al.* [36] indicate rise and fall times of 7 ps for their depletion device. The fastest possible device has ~3-ps response. Luxtera developed an SOI-waveguided modulator for which they report carrier-depletion modulation at 10 Gb/s [15]. They describe

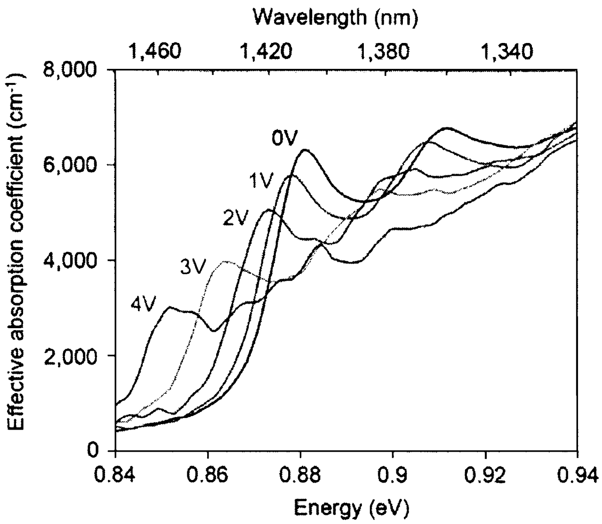

Fig. 4. Absorption coefficient spectra of the Si-based Ge/SiGe MQW at different values of applied reverse bias (reprinted from [37]).

credible ways of increasing the data rates into the 10–100-Gb/s regime.

Y.-H. Kuo and coworkers at Stanford University obtained significant experimental results on a new Si-based electroabsorption modulator that uses the quantum-confined Stark effect (a low-power electric field effect) within a stack of compressive Type-I Ge QWs separated by the tensile SiGe barriers [37]. The direct bandgap of Ge (at the Γ point of the conduction band) dominates, producing absorption with an excitonic peak at 1400 nm. As shown in Fig. 4, during reverse biasing of this ultrafast p-i-n device, the absorption spectrum shifts toward the red, giving induced absorption $\Delta\alpha = 2800$ cm^{-1} at 1438 nm for 3-V bias. It is meaningful that the 1400–1600-nm absorption due to the indirect gap at the L conduction-band valley is much weaker. Waveguided versions of this modulator appear feasible and I would suggest that QWs made of GeSn alloy would allow the peak $\Delta\alpha$ to be obtained at 1550 nm. QWs can indeed play a role in nanophotonics as envisioned in [38]. Whether quantum-confined devices will be adopted in the mass-produced OE chips depends upon whether the cost and complexity of the carefully controlled multilayers prove to be too great.

Quite recently, an MIT research group found that the ultrafast Franz–Keldysh electroabsorption modulation (EAM) effect (the bulk analog of the quantum-confined Stark effect) is quite strong in both unstrained and strained crystal Ge [39]. The refractive and absorptive figures-of-merit, $\Delta n/F$ and $\Delta\alpha/\alpha$, are impressive. This implies that the Ge-on-Si EAM may be the best EPIC modulator.

E. Direct-Bandgap SiGeSn/Ge/GeSn Heterostructure/QW Devices

The development of the GeSn alloys for photonics was pioneered by H. Atwater, Y.-H. Xie, E. Fitzgerald, and several others. In 1993 [40] and in a patent [41], I proposed that tensile-strained layers of Ge upon GeSn would have a direct bandgap, and that strain-balanced multi-QW structures made of alternating Ge and GeSn nanolayers are a basis for direct band-to-band photonic devices. J. Kouvetakis' research group at Arizona State University (ASU) has become a leader in the epitaxy of Sn-containing Group IV alloys as evidenced by the list of publications cited at http://www.public.asu.edu/%7Eyan01/, of which [42]–[44] are a few. A relaxed buffer of GeSn or SiGeSn can be grown directly upon a silicon substrate and the top surface of either "virtual substrate" is an excellent template for the subsequent growth of MQWs because there are very few defects at that surface. Regarding heterostructure band-offsets, the theory of J. Menendez shows that the band alignment is Type I between Ge QWs and GeSn barriers when the buffer is SiGeSn (but it is Type II when the buffer is GeSn). This Type I prediction has been verified experimentally [45].

A recent patent [46] shows that Si-based Ge/GeSn MQWs (or heterodiodes having four or five layers) grown upon a SiGeSn buffer layer will give direct-bandgap wells when the barrier and buffer compositions are chosen appropriately. The patent forms the conceptual basis for the 1.55-μm band-to-band laser diode project begun in 2006 at Quant Tera Corporation. Using Si-based epitaxial Ge/GeSn MQW stacks grown at ASU, Quant Tera is investigating p-i-n pumped lasers.

The invention [46] also illustrates many possibilities for direct-gap conduction-to-valence band photonic devices operating in the near- and midinfrared regions—as well as valence or conduction intersubband devices for the longer wave infrared region. The devices include laser diodes, LEDs, photodetectors, and modulators. (The intersubband devices do not require directness.) Unlike the lattice-matched GaAs/AlGaAs system, the Ge/GeSn, GeSn/SiGeSn, and GeSn/SiGeSn heterosystems tend to be coherent strain-balanced (strain symmetrized) stacks upon the SiGeSn buffer (a stable condition for stacks having hundreds of periods). Apart from strain, these direct-gap Group IV electrooptical heterostructures are expected to be analogous (in their effect) to those of InAs/InGaAs, suggesting that a "compound-semiconductor technology" is available (in effect) in Group IV. The issue or critical challenge for this technology is whether the GeSn growth reactors (and the alloy layers themselves) are compatible with a CMOS foundry.

F. Electrically Pumped Group IV Laser for 1.2–1.6 μm

A silicon-based Group IV laser diode can, by definition, contain alloys of SiGe or SiGeSn in its active region. Germanium, in particular, is an "almost-direct-bandgap material." As such, it is a good candidate for Ge-in-Si lasing. The Ge idea and related concepts have been generated recently in the silicon photonics community as ways to realize a room-temperature electrically pumped Group IV laser diode operating at, or near, the fiber-optic communications wavelengths. The recent literature contains theory and experiment related to such a laser. In that context, I would like to present here some ideas that I and my colleague S. Emelett have developed [47] to illustrate how one might go about building this 1.2–1.6-μm laser diode. We have drawn upon a number of reported experimental techniques in order to propose a highly compact Group IV laser (or an inplane 2-D array of lasers) integrated in a 3-D manner

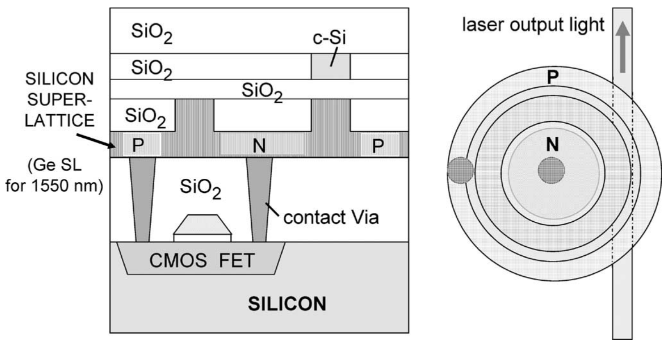

Fig. 5. Proposed Group IV laser diode showing the nanostructured p-i-n device. (a) Cross-sectional sideview. (b) Top view.

on a silicon substrate in an arrangement that links the diode directly to its CMOS drive transistor. Fig. 5 shows side and plan views of the laser. This structure uses a vertical stacking of two SOI structures, a double SOI layering that was used in 1991 for independent waveguiding in the two silicon layers [48]. In lieu of dual SOI, it is possible to use double SiGeOI [49] or double GeOI [50] to redshift the laser emission. The upper bus channel waveguide (rib or strip) that transports the laser output light to other photonic components is deposited Si or crystalline Si or SiGe; whereas the active rib-waveguided microring laser resonator consists of crystalline Si or SiGe or Ge.

The bus and ring in Fig. 5 are formed using the 3-D sculpting techniques, which are proven recently [51], [52]. The construction aspects are: a uniform $\sim$300-nm weak-coupling gap between ring and bus that preserves the ring's high Q, a self-assembled lateral superlattice [53] that penetrates the ridge and slab portions of the rib resonator (an *hcp* lattice with $\sim$60-nm pore diameter), and a lateral p-i-n diode structure for electron-and-hole injection into the intrinsic cavity under forward bias [54], [55]. The N-doped region completely surrounds the ring, while the P-doped area is a disk inside the ring—both P and N being formed on the nanoperforated slab regions. A pair of 400-nm diameter holes or vias is etched through the lowest SiO_2 layer. Those vias are filled with metal that contacts the P and N nanopored silicon above and the transistor regions below.

The device geometry includes ways to increase the optical gain, so as to overcome self-absorption by the pumped-in free carriers, as follows:

1) nanolocalized current injection [56], [57] that spreads the electron-and-hole wavefunctions in k-space thereby enhancing the radiative recombination rate;
2) ring diameter in the range of 3–5 μm that produces a large Q-to-volume ratio, thus giving Purcell-effect enhancement of optical gain—using a ring diameter not so small as to give high bend loss;
3) short-period superlattice in the Group IV resonator that gives phonon localization [58] that breaks the phonon-selection rule in the laser transition, enabling stronger radiative emission.

A similar superlattice in cryocooled silicon gave laser-like emission under optical pumping [59]. Generally, the microring geometry is attractive for lasing because the cavity can have high Q, although the mode volume will not be as small as that in a PhC resonator. Coupling to the output waveguide adds some complexity.

G. Hybrid Integration of III–V Lasers on Si

Over the next three years or so, integration of III–V laser diodes on silicon will be the cost-effective solution for on-chip light sources; however, within a five-year time frame, the IV–IV lasers discussed earlier will come onstream and may become the preferred on-chip emitters—provided that those IV–IV lasers are sufficiently efficient and fast. Adequate efficiency and speed in IV–IV diodes are likely because those lasers can be embodied in the nanophotonic form discussed in Section IV-I. For now, let us take a quick look at the III–V approaches.

The competing hybrid-integration approaches include bonding of the III–V device wafer to the Si wafer [60], [61], III–V die to Si-chip bonding, and heteroepitaxy of III–V materials directly upon Si or SiGe [62]. At this time, it is not clear which technique is best because experimental trials are needed to determine the "most manufacturable" method. When that has been done, the laser's cost can be traded off against its electrooptical performance. I think the laser with the lowest cost will win.

H. Active Microresonator Devices

There is an ongoing push toward reducing the "footprint" of silicon photonic components, thereby affording a larger scale of on-chip integration. Silicon microresonators, whether in PhCs or in conventional waveguides, contribute to this miniaturization trend. The resonators are versatile because they can form the basis of a laser, a light emitter (like the Er structures described above), a photodetector, a modulator, or a spatial routing switch. Rings can be racetrack-shaped as well as circular. The rings offer excellent narrow-band spectral filtering whose passband can be shaped by thermooptic (TO) tuning sections. Rings can be coupled to Mach–Zehnder interferometers for advanced filtering.

High-performance modulation and switching is provided by devices in which the real and imaginary indices of the resonator(s) are altered by means of the TO effect on $\sim$100-ns time scale [63] or by injection, depletion, or accumulation of free carriers on a subnanoseconds scale. The active microring modulator has been pioneered by Michal Lipson's group at Cornell [54]. Andrew Poon tested a laterally injected 20-μm diameter p-i-n microdisk in SOI, and obtained 0.4 nm of blueshift for 1-V forward bias [55]. Unique and important progress was made by Luxtera, who obtained 10-Gb/s intensity modulation via depletion of the carriers in an SOI microring [[15], Fig. 10].

Stephen Emelett and I have made extensive studies of waveguided 1×1 modulators and 2×2 spatial routing photonic switches that use a pair of coupled high-Q microring resonators, typically in SOI [64]–[67]. We described the novel fixed-ring and floating-ring devices. These double-ring switches are readily interconnected to make the planar monolithic matrix switches illustrated in Figs. 6 and 7—devices that have not yet been built. The floating rings are found in Fig. 6. Generally, the two-ring structures provide higher performance than do single-ring

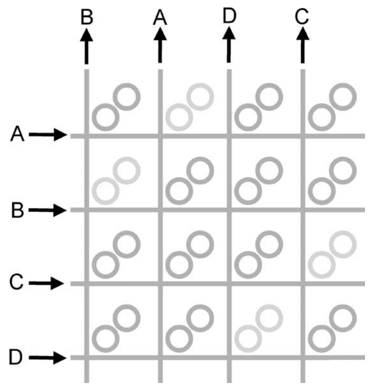

Fig. 6. Layout of proposed waveguided $N \times N$ cross-connect spatial switch utilizing active SOI microrings in a planar PIC.

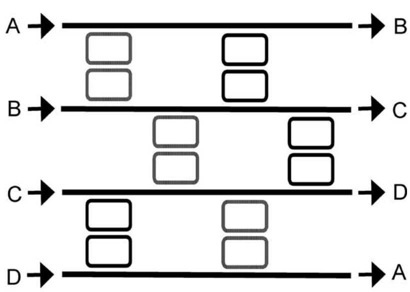

Fig. 7. Layout of proposed waveguided $N \times N$ permutation-matrix spatial switch utilizing active SOI microrings in a planar PIC.

structures. The principal findings are that the depth of the 1×1 intensity modulation is linear with respect to the real index shift Δn (induced in the rings) over four decades of Δn, and that the 2×2 switch is expected to give complete switching at $\Delta n \sim 2 \times 10^{-3}$ with low optical crosstalk, low optical insertion loss, and low electrical control power. The drawback is that the laser wavelength must coincide with the resonator-mode wavelength (the initial-bias wavelength), or that the resonator-mode wavelength must be trimmed via TO bias or polymer loading to match the laser wavelength.

I. PhC Devices

During the past five years, silicon PhC structures have become a special part of the silicon photonics technology. An extensive PhC literature has sprung up on both theory and experiment, and useful one-dimensional (1-D), 2-D, and 3-D silicon PhCs have been reported. PhCs can be engineered to yield devices with unique properties, such as negative-refraction lenses, superprisms, self-collimated waveguides, sharp waveguide bends, all-optical buffer memories, dynamic dispersion compensators, and nanoscale 3-D point-defect resonators that provide high Q and high concentration of the optical fields. The uniqueness adds value to a PIC. In an experimental PIC, conventional Si strip (or rib) waveguides have been joined smoothly to the "unconventional" PhC line-defect waveguides.

Active devices are feasible too. For example, Altair Center LLC in cooperation with the University of Rochester is currently investigating a silicon-based PhC laser diode wherein a PhC microcavity forms the laser's gain region. Modulators have also been studied. By means of PhC "dispersion engineering," a carrier-injected PhC line-defect waveguide can be designed for the reduced group velocity ("slow light") that, in a recent experiment [68], produced a 33× reduction in the π-radian active length L_π as compared to the L_π of a conventional waveguide. Vlasov's group at IBM attained a 300-fold reduction in group velocity in the Si PhC line-defect waveguides [69]. Their waveguides were made in a CMOS facility. Jacobsen *et al.* [70] show that an SOI PhC line-defect waveguide, when strained by Si_3N_4 or SiO_2, will possess a Pockel's electrooptic field effect having 830-pm/V susceptibility at $\lambda = 1561.5$ nm.

These results suggest that the PhC devices can be a part of the high-performance chip-scale PICs and OEICs in future. The viability of the PhC contribution will depend, in part, on whether the PhC waveguide losses can be kept acceptably low. Evidence for low propagation loss was obtained with a suspended silicon PhC membrane (clad below and above by air) that contains the waveguides [63], [69]. Nanophotonic devices hold the key to chip-to-chip and intrachip interconnects because the energy per bit processed must be less than 100 fJ, which implies a very small mode volume in each active device. For such interconnects, I would suggest the use of PhC components because they exemplify "true nanophotonics." Lipson and coworkers describe an SOI strip waveguide that contains a 1-D PhC resonator. They show that a mode volume of $\sim 0.1\ (\lambda/2n)^3$ is obtained by etching a thin mode-confining slot between the two PhC reflectors. I believe that active SiGe material can be deposited in this slot to create the "smallest possible" p-i-n lasers, modulators, and photodetectors.

J. Plasmon Optics

Silicon-based plasmonic components are discussed elsewhere in this special issue. Metal-containing plasmon optics are indeed nanophotonics. The subwavelength dimensions of these devices support a "Moore's Law for Photonics"—the progressive development of increasingly smaller components. Currently, scientists from California Institute of Technology, Stanford, Harvard, UCLA, and UCSD are researching "Novel devices for plasmonic and nanophotonic networks" described at www.plasmonmuri.caltech.edu/research/index.html. The objective is "to enable nanophotonic components for communications and imaging systems by exploiting localized and propagating surface plasmons that access *nanometer-scale wavelengths at optical frequencies*." They say that "plasmon optics will open a new domain for integrated photonics based on: (1) extreme light localization—nonlinear excitations in ultrasmall volumes—compact, low-power optical devices, (2) very high spatial frequencies—an opportunity for optical imaging systems with nanometer-scale resolution, (3) enhanced light emission from active photonic devices via coupling to surface plasmons, (4) coupling from dielectric (*fiber and SOI waveguide-based*) photonics to plasmonic devices." The last point illustrates a new and promising linkage between microphotonics, PhC devices, and plasmon-optic structures. Confined light on the chip can flow efficiently between a Si ridge, a plasmonic guide, and a PhC guide in any sequence. A fiber-accessible plasmon waveguide in a Si membrane has already been tested [71]. Active plasmonic devices such as electrooptic waveguided modulators are at the frontier of research.

K. The Long-Wave Infrared (LWIR) Paradigm for Silicon Integrated Photonics

There are opportunities for sensing, communications, signal processing, missile detection, tracking, and imaging in the "wide infrared," especially in the 3–5- and 8–14-μm windows, in a band near 20 μm, and in the 30–100-μm "terahertz" range. Silicon photonics will "enable" these applications. I am suggesting [72] that appropriately designed Si-based PICs and OEICs can operate at a wavelength anywhere from 1.2 to 100 μm. Noteworthy progress has already been made on long-wave Si-based photodetectors, modulators, and light emitters [9], [10]—results that will facilitate the migration of "active" integrated photonic networks to the long-wave regions. Additional reasons for migration are given in [72].

A significant R&D challenge is to find Si waveguides with low propagation loss over the wide infrared or portions thereof. I have investigated the low-loss possibilities and have proposed several waveguide types [72], whose infrared coverage is as follows: the suspended silicon rib-membrane for 1.2–6.0 and 24–100 μm, the germanium rib on silicon for 1.9–14 μm, and the Si-based air-filled hollow-core channel waveguide for 1.2–100 μm. The hollow-core of the silicon "cylinder" is clad by GeSi/Si Bragg reflectors or antiresonant reflectors. An issue for the LWIR OEIC chips is whether they will require cryogenic cooling for proper operation. This challenge arises mainly at wavelengths beyond 10 μm.

L. Nonlinear Optical (NLO) Devices

Third-order NLO effects in silicon (and in Group IV generally) are relatively strong. These include resonant and nonresonant effects. The prominent effects are the Franz–Keldysh shift, Kerr effect, stimulated Raman scattering, coherent anti-Stokes Raman scattering, two-photon absorption (which is often deleterious to Raman lasing), and the intensity-dependent refractive index [73], [74]. Another NLO effect, four-wave mixing [75], is important for "all-optical" silicon applications. For example, Hochberg *et al.* [76] intensity-modulated a light beam at terahertz rates within a 120 nm $\times$ 500 nm SOI strip waveguide clad with NLO polymer.

The locally strained Si (and I propose SiGe) waveguided devices in [70] appear to be a breakthrough. Here, a new lattice is born due to a nonuniform spatial distortion of the diamond lattice. A challenge for the future is to bring these devices into the "nonlinear mainstream." The question is whether foundry-built strained devices can be exploited for second-order effects such as Pockels modulation or sum-and-difference frequency generation.

A few years ago, the idea of "all-optical logic" was floated. Now there is a reason to think that "electrooptical logic" may be more practical, and a recent paper describes how an active silicon PIC can be built for that purpose [74]. The concept in the paper is that binary electrical control signals will operate upon two incoming optical data streams A and B in order to perform any 1 of 16 possible Boolean logic operations on A and B. (The optical streams A and B are at the same wavelength and are phase-coherent with each other.) It is proposed that each resonant "logic gate" be realized with interconnected p-i-n SOI waveguided microring resonators. Nonresonant silicon logic uses electrooptical waveguided interferometers. This EO logic has specialized applications and is not aimed at large-scale computing.

V. Future Prospects

The future cannot be predicted: one can only make educated guesses about it. Instead of trying to foresee radical events (there will be some), I shall simply make a few extrapolations of the present trends. I will assume that many of the challenges raised in Sections IV-A–IV-J have been met, and I shall present the resulting "scenarios."

Within a five-year time frame, it is likely that we will see the following:

1) true OE integration on CMOS in a stable 130-nm or 90-nm commercial process;
2) hundreds of photonic components and more than a million transistors on a monolithic OE chip;
3) cost-effective fiber-optic links using Si OE transceivers exchanging data at 10–100 Gb/s;
4) fast, cost-effective optical interconnection of computer chips;
5) integrated Ge-on-Si photodiodes as the 1.55 μm detectors-of-choice in PICs and OEICs;
6) a room-temperature electrically pumped Ge/Si laser;
7) a well-developed Ge/GeSn technology—both MQWs and heterodiodes—that includes 1.55-μm band-to-band laser diodes, LEDs, modulators, and photodetectors;
8) silicon laser diodes that rely upon Erbium ions or PbS nanocrystals;
9) integration of silicon PhC devices into high-performance silicon photonic circuits;
10) development of practical Si-based Group IV components for the wide infrared spectrum stretching beyond 1.6 μm out to 100 μm—components such as emitters, quantum-cascade lasers, detectors, and modulators;
11) ultrasmall, nanophotonic Ge-in-Si p-i-n lasers, modulators, and detectors;
12) Si-based photonic devices utilizing Group IV quantum dots or QWs.

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