Large-Scale Photonic Integrated Circuits

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***Abstract*-We present an overview of Infinera's current generation of 100 Gb/s transmitter and receiver PICs as well as results from the next-generation 500 Gb/s PM-QPSK PICs.**

I. Introduction

Photonic integration has made significant progress over the last few decades. In this article we will provide an overview of Infinera's large-scale photonic integrated circuits. The current generation of Infinera products is using 100 Gb/s transmitter and receiver PICs using on-off keyed (OOK) modulation format. In order to provide higher fiber transmission capacity, the next generation of optical systems will use polarization-multiplexed quadrature phase-shift keyed (PM-QPSK) modulation format. This modulation format requires a significantly larger amount of optical components per wavelength than conventional OOK solutions, and is ideally suited to photonic integration. Results of the 500 Gb/s PM-QPSK PICs that were developed at Infinera will be presented.

II. 100 Gb/s Photonic Integrated Circuits

A. Architecture of the PICs

The architecture of the monolithic InP-based 100 Gb/s transmitter PIC is shown in Fig. 1. The device has 10 channels, and each channel operates at an aggregate data rate of 10 Gb/s on a 200 GHz ITU wavelength grid in the C-band. The active train of each monolithically integrated channel includes a tunable distributed feedback (DFB) laser, a 10 Gb/s electroabsorption modulator (EAM), a semiconductor optical amplifier (SOA), and two optical power monitor (OPM) photodiodes. Each individual channel is subsequently multiplexed into a single output channel via a monolithically integrated arrayed waveguide grating (AWG) in the passive section of the chip. The single output waveguide is terminated in a spot size converter for optimized fiber coupling in the package.

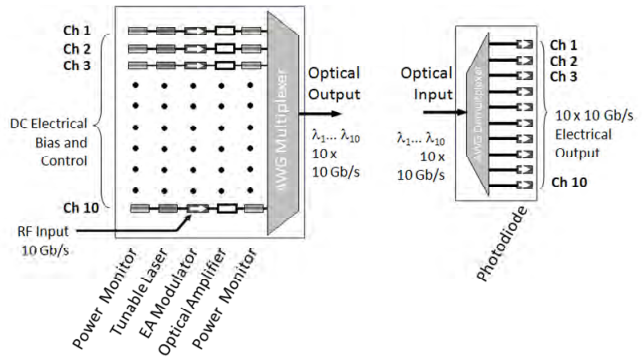

Figure 1. Schematic diagrams of the 100 Gb/s transmitter and receiver PIC architectures.

The 100 Gb/s receiver PIC consists of a single optical input channel / spot-size converter routed through a waveguide to a polarization independent demultiplexing AWG in the passive section of the chip. The AWG filter functions are aligned on a 200 GHz ITU wavelength grid in the C-band. Ten high-speed (>10 Gb/s) PIN photodiodes (PDs) are monolithically integrated into the waveguides at the output of each AWG arm resulting in a 10 channel x 10 Gb/s receive PIC.

B. Performance of the PICs

Some performance metrics of the 100 Gb/s TxPIC and RxPIC are shown in Figs. 2 and 3. Fig. 2 shows the spectral performance of the TxPIC. Side-mode suppression ratio of >45dB can be seen. The DFB laser linewidth was measured as

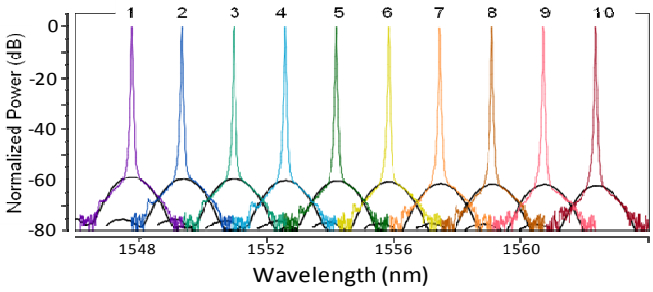

Figure 2. TxPIC spectral output.

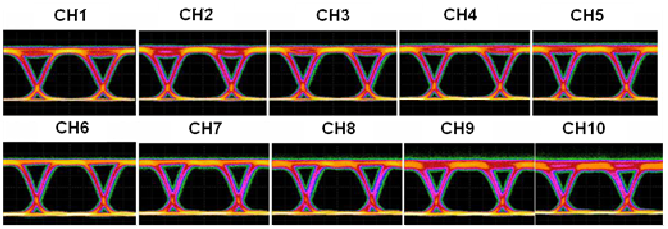

Figure 3. TxPIC output eye diagrams.

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4 MHz using a self-heterodyne technique. Superimposed over the DFB spectra is shown the AWG spectral transmission response. In Fig. 3 the eye diagrams for all channels of a TxPIC is shown. The eye diagrams have uniform open eyes and the extinction ratio is >13dB. More performance data of the 100 Gb/s PICs can be found in [1,2] and references therein.

III. Next Generation 500 Gb/s Photonic Integrated Circuits

A. Architecture of the PICs

A schematic of the 500 Gb/s transmitter PIC for PM-QPSK modulation is shown in Fig. 4. The device has 10 channels, each of which has a tunable DFB laser, a splitter for the second polarization, and one nested Mach-Zehnder modulator per polarization. All light is maintained in the TE polarization on the chip until it is rotated and combined externally with a polarization rotator and beam combiner. The twenty optical data signals are combined into 10:1 AWG multiplexers (one per polarization) and routed to the output facet.

The coherent 500 Gb/s PM-QPSK receiver PIC receives fiber coupled signals with one polarization rotated such that both inputs are launched into the chip in the TE orientation. There is an input TE polarizer on both paths to strip any remaining TM components. The V and H signal components

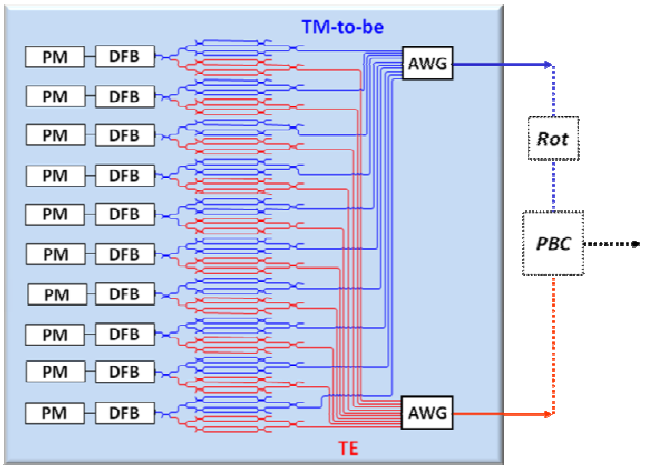

Figure 4. Schematic diagram of the 500 Gb/s PM-QPSK transmitter PIC.

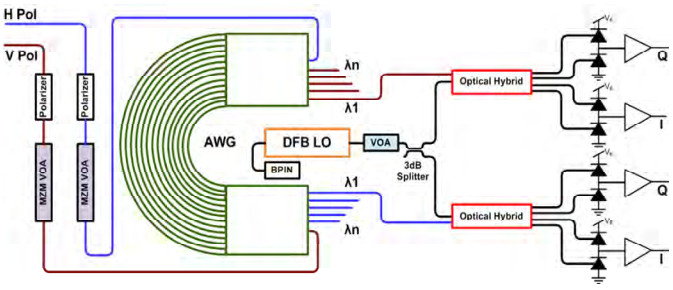

Figure 5. Schematic diagram of the 500 Gb/s PM-QPSK receiver PIC.

are then wavelength demultiplexed using a single AWG. Each of the demultiplexed outputs is then mixed with one of ten local oscillators (LOs) using a 90º optical hybrid. The LO's are tunable DFB lasers monolithically integrated and tuned to the incoming signal frequencies. The mixed outputs of the optical hybrid are fed to high speed, balanced photodetector pairs with 3dB bandwidths of >25 GHz. A schematic diagram is shown in Fig. 5.

B. Performance of the PICs

Fig. 6 shows the performance of one channel of a PIC-to-PIC transmission using coherent 500 Gb/s PM-QPSK transmitter and receiver PICs over 1300 km of LEAF fiber. The testbed consists of 16 spans of fiber with an 80 km average spacing between hybrid Raman/EDFA optical amplifiers. The input data consists of two delayed PRBS $2^{15} - 1$ patterns to achieve pseudo-random quaternary sequence (PRQS) symbol states. A 50 Gs/s high-speed real-time oscilloscope and Infinera proprietary signal processing are utilized to capture the constellation diagrams. The error rate for this transmission is below the requisite FEC correctable limit. More performance data of the 500 Gb/s PICs can be found in [2,3].

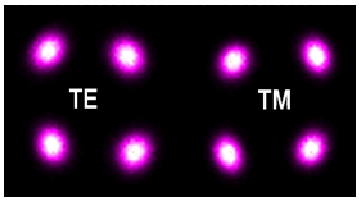

Figure 6. Constellation diagram for one-channel received transmission of a 500 Gb/s PM-QPSK transmitter PIC to a 500 Gb/s PM-QPSK receiver PIC over 1300km of LEAF fiber.

IV. Summary

We have demonstrated 100 Gb/s InP large-scale photonic integrated circuits with performance, capability, and economics sufficient for commercial deployment. Furthermore, next generation devices with capacities of 500 Gb/s per chip have been developed, monolithically integrating over 400 optical elements.

Acknowledgment

We would like to thank all of the Infinera employees who have contributed to the success of the company's large-scale InP PICs and PIC-based products.

References

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