北京邮电大学研究生课程

数字超大规模集成电路分析与设计

第三讲 互连线模型

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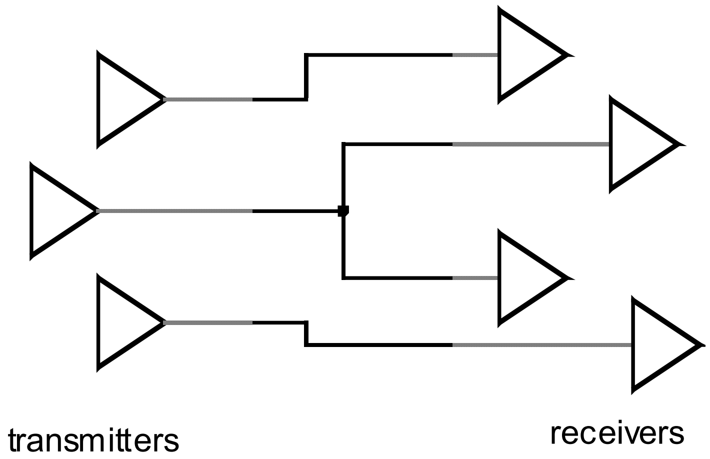
本讲主要内容

- （一）电阻、电容和电感
- （二）互连模型

2.1 电阻、电容和电感

□ 导线



schematics

physical

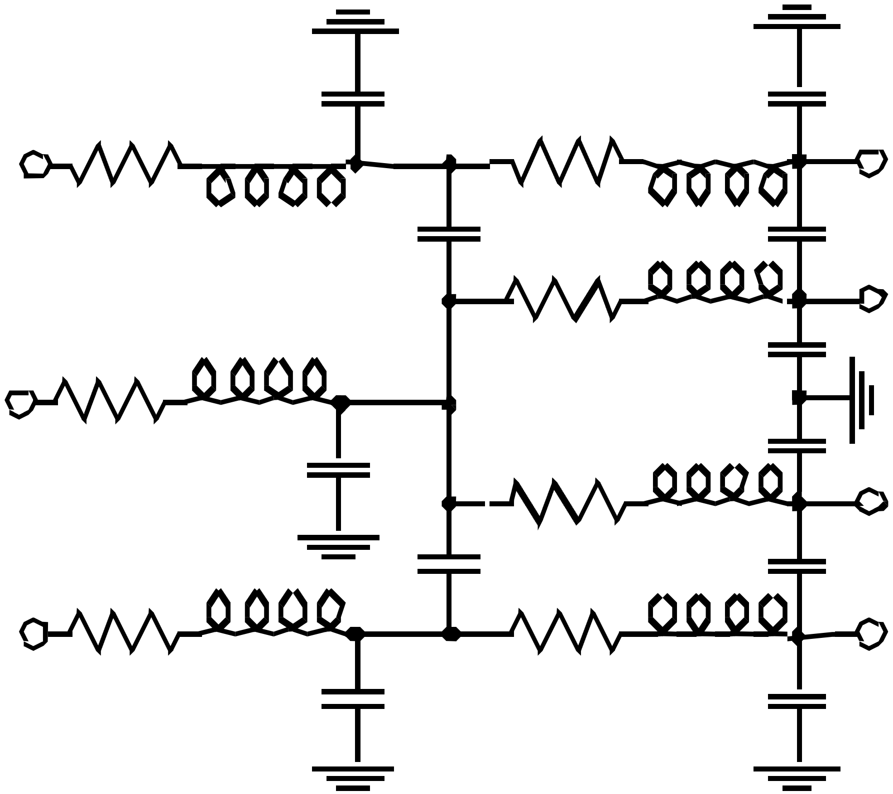
2.2 电阻、电容和电感

☐ 导线模型

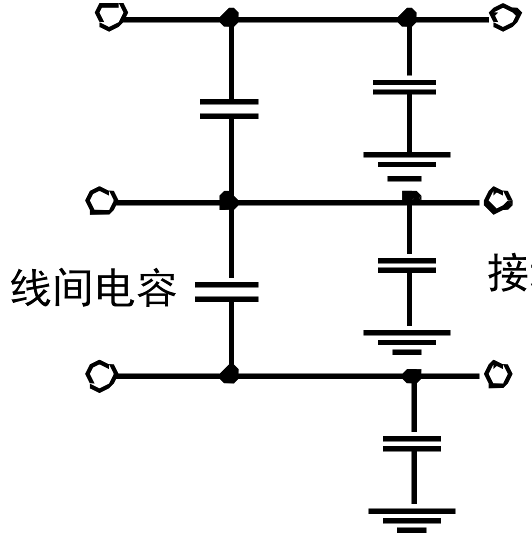
忽略电感的电容模型

当导线的电阻很大或者外加信号的上升或下降时间很慢

当导线很短、导线的截面很大或互连材料电阻率很低



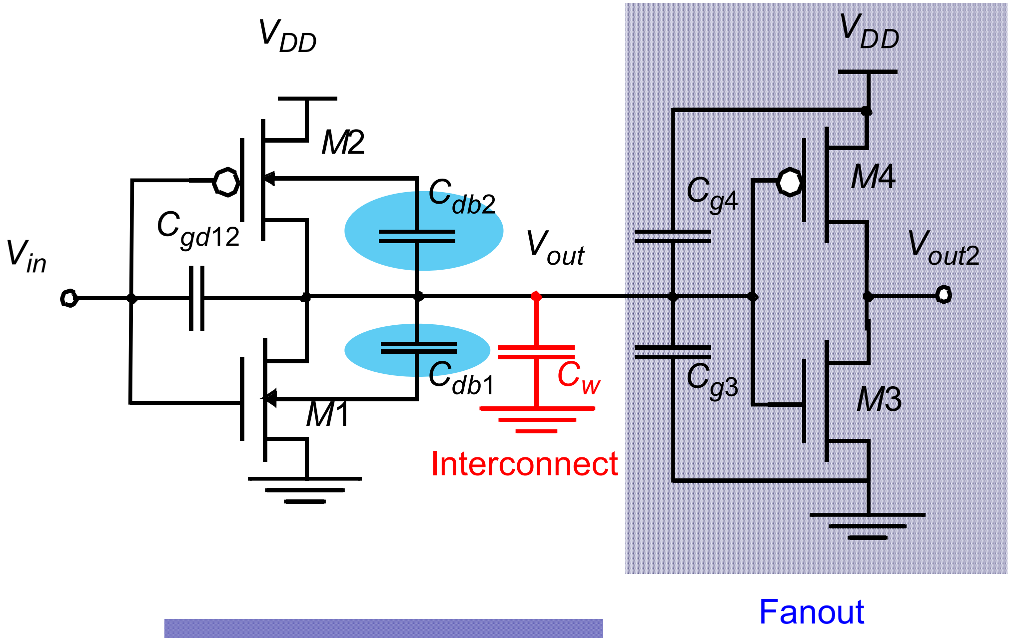
All-inclusive model



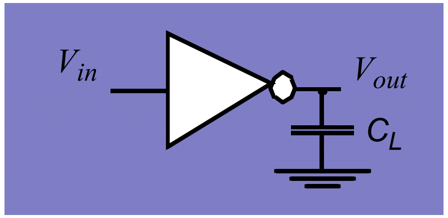
Capacitance-only

2.3 电阻、电容和电感

□ 连线电容



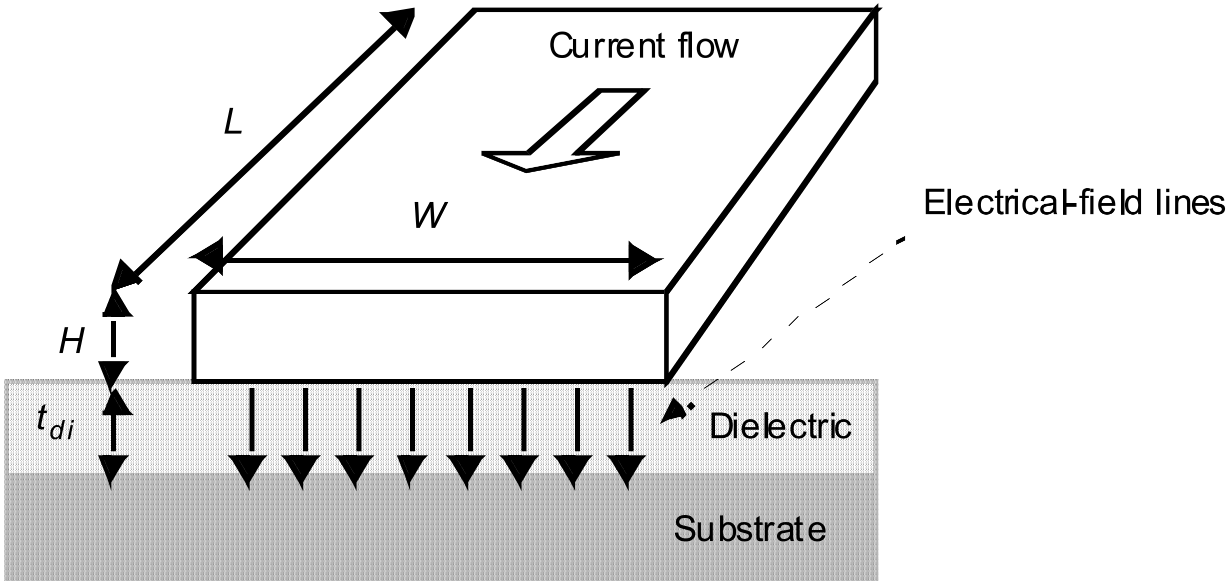
Simplified Model



$C_L = ?$

2.4 电阻、电容和电感

平板电容模型



$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

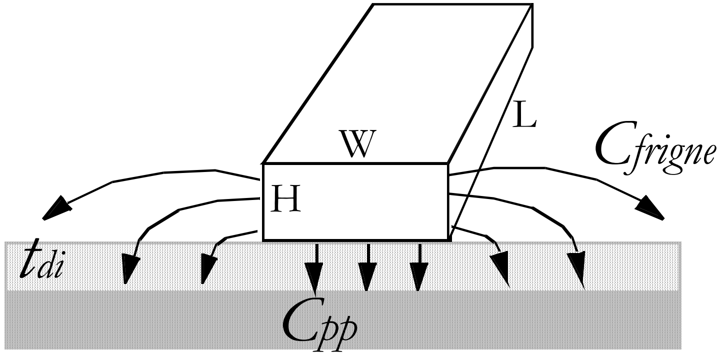
2.5 电阻、电容和电感

□ 各种材料的相对介电常数

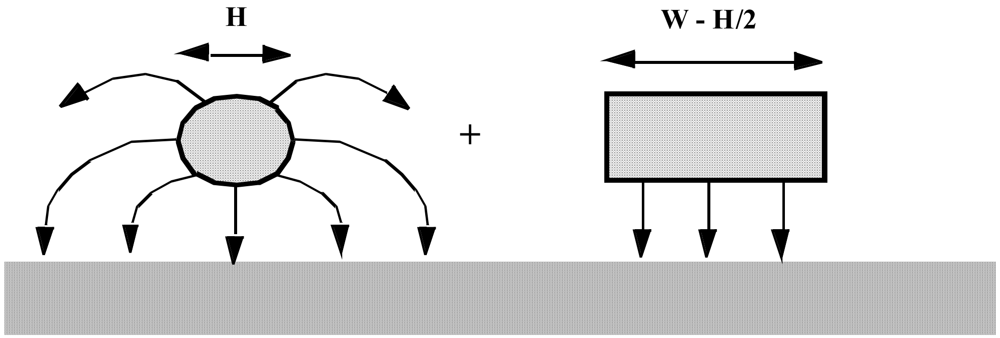
Material	ε_r	
Free space	1	
Aerogels	~1.5	气凝胶
Polyimides (organic)	3-4	有机聚合物
Silicon dioxide	3.9	
Glass-epoxy (PC board)	5	
Silicon Nitride (Si_3N_4)	7.5	
Alumina (package)	9.5	
Silicon	11.7	

2.6 电阻、电容和电感

□ 边缘电容



(a)



(b)

近似计算

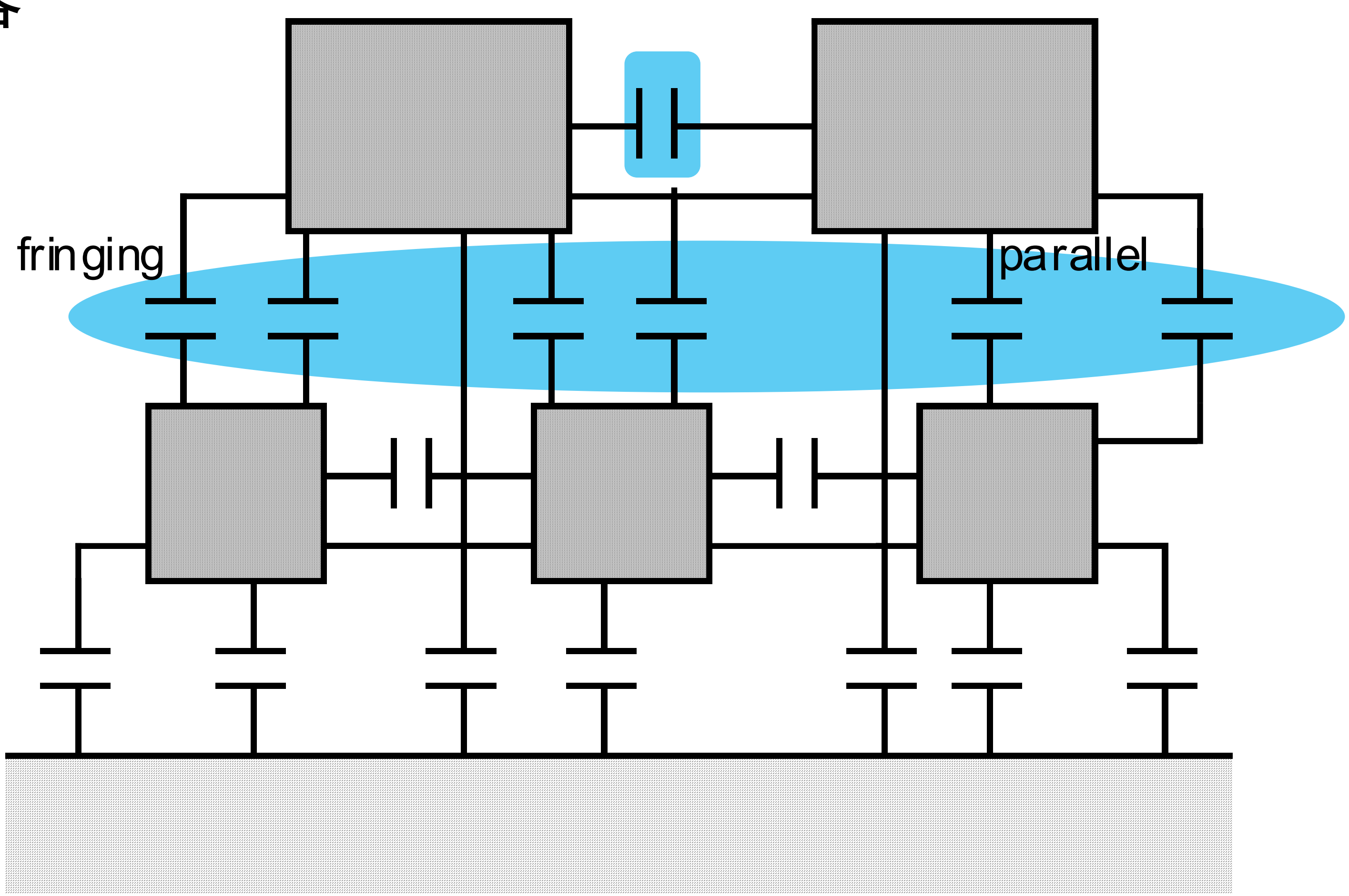
$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

互连线宽度

对于较大的W/H值，总电容接近平板电容模型
当W/H小于1.5时，边缘电容变成了主要部分

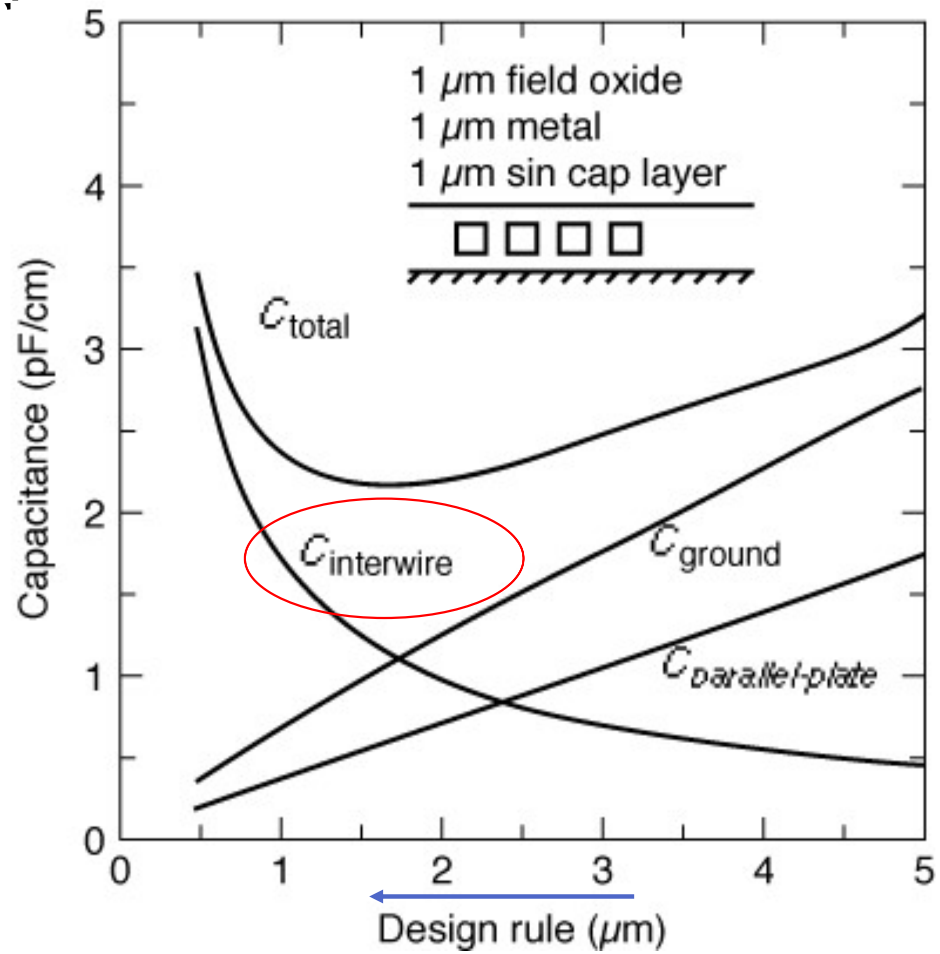
2.7 电阻、电容和电感

- 线间的电容



2.8 电阻、电容和电感

□ 线间电容的影响



2.9 电阻、电容和电感

□ 电容举例（0.25um CMOS工艺）

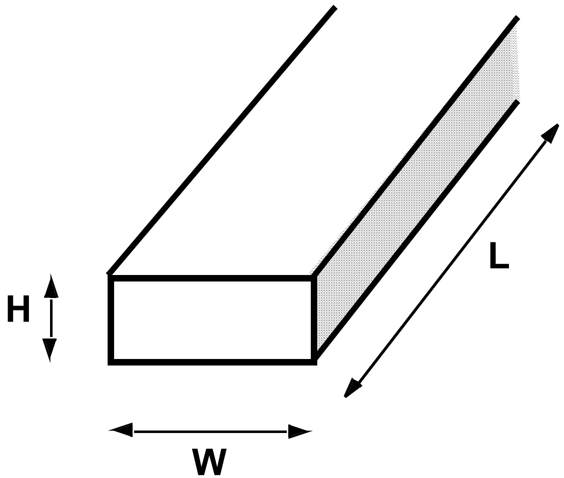
平板电容aF/um2 边缘电容aF/um

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

阴影栏部分为边缘电容

2.10 电阻、电容和电感

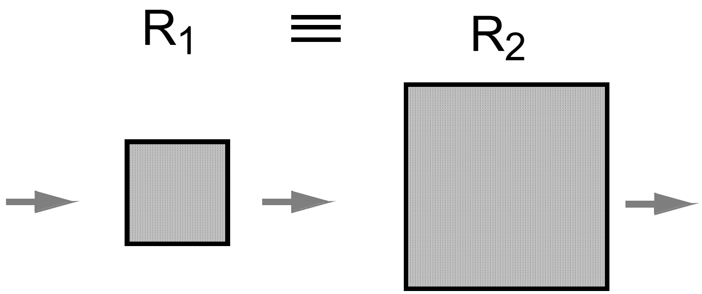
□ 导线电阻



$$R = \frac{\rho L}{H W}$$

Sheet Resistance R_o

方块电阻或薄层电阻（对于给定的工艺）



2.11 电阻、电容和电感

- 互连的电阻率（20摄氏度）

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

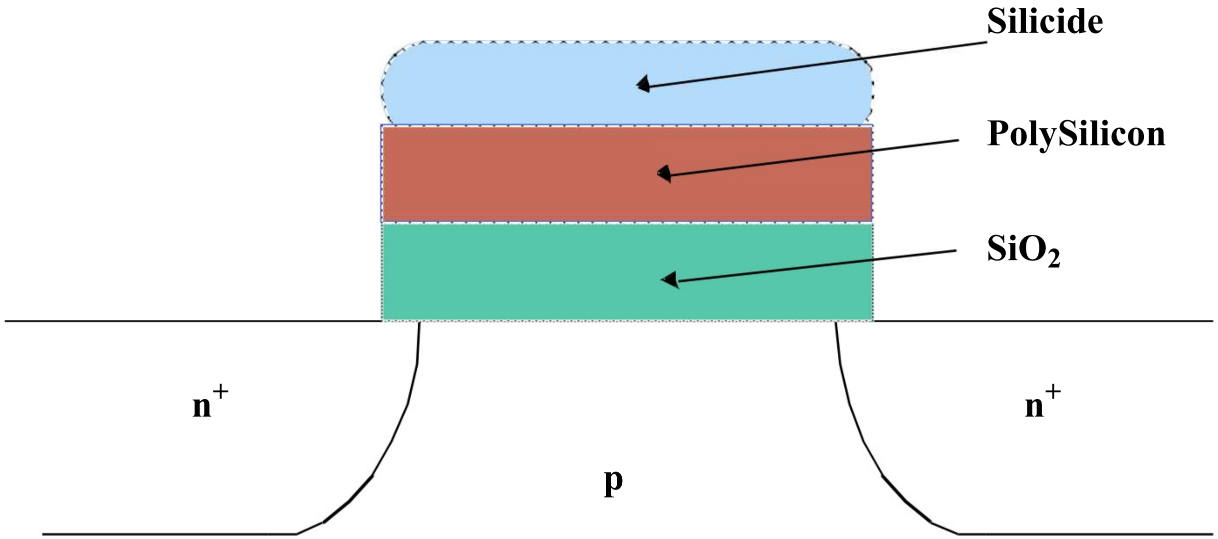
2.12 电阻、电容和电感

- 如何减小电阻？
  - 线长
  - 电导率

2.12 电阻、电容和电感

□ 硅化物栅（先进工艺）

- 硅化物是用硅和一种难熔金属形成的合成材料，具有高导电性且耐受高温工艺步骤而不会融化。



Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly

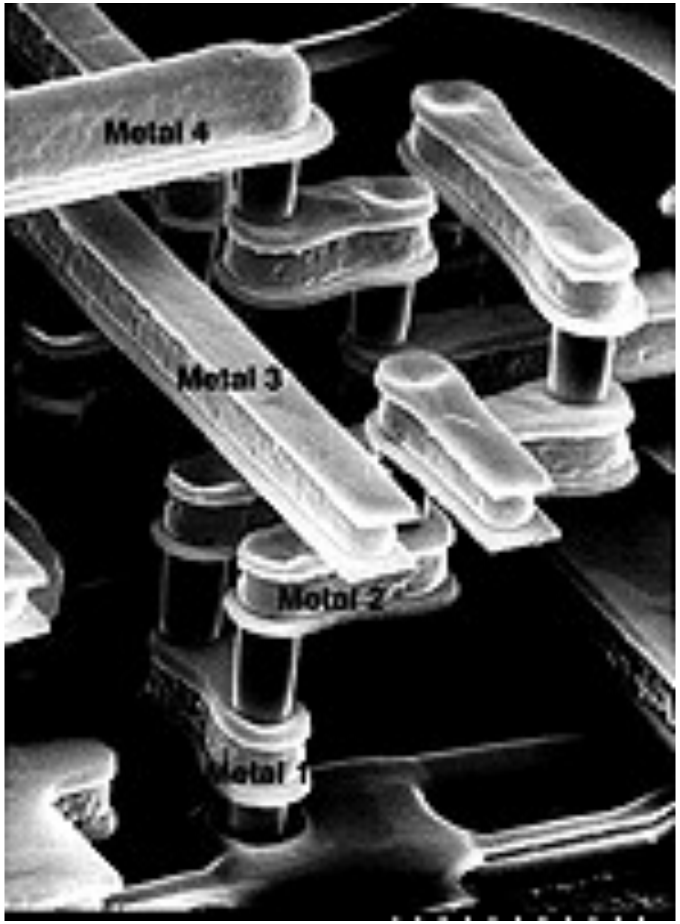
2.13 电阻、电容和电感

□ 方块电阻（薄层电阻）

Material	Sheet Resistance (Ω/□)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

2.14 电阻、电容和电感

- 互连举例



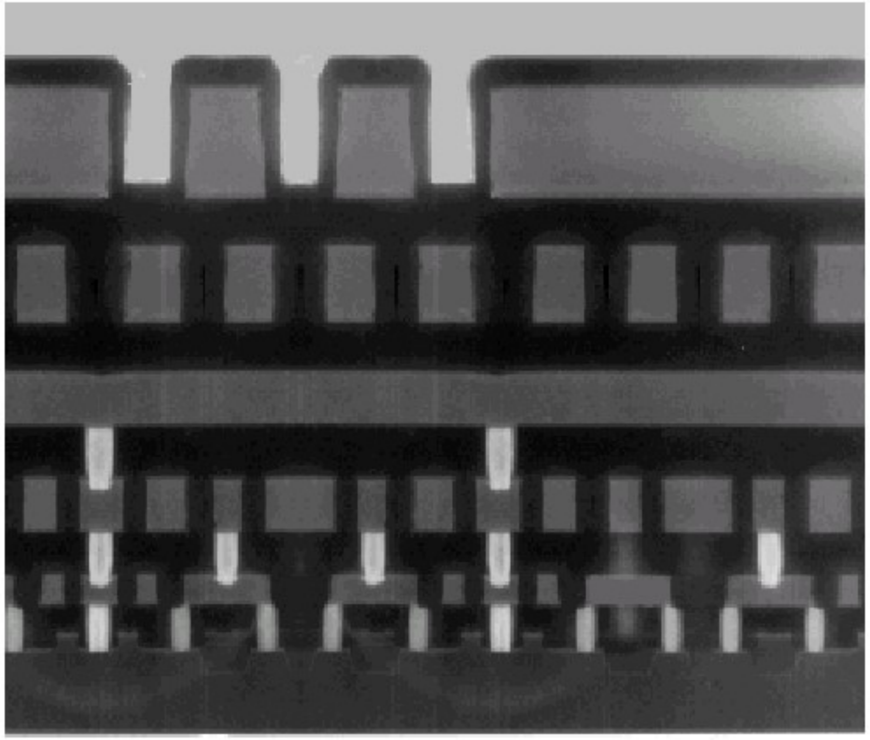
2.15 电阻、电容和电感

0.25um工艺举例

5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio

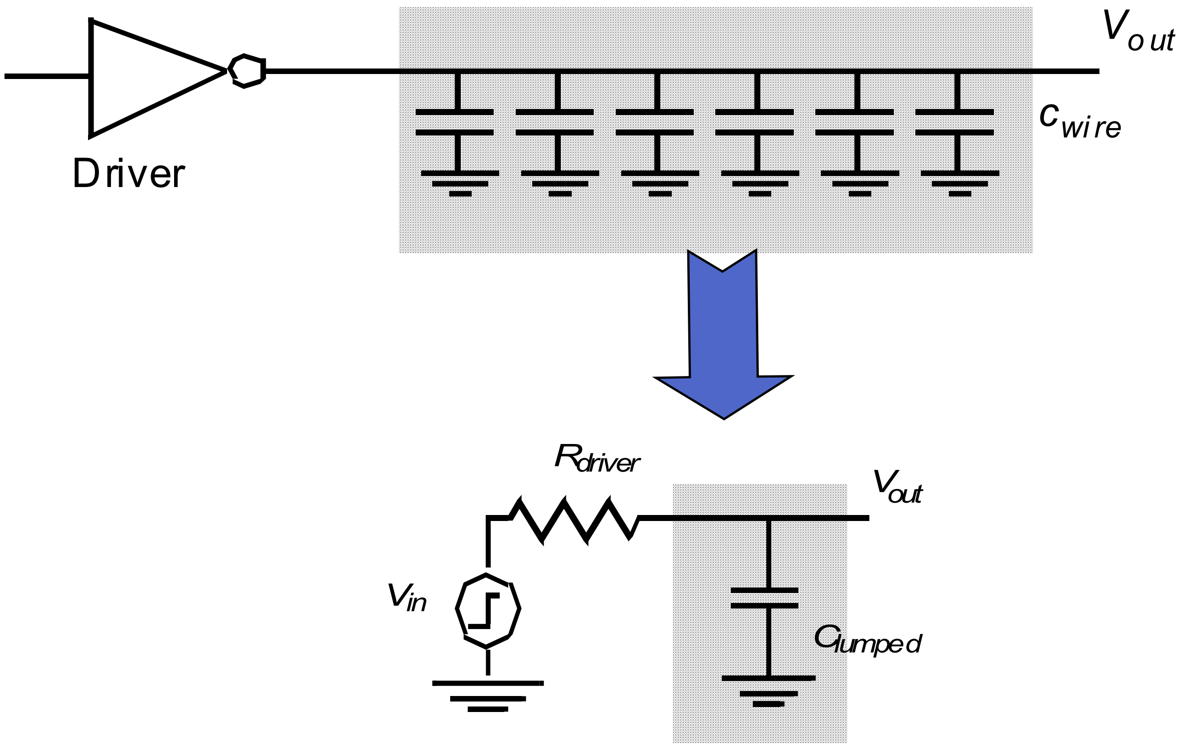


本讲主要内容

- □ （一）电阻、电容和电感
- □ （二）互连模型

2.1 互连模型

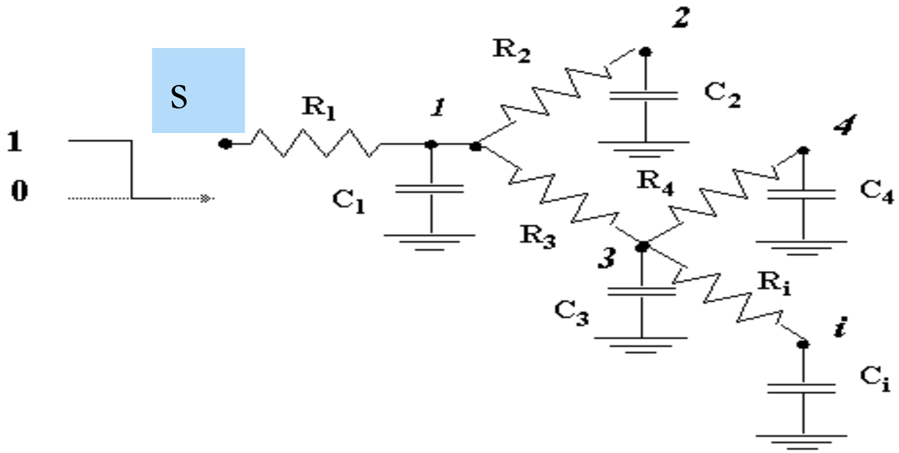
- **集总模型（The Lumped Model）**
  - 导线电阻部分很小且开关频率在低到中间范围，分布电容可以集总为单个电容



2.2 互连模型

□ 集总RC模型（The Lumped RC-Model ）

- 长度超过几毫米的片上金属具有明显电阻
- Elmore延时（The Elmore Delay）

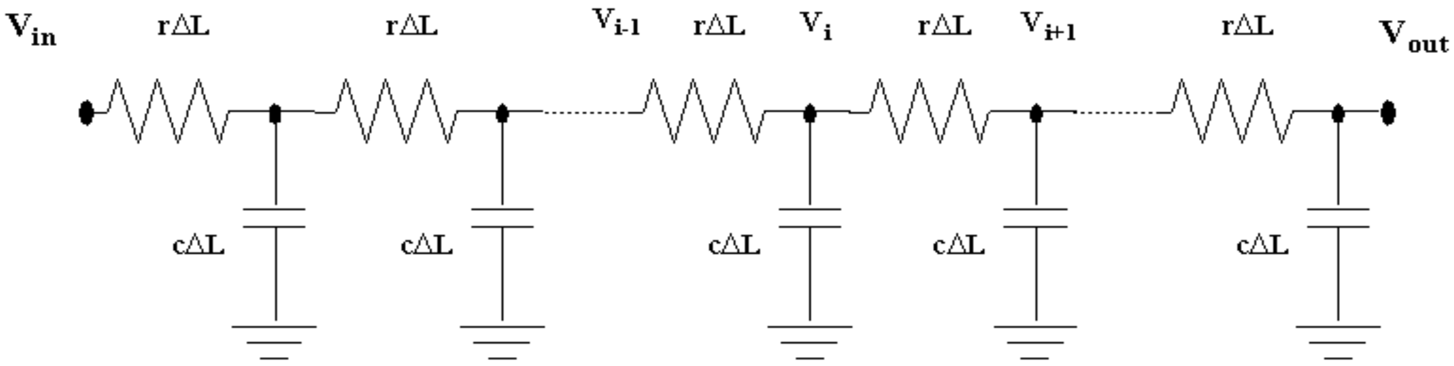


$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

2.3 互连模型

☐ The Elmore Delay RC Chain



$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

2.4 互连模型

☐ Wire Model

- Assume: Wire modeled by N equal-length segments

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

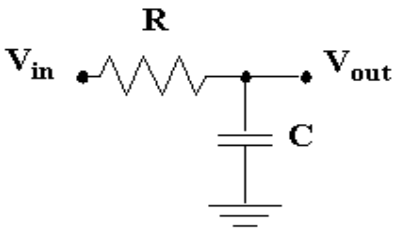
For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

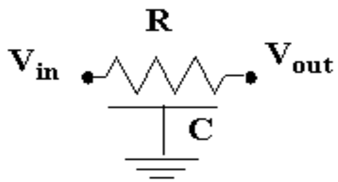
导线的延时是长度的二次函数

2.5 互连模型

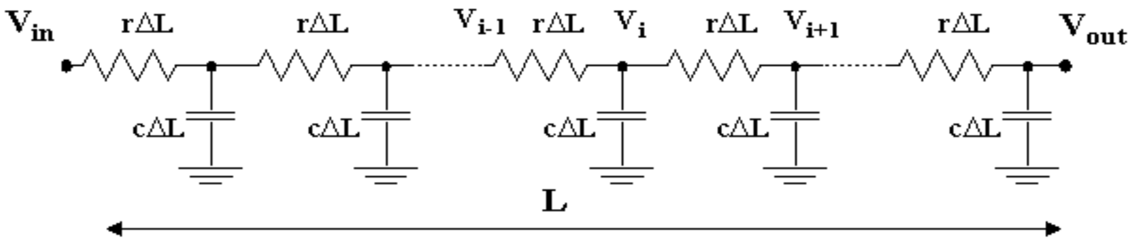
□ 分布式RC线



(a)



(c)



(b)

$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

扩散方程

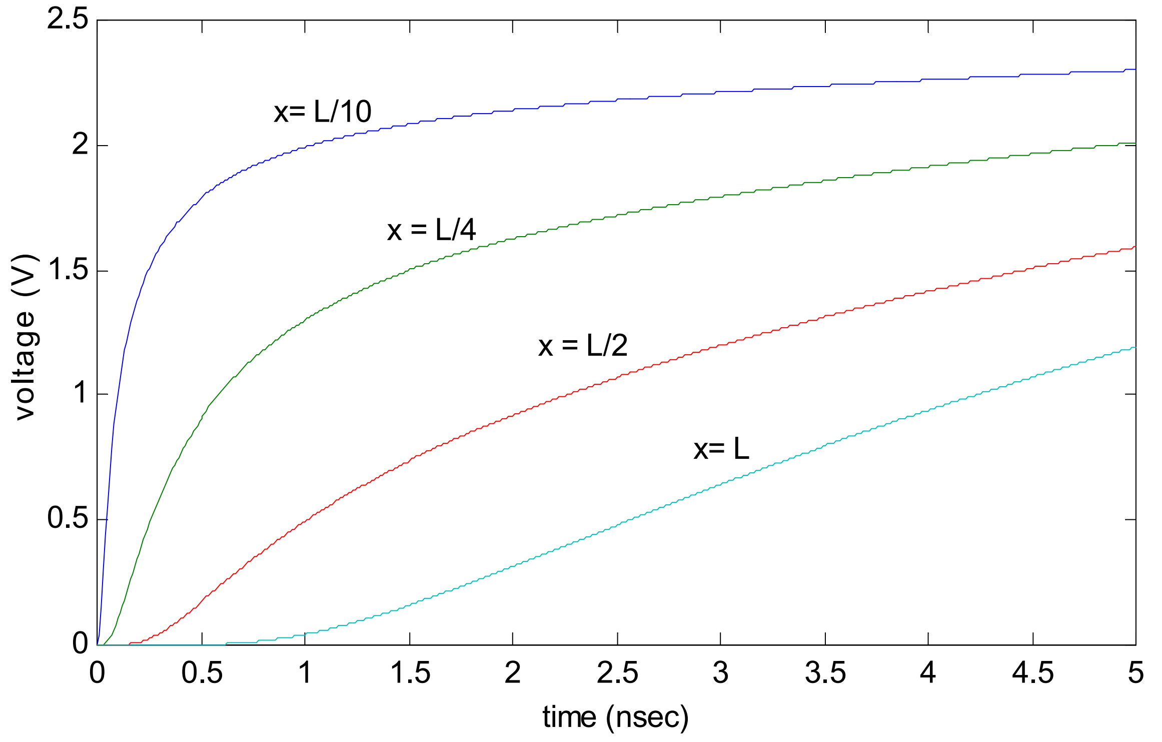
不存在收敛解

$$\tau(V_{out}) = \frac{rc\,L^2}{2}$$

可用集总RC梯形网络近似

2.6 互连模型

□ 电阻-电容导线的阶跃响应



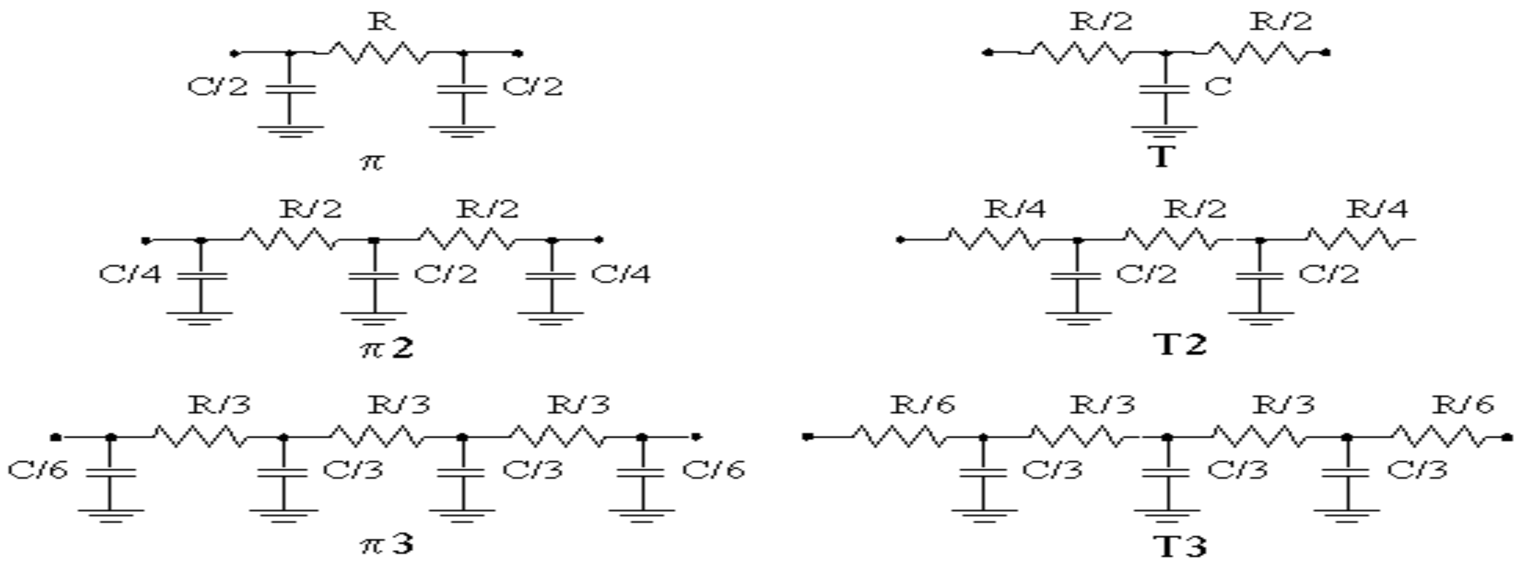
Step-response of RC wire as a function of time and space

2.7 互连模型

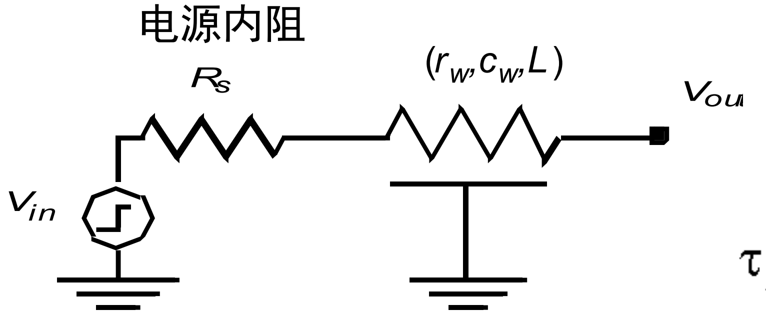
□ RC模型

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

$$Rw = rL$$
$$Cw = cL$$

2.9 互连模型

- 设计经验规则

  - rc delays should only be considered when $t_{pRC} >> t_{pgate}$ of the driving gate

    $$L_{crit} >> \sqrt{t_{pgate}/0.38rc}$$ 临界长度

  - rc delays should only be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

    $$t_{rise} < RC$$

    - when not met, the change in the signal is slower than the propagation delay of the wire

讨论

- 树状网络的延迟？

谢谢！

欢迎指正！