EDA Tool Tutorial

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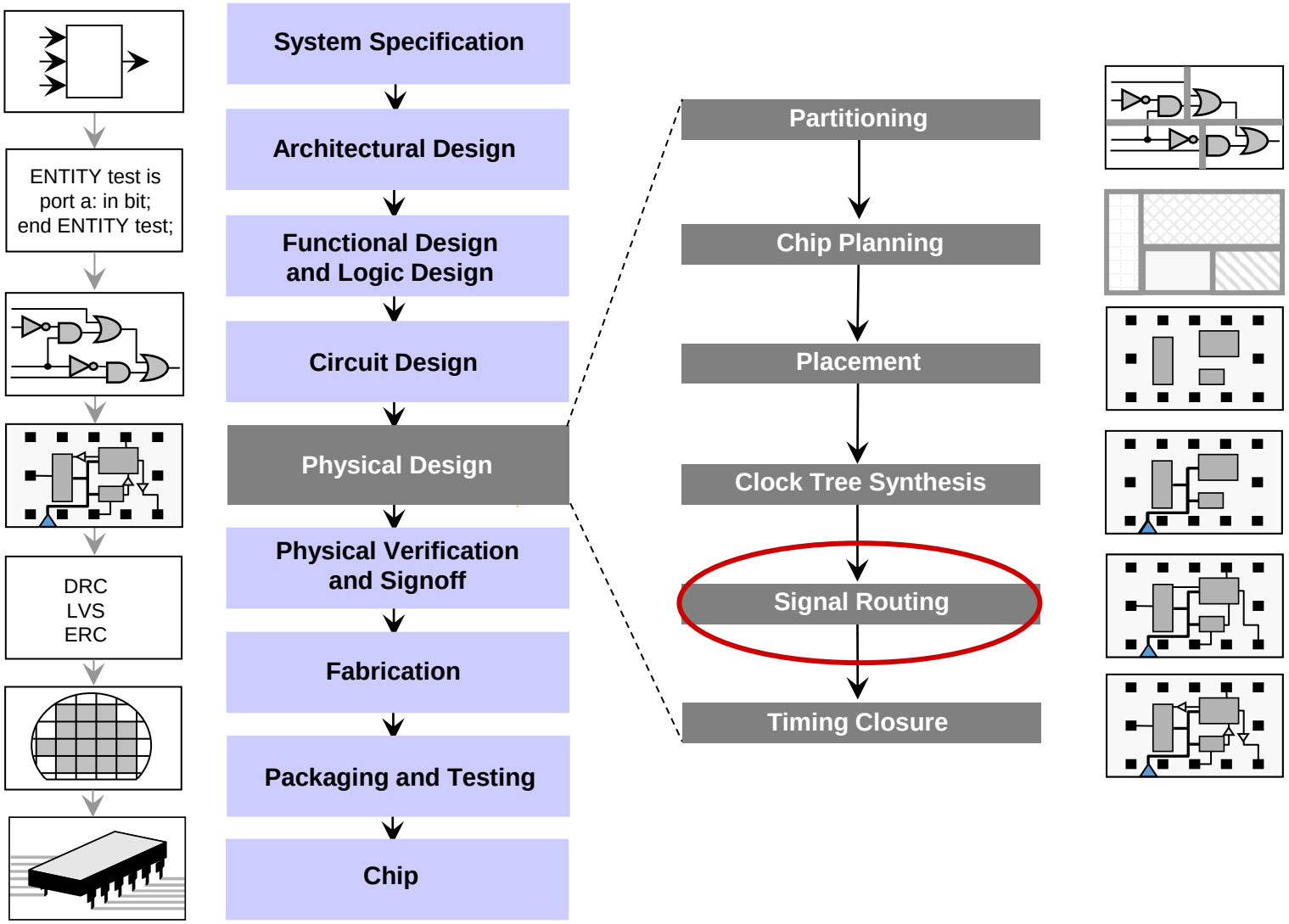
Outline

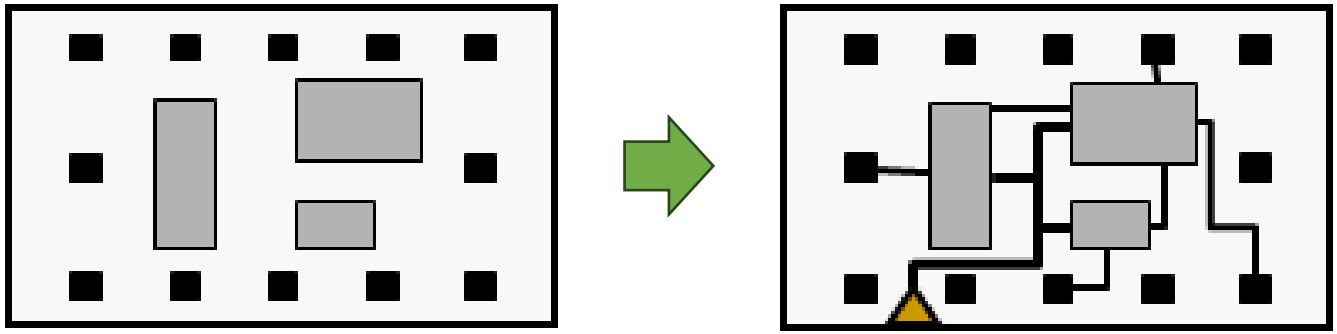
Introduction



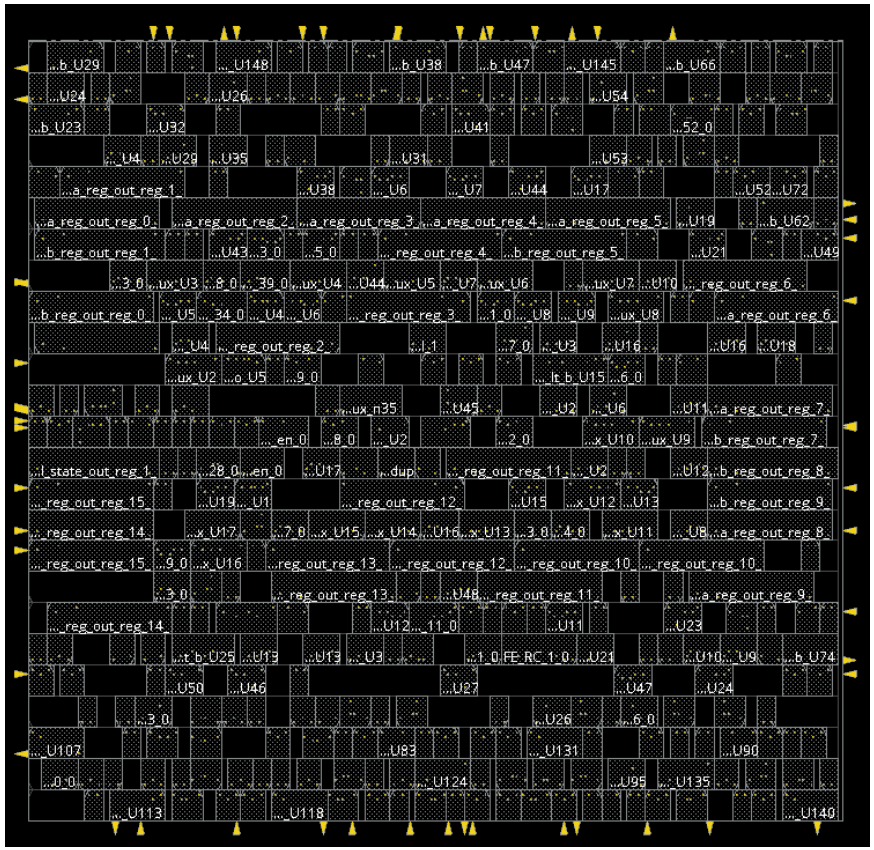
Introduction

Given a placement, a netlist and technology information,

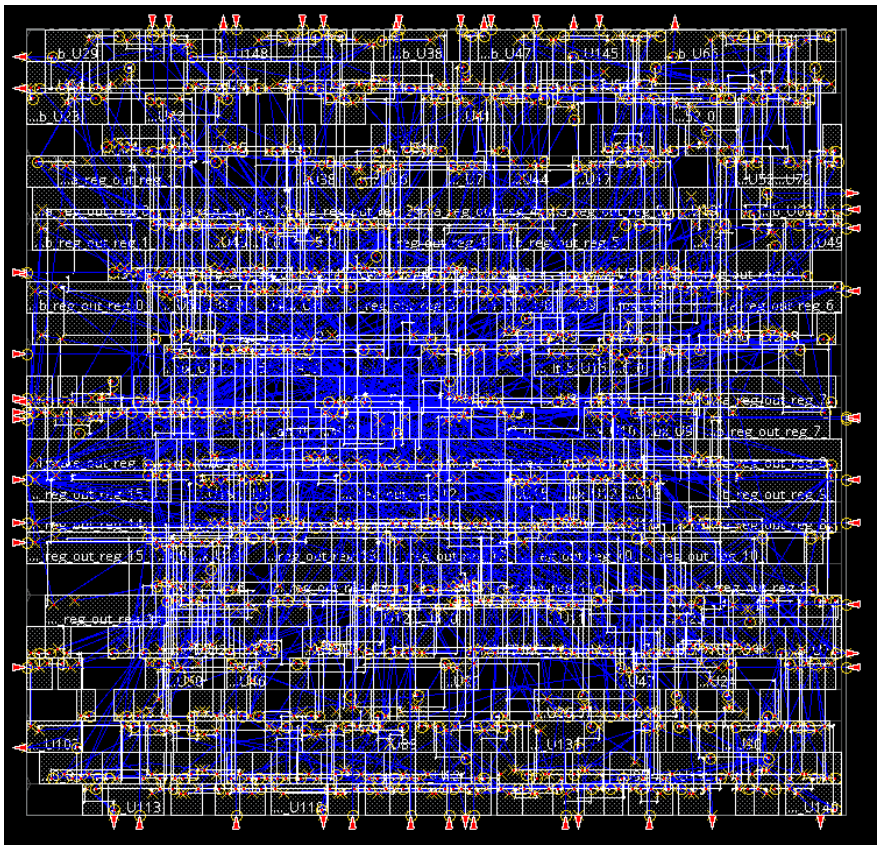
- determine the necessary wiring, e.g., net topologies and specific ro uting segments, to connect these cells
- while respecting constraints, e.g., design rules and routing resource capacities, and
- optimizing routing objectives, e.g., minimizing total wirelength and maximizing timing slack.



Introduction

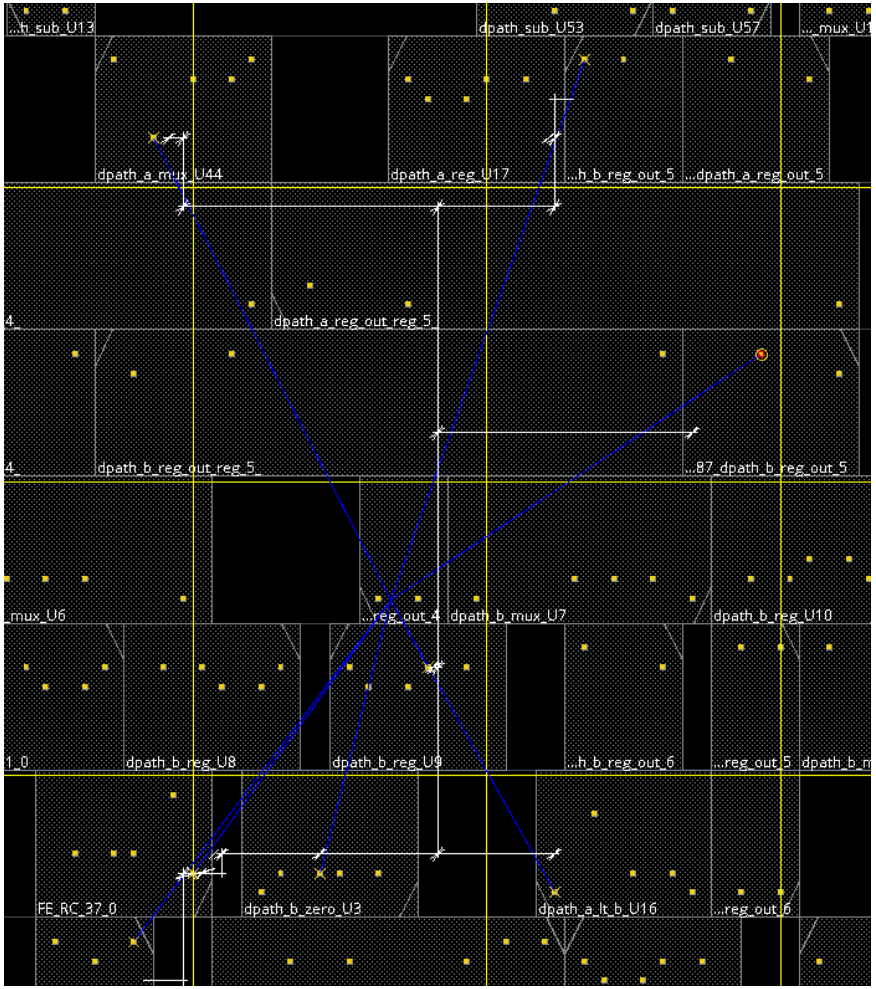


Placement

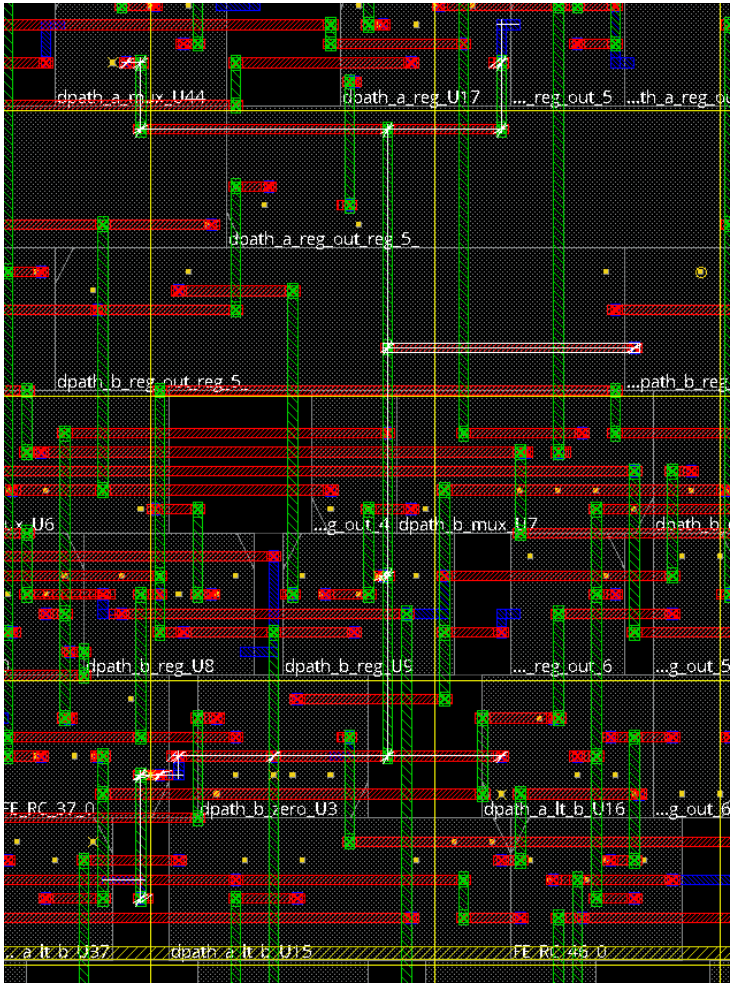


Nets

Global & Detailed Routing

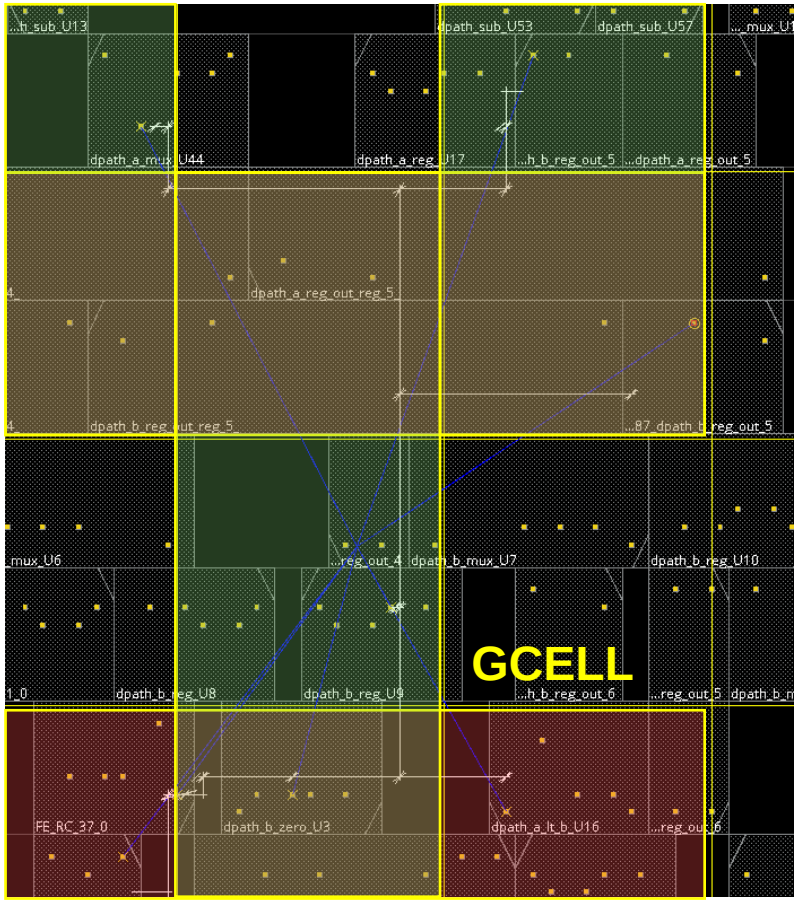


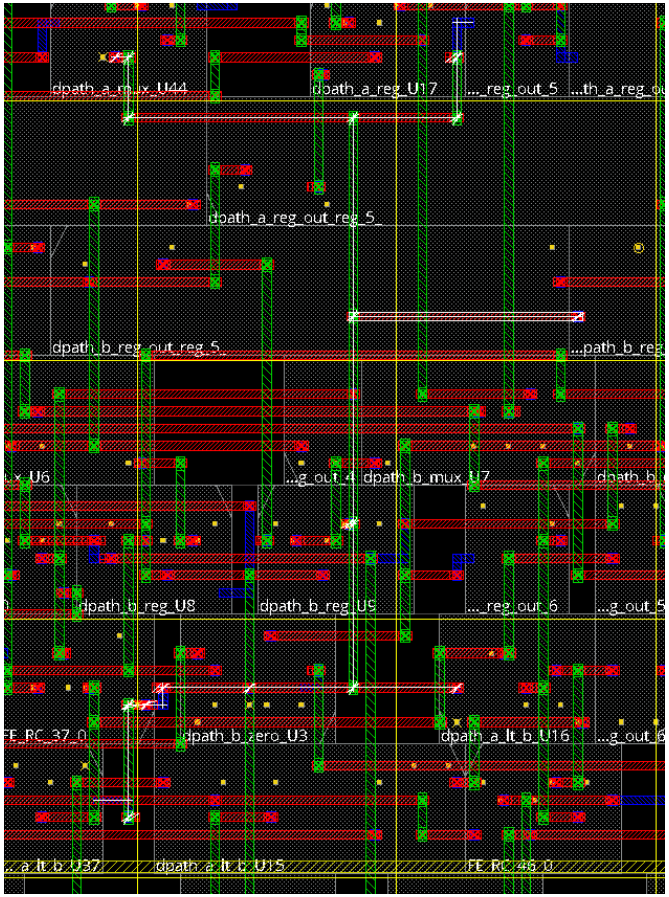
A net to be connected



Post-route

Global & Detailed Routing





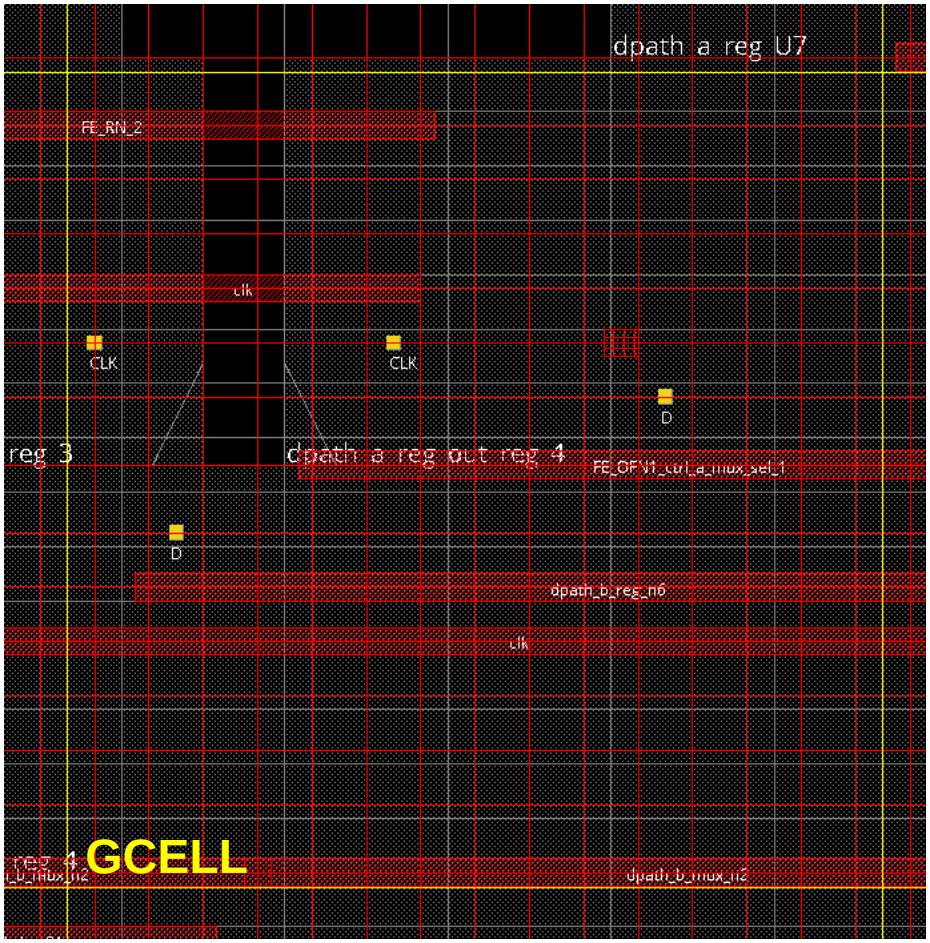
Global Routing

- Partitions the routing region into global routing cells (gcells)
- Plans routes as sequences of gcells
- Minimizes total length of routes and, possibly, routed congestio
  n

Detailed Routing

- Seeks to implement each global route as a sequence of track segments

Terminology

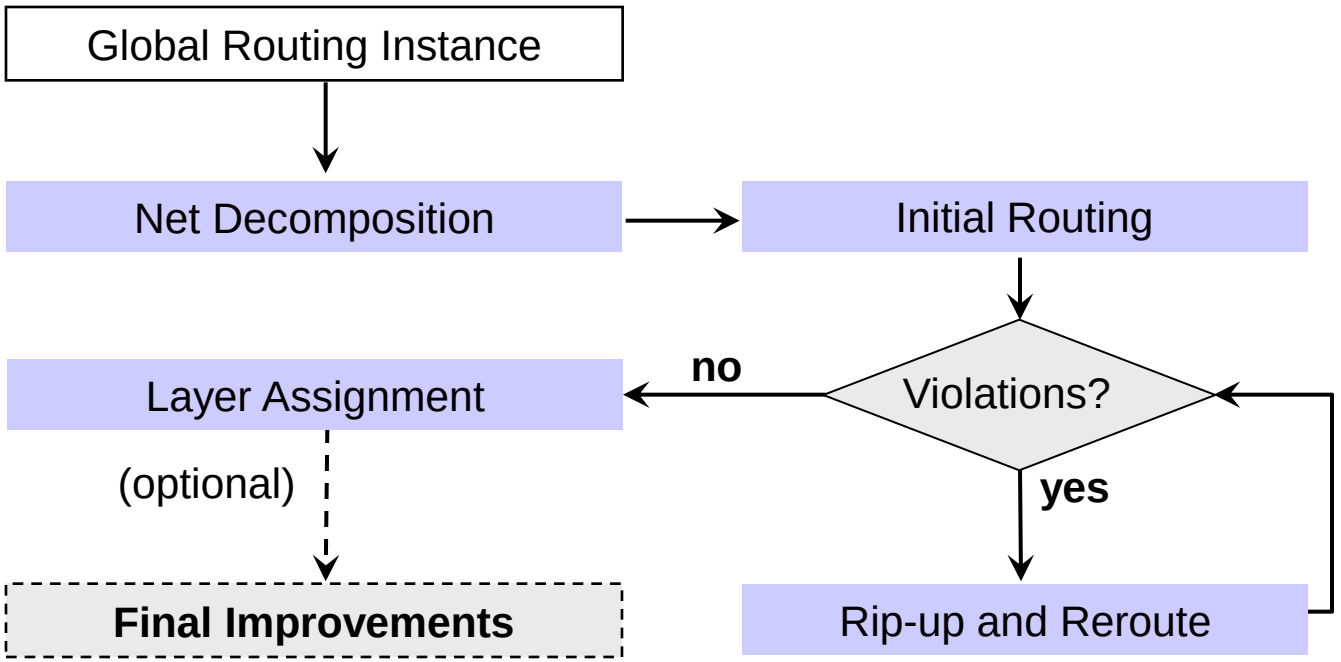


Track(M2 Layer)

Track(M3 Layer)

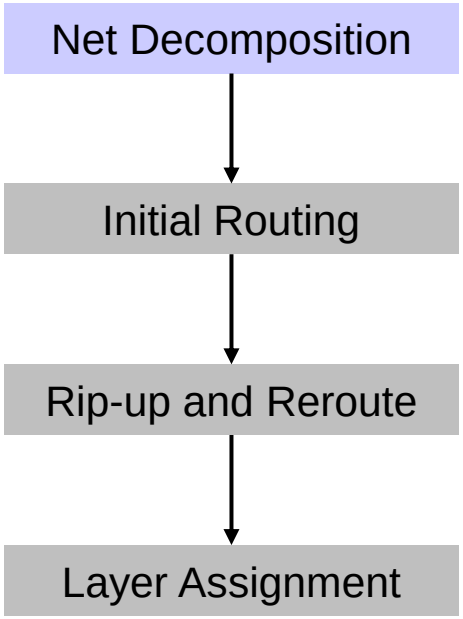
Flow for Modern Global Routers

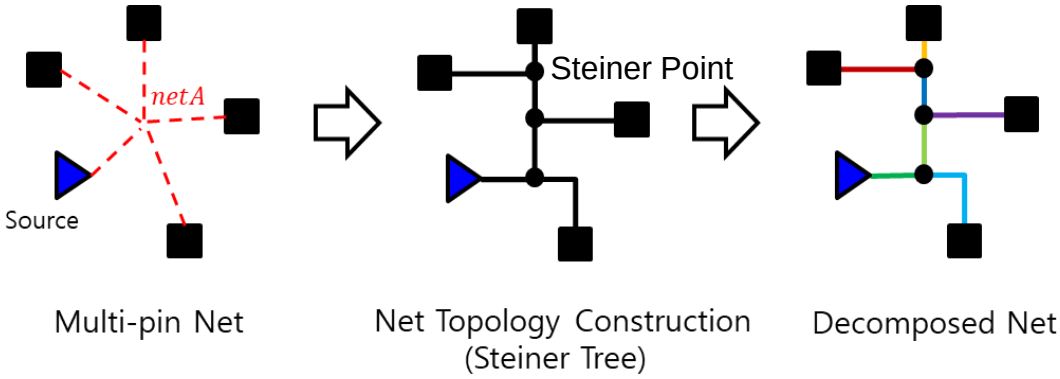
- **General flow for modern global routers, where each router uses a unique set of optimizations:**



* Reference: VLSI Physical Design: From Graph Partitioning to Timing Closure

Net Decomposition



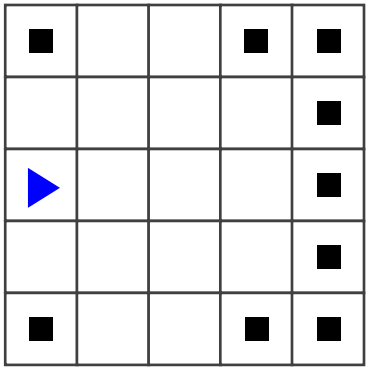


Net Topology – Background

▶ Source ■ Sink ■ Critical sink

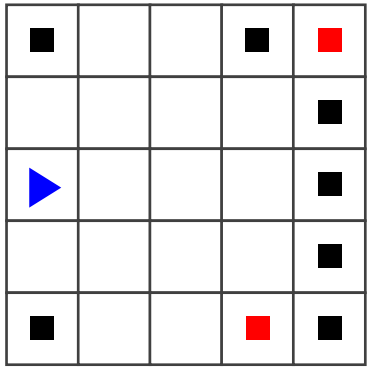
Pins on grid

Case 1



Net with non-critical pins

Case 2



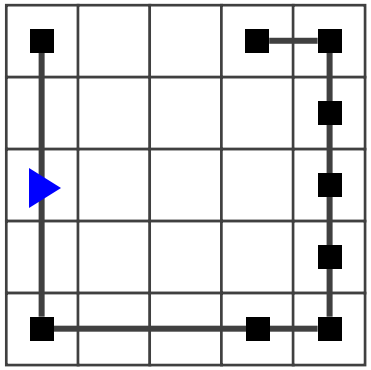
Net with critical pins

Net Topology – Background

▶ Source ■ Sink ■ Critical sink

RSMT*

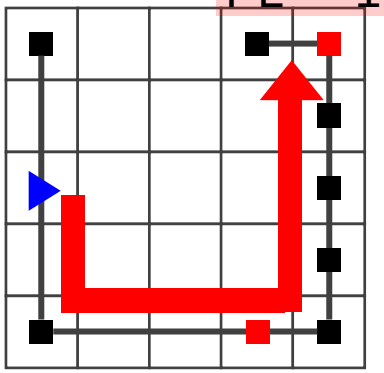
Case 1



WL=13

Minimal WL

Case 2



WL=13

Long PL to critical pin
→ Timing violation

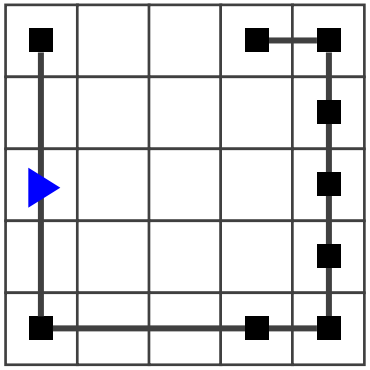
* Rectilinear Steiner Minimum Tree: **FLUTE(2008)**, REST(2021)

Net Topology – Motivation

▶ Source ■ Sink ■ Critical sink

Proposed

Case 1

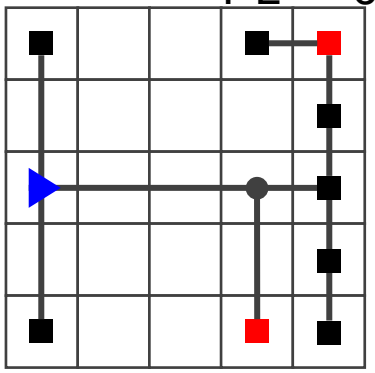


WL=13

Minimal WL

Case 2

$PL^{crit}=6$



WL=15

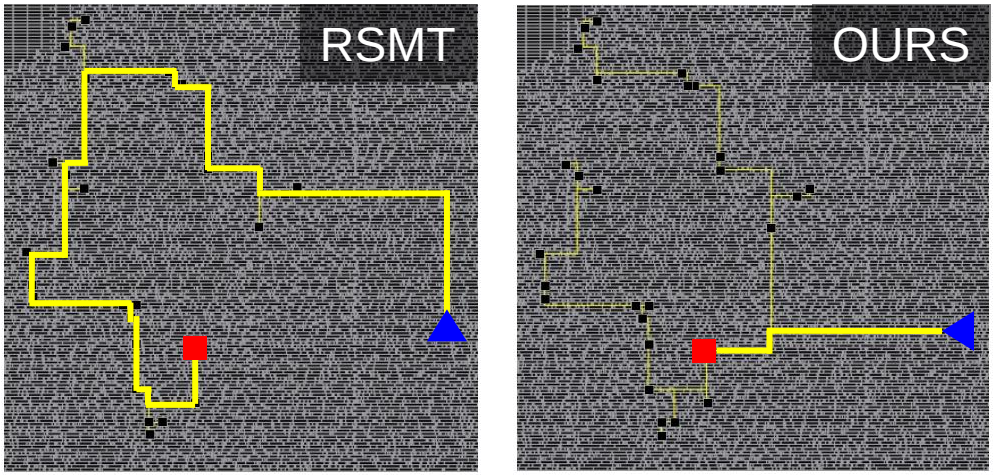
Short PL to critical pins

Robust timing
w/ minimal WL increase

Net Topology – Experimental Results

- Integrated our methodology into **OpenROAD(C++)**
- **Net Topology Construction:** FLUTE(RSMT), PD-II(RSSLT), Ours

Example



Delay to the critical pin:
$64.6ps \rightarrow 21.7ps$

Comparison of results for the post-route final designs

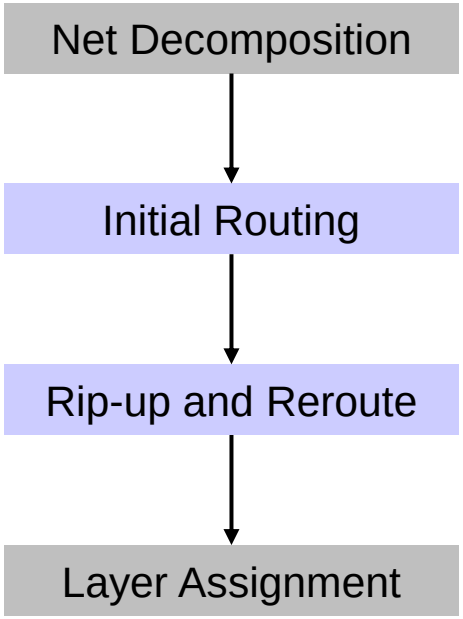
WNS: -18.28%

TNS: -53.37%

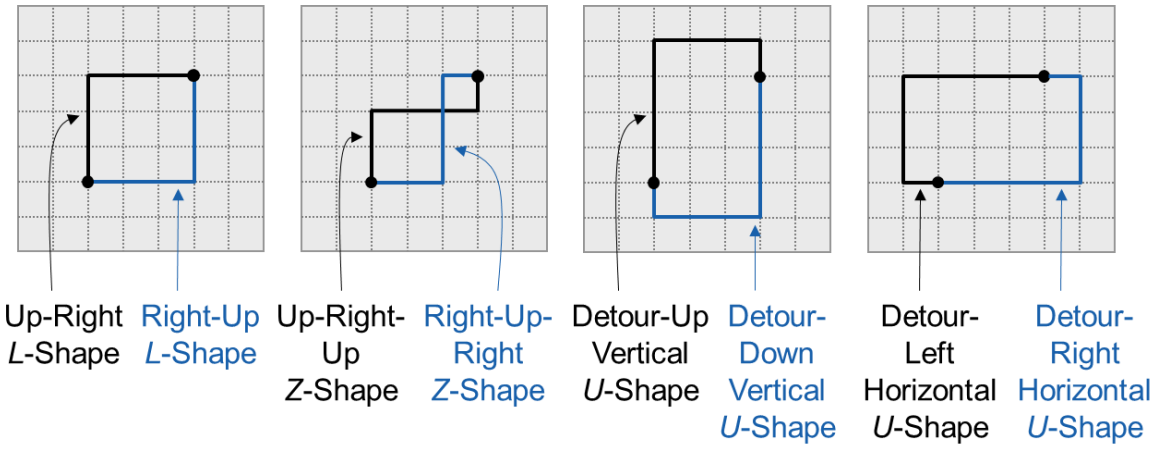
Power: -0.06%

Reference: Jayoung Yang and Taewhan Kim, "Improving Timing Quality Through Net Topology Optimization in Global Routing"
IEEE International System-on-Chip Conference (SOCC) 2024

Pattern Routing



- **Pattern Routing**
  - Searches through a small number of route patterns to im prove runtime
  - Topologies commonly used in pattern routing: *L*-shapes, *Z*-shapes, *U*-shapes



Pattern Routing

Net Decomposition

↓

Initial Routing

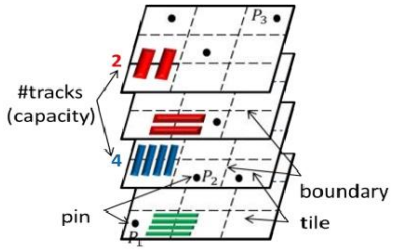
↓

Rip-up and Reroute

↓

Layer Assignment

- **Negotiated-Congestion Routing**



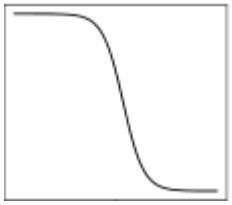
$capacity(e)$: Edge e를 지나갈 수 있는 최대 track 수
(주로 $\frac{gcell_tile_size}{track_pitch}$로 계산)

$demand(e)$: Edge e에서 routing에 사용된 track 수

The edge cost ***cost(e)*** is increased according to t he *edge congestion*

Cost function of CUGR 2.0

$1/(1+e^{capacity(e)-demand(e)})$



$capacity(e) - demand(e)$

[LAB1] Objective - Random Sensitivity Analysis

Random exploration can be used to identify **potential improvements over default flow**

- **Ex) Random-ordered Cell Placement → Placement metric change**

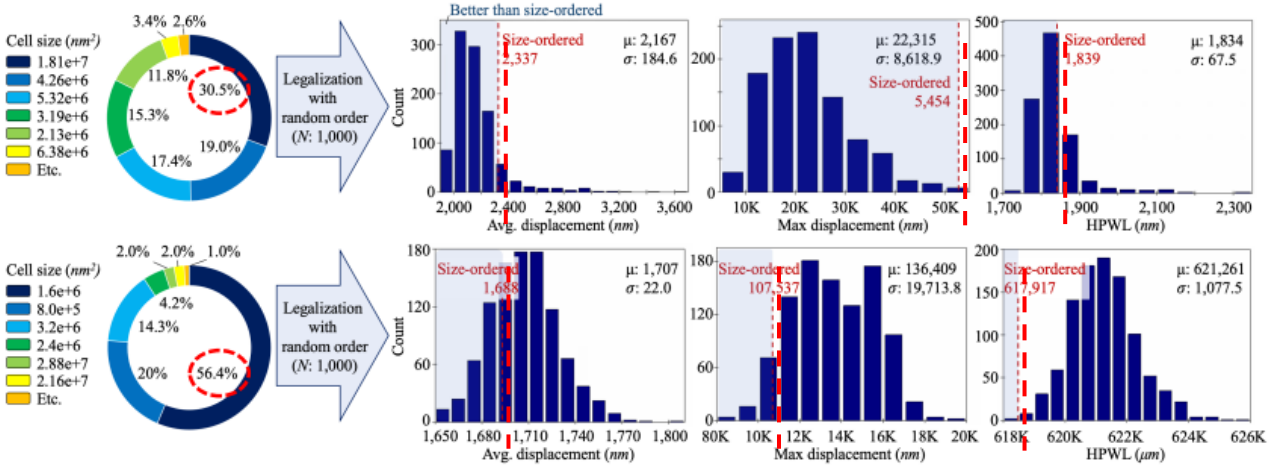
S. -Y. Lee, et al., "RL-Legalizer: Reinforcement Learning-based Cell Priority Optimization in Mixed-Height Standard Cell Legalization," 2023 DATE

(a) usb_phy

OpenCores design implemented with 75% util. and 1.0 aspect ratio in 45-nm NanGate technology.

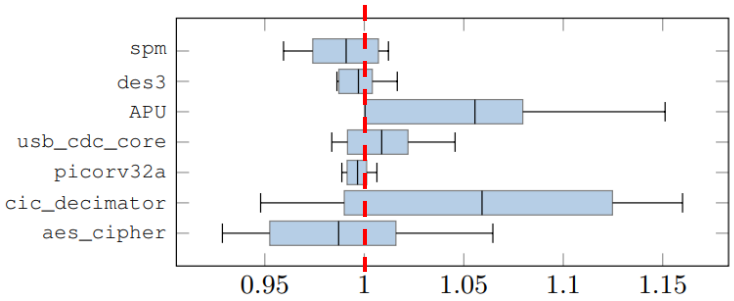
(b) pci_bridge32_b_md3

ICCAD-2017 CAD contest benchmark.



- **Ex) Random Steiner Point Disturbance → Timing metric change**

S. Liu, Z. et al., "Concurrent Sign-off Timing Optimization via Deep Steiner Points Refinement," 2023 DAC



Distribution of sign-off TNS ratio of the updated solution with random Steiner point disturbance to the original one

[LAB1] Adjustable parameters in Routing (Innovus)

```
setAttribute -net <net_name> -avoid_detour {true|false} -weight <integer> …
```

Attaches attributes to nets and subnets. Attaching the attributes allows the NanoRoute routing commands to route the nets following specific requirements.

Parameters

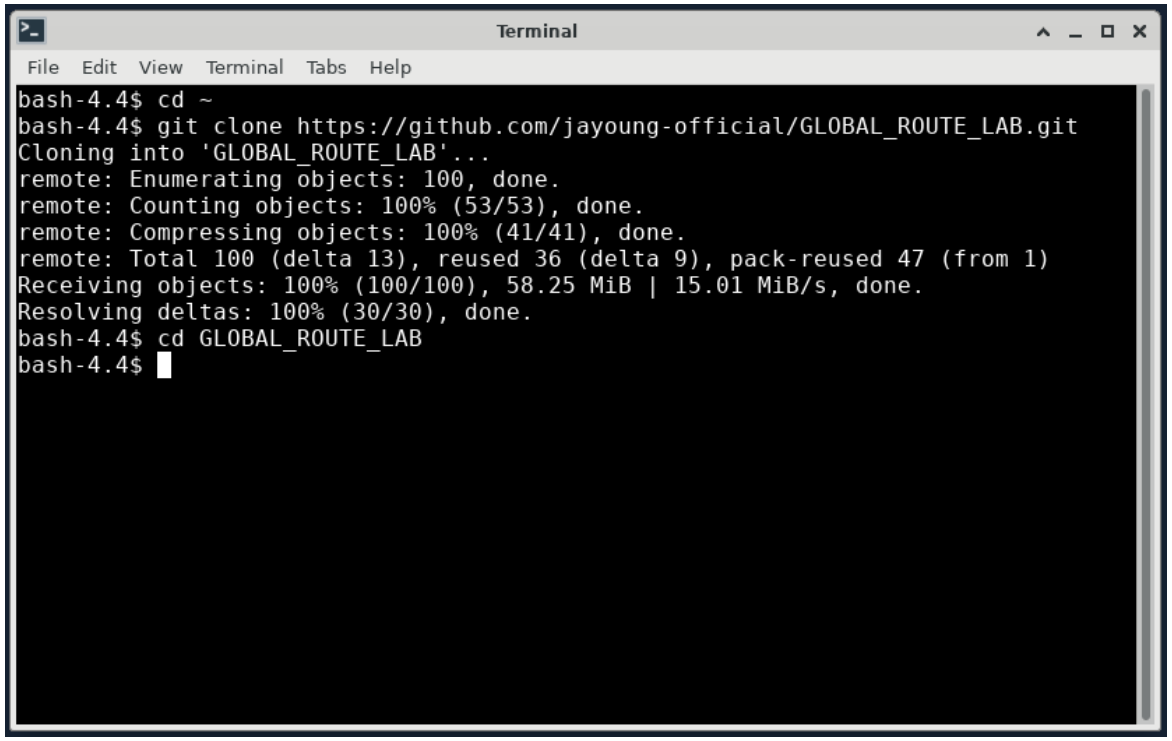
`-avoid_detour {true | false}`

Avoids detours of roughly more than a few gcell grids on the specified nets. This attribute affects global routing only. (Default: false)
Note: Cadence recommends that you use caution with this attribute, as it adds congestion to the design.

`-weight <integer>`

Specifies a relative weight for routing nets. In each switch box, the NanoRoute router routes nets with the highest weight first, then the next highest weight, and so on. Specify a value higher than 2 to ensure a net is routed before other nets. (Default: **2**)

[LAB1-1] Download LAB Materials




```
cd ~
git clone https://github.com/jayoung-official/GLOBAL_ROUTE_LAB.git
cd GLOBAL_ROUTE_LAB
```