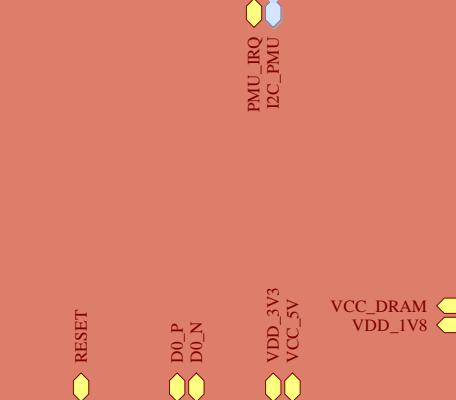
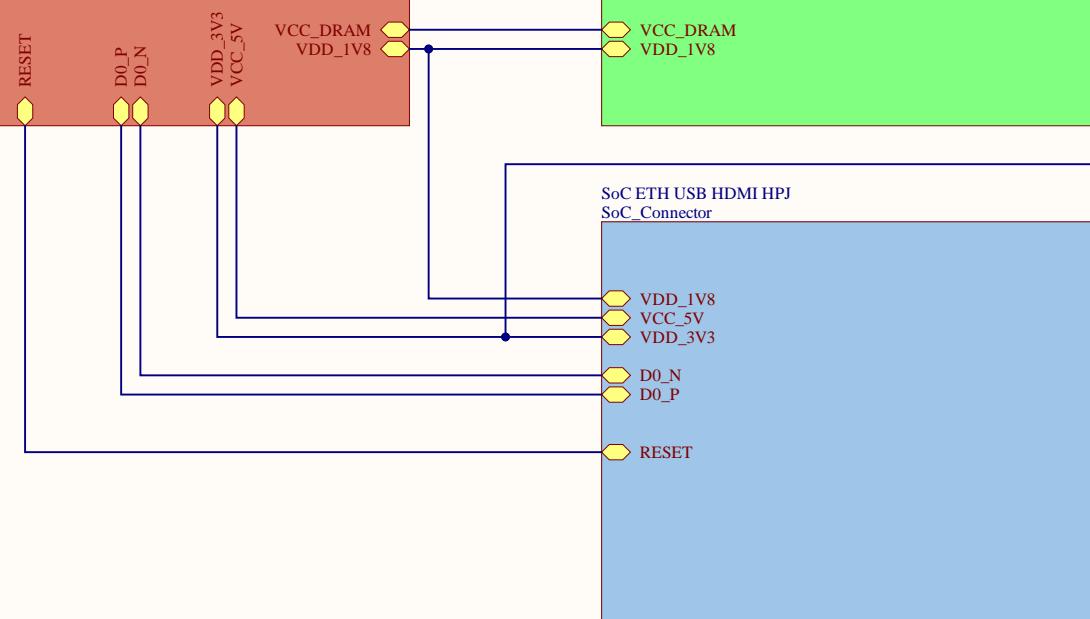
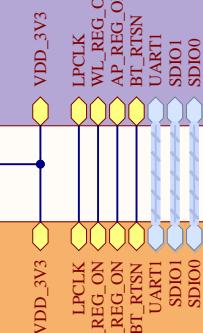
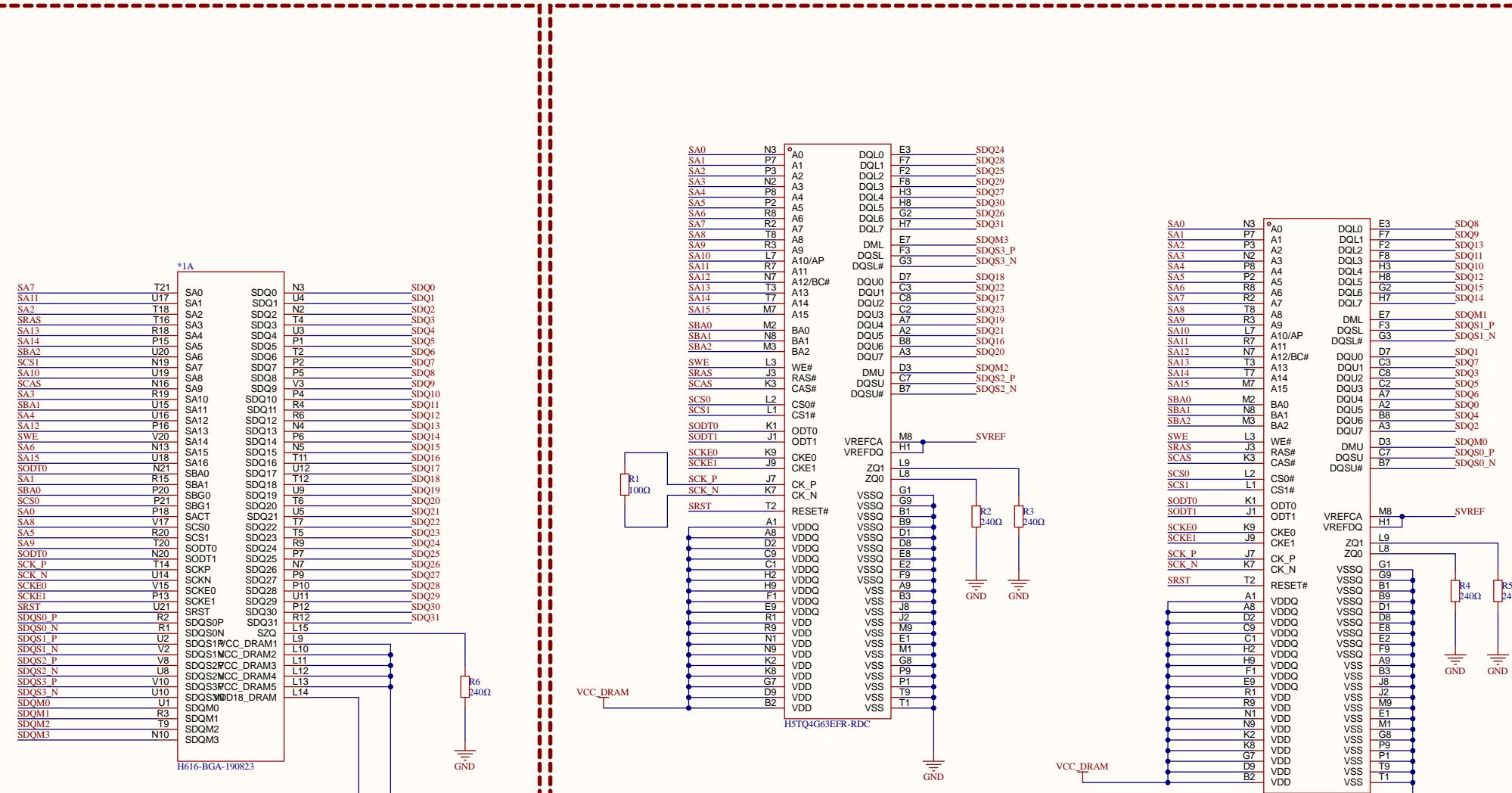


1 2 3 4

SoC_PWR & POWER
SoC_PWRSoC_DDR & DDR3
SoC_DDRSoC_SDIO
SoC_SDIOSoC ETH USB HDMI HPJ
SoC_ConnectorWiFi_TF_EMMC
WiFi_TF_EMMC

Title		
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A4		
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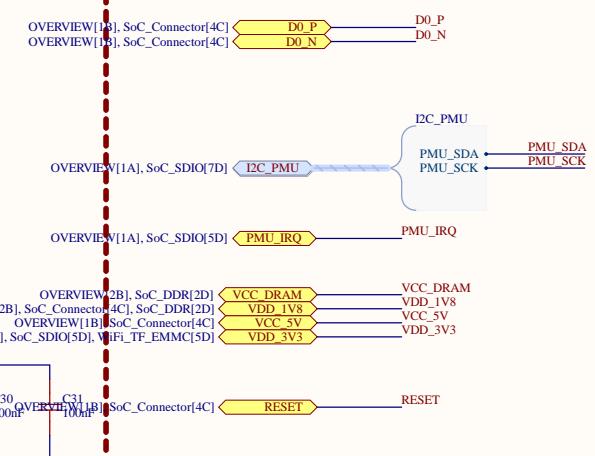
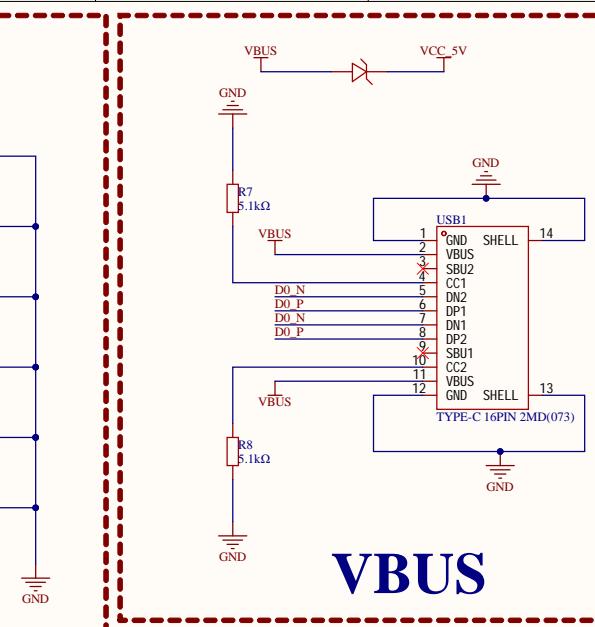
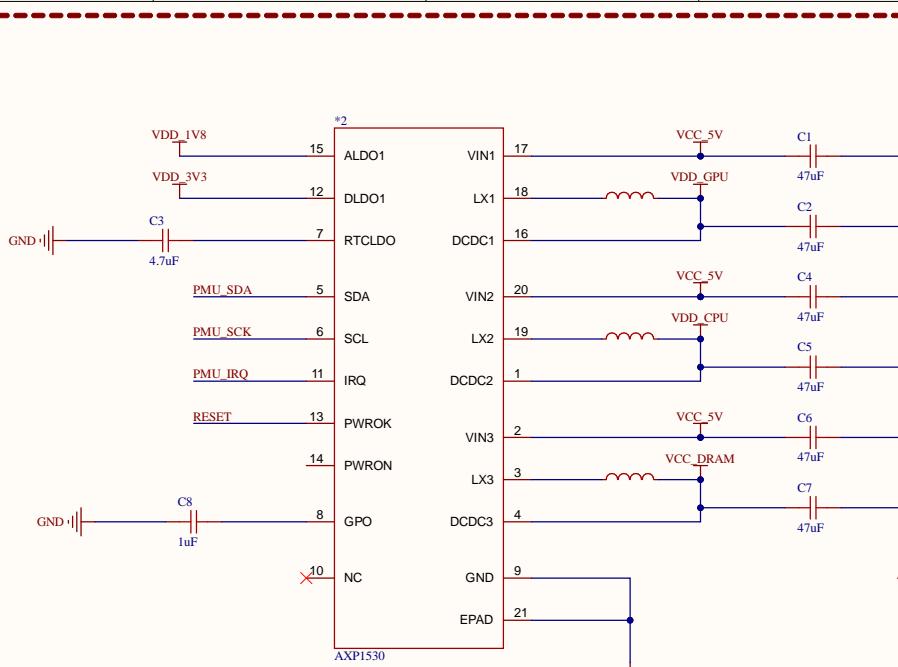
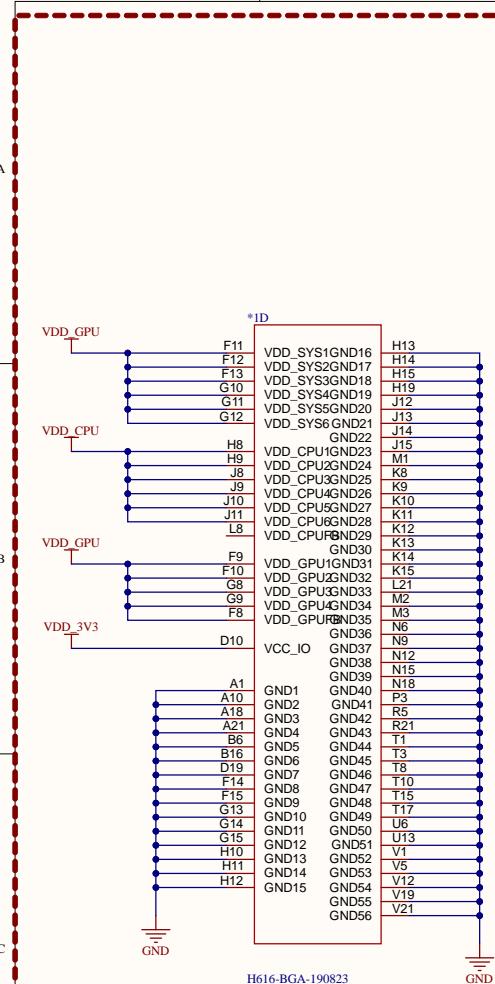


SoC DDR

DDR3

The diagram shows two main horizontal connections. The top connection starts with a red vertical bar, followed by the label "OVERVIEW[2B]", then "SoC_PWR[7C]" in a blue box, then "VCC_DRAM" in a yellow box, and finally "VDD_1V8" in a purple box. The bottom connection starts with "OVERVIEW[2B]", followed by "SoC_Connector[4C]", then "SoC_PWR[7D]" in a blue box, and ends with "VDD_1V8" in a purple box.

Title		
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A3		
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Title		
Size	Number	Revision
A3		
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