Z-Lite Block Diagram

REV	DATE	PAGES	DESCRIPTION
1.0	24/04/2020	All	Rev 1.0 Release
1.1	29/05/2020	All	Rev 1.1 Release

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3	PS BANK502
4	PL BANK0&13
5	PL BANK34&35
6	ZYNQ Power
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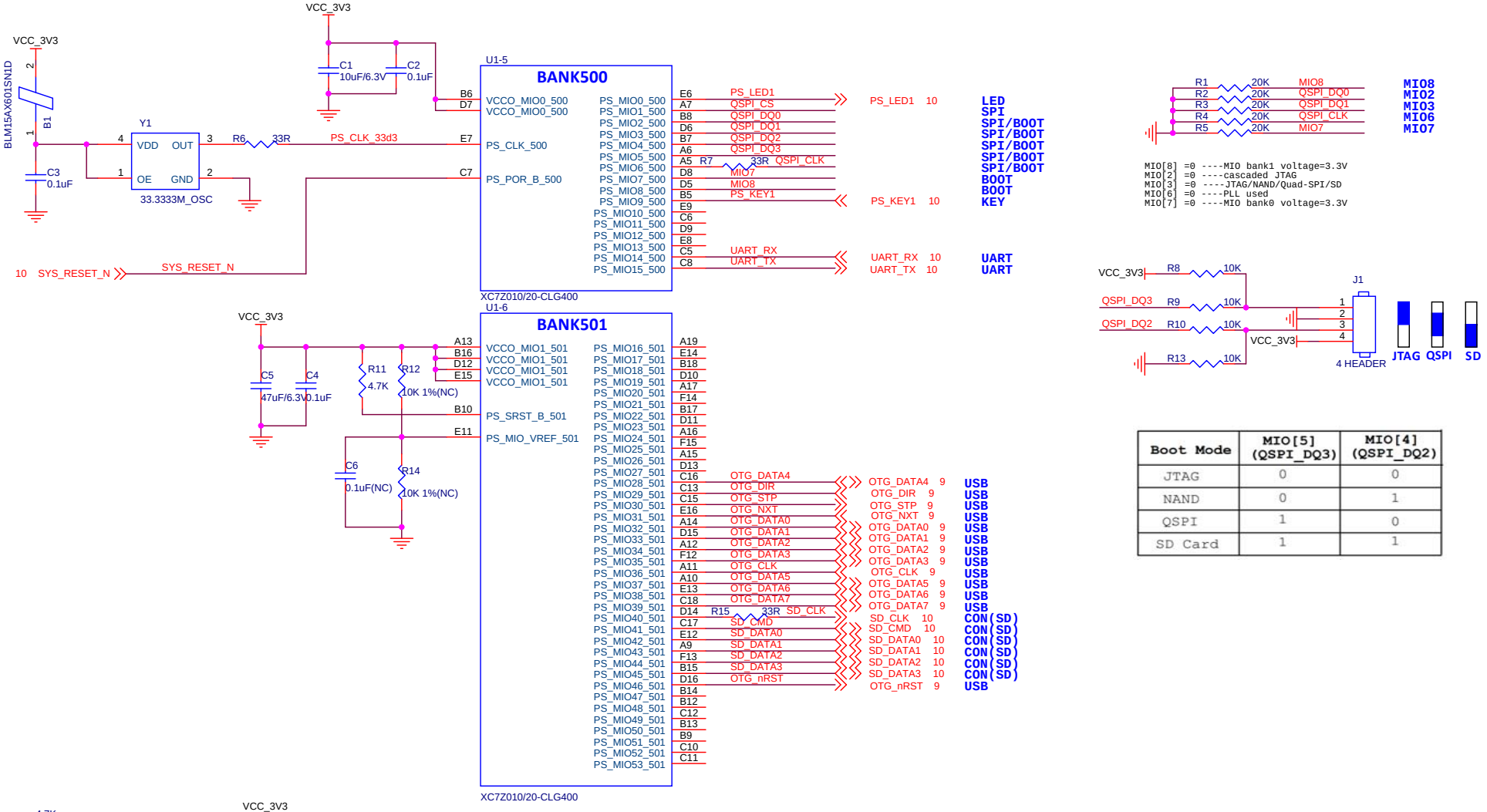
Title: Mizar Board

Size: B | Document Number: Block Diagram | Rev: 1.0

Date: Monday, July 20, 2020 | Sheet 1 of 14



Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

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Title: Mizar Board

Size: B | Document Number: PS BANK500&501 | Rev: 1.0

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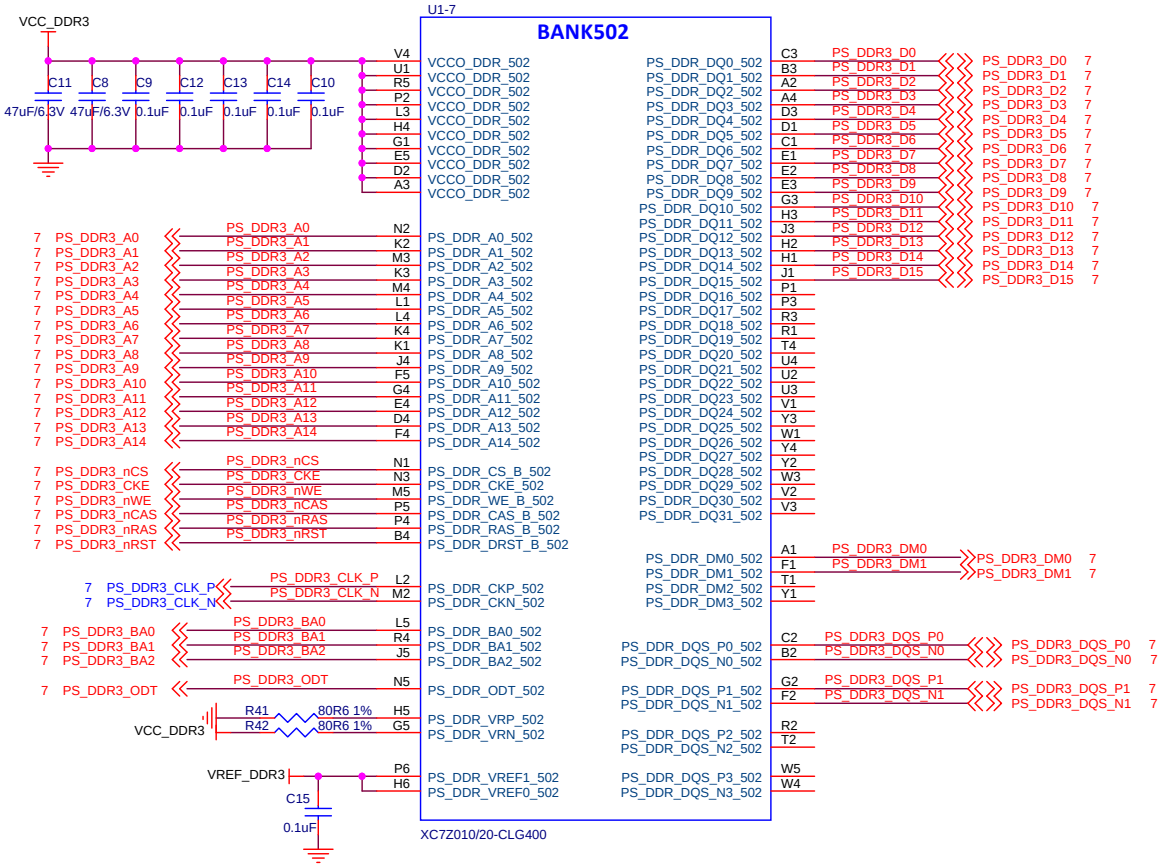
DDR3



Title			
Mizar Board			
Size: B	Document Number: PS BANK502		Rev: 1.0
Date: Monday, July 20, 2020	Sheet 3 of 14		

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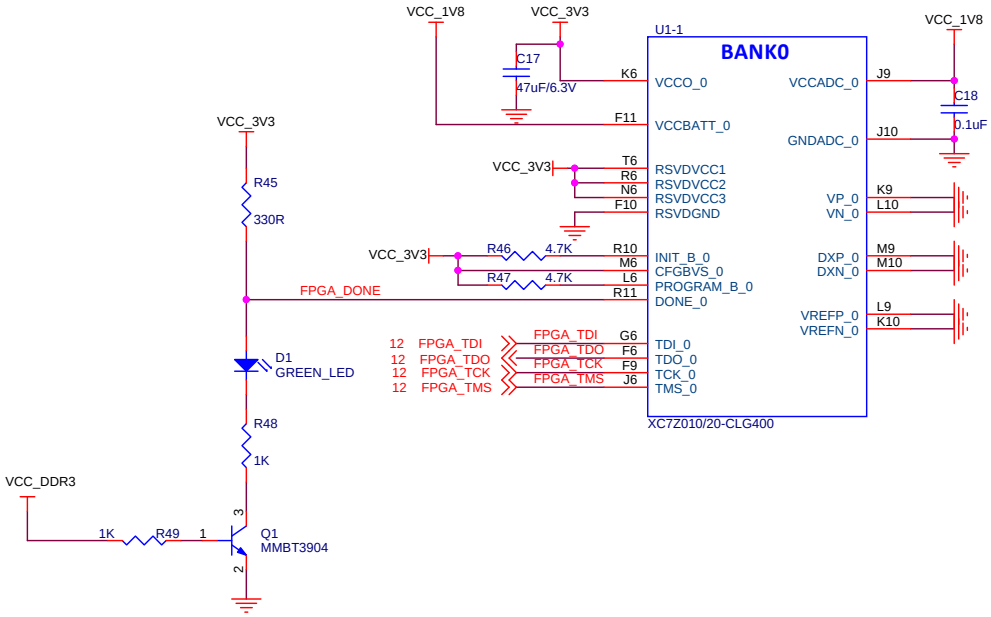
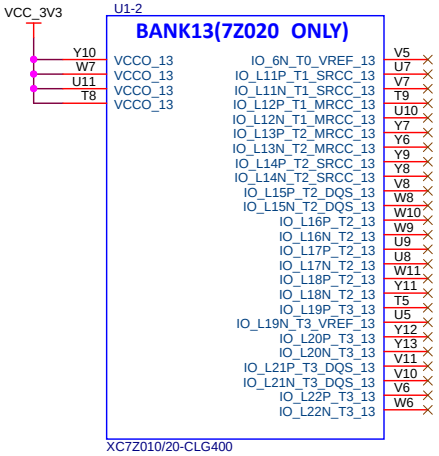
ZYNQ_CONFIG





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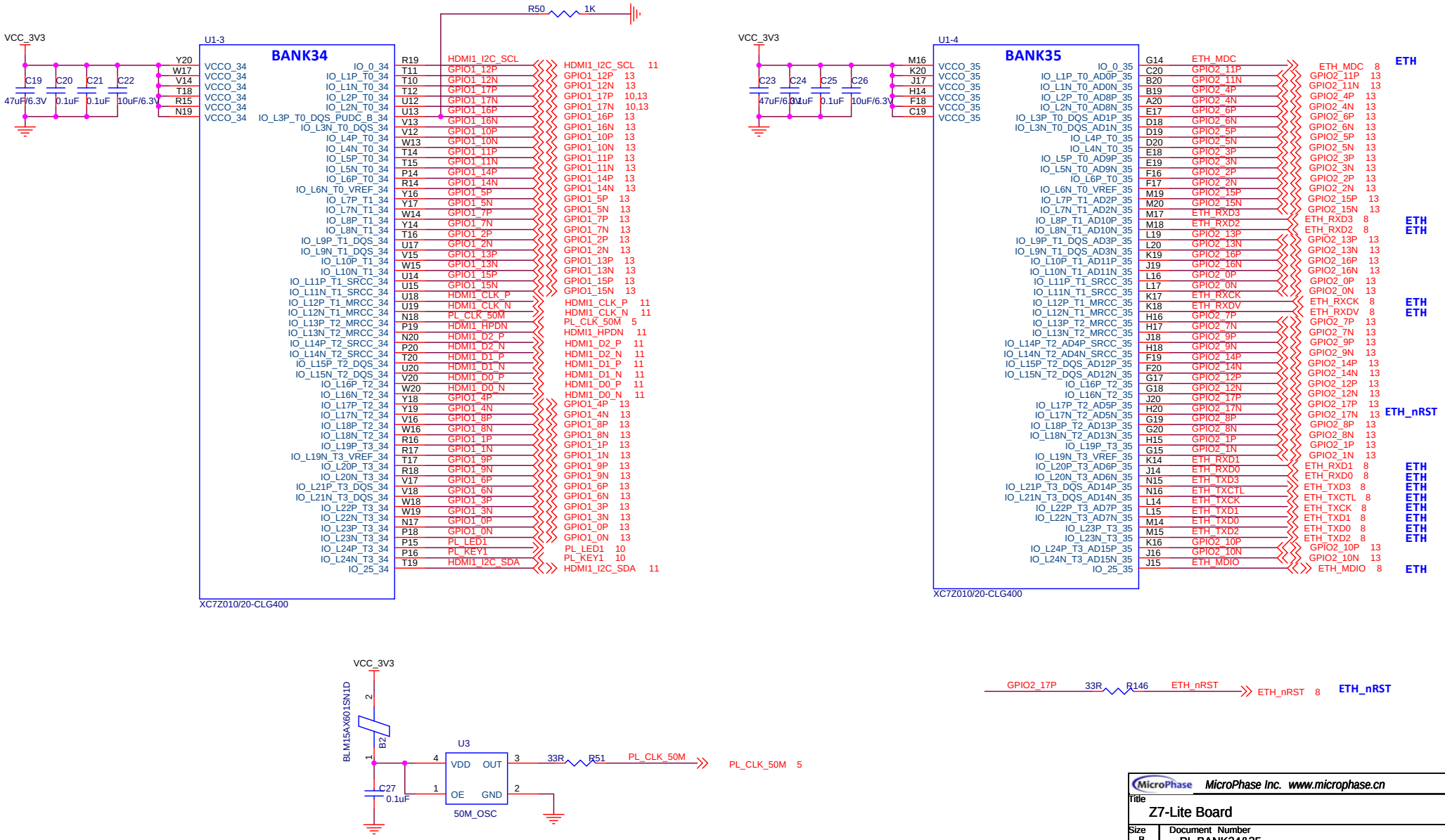
Title: Z7-Lite Board

Size	Document Number	Rev
B	PL BANK0&13	1.0

Date: Monday, July 20, 2020 Sheet 4 of 14

FPGA_PL



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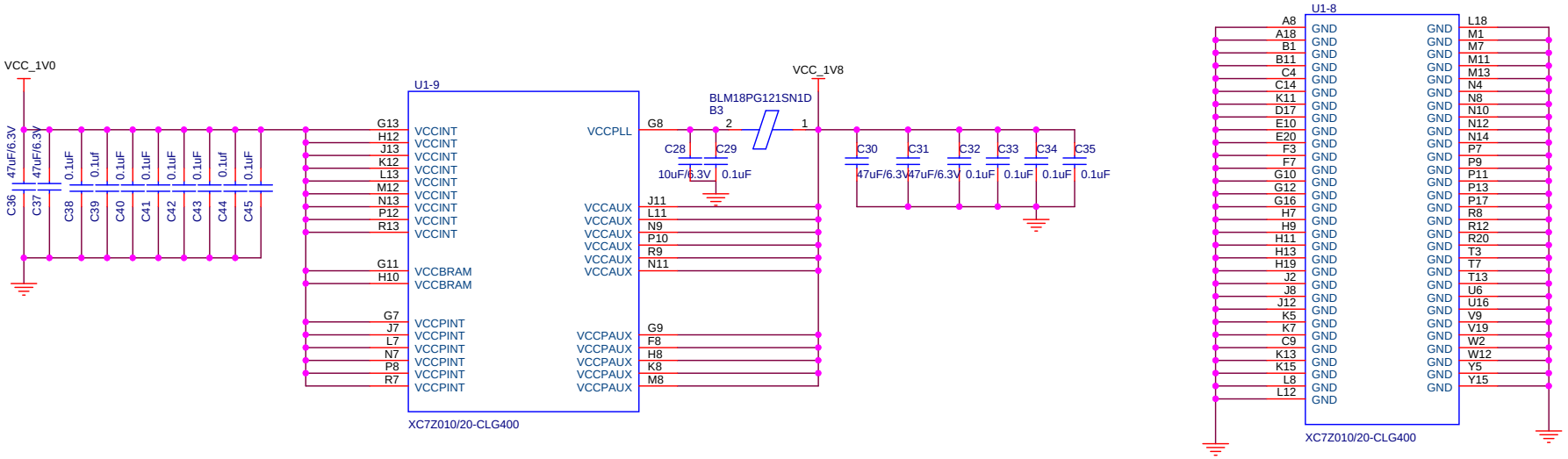
Title: Z7-Lite Board			
Size: B	Document Number: PL BANK34&35		Rev: 1.0
Date: Monday, July 20, 2020	Sheet 5 of 14		



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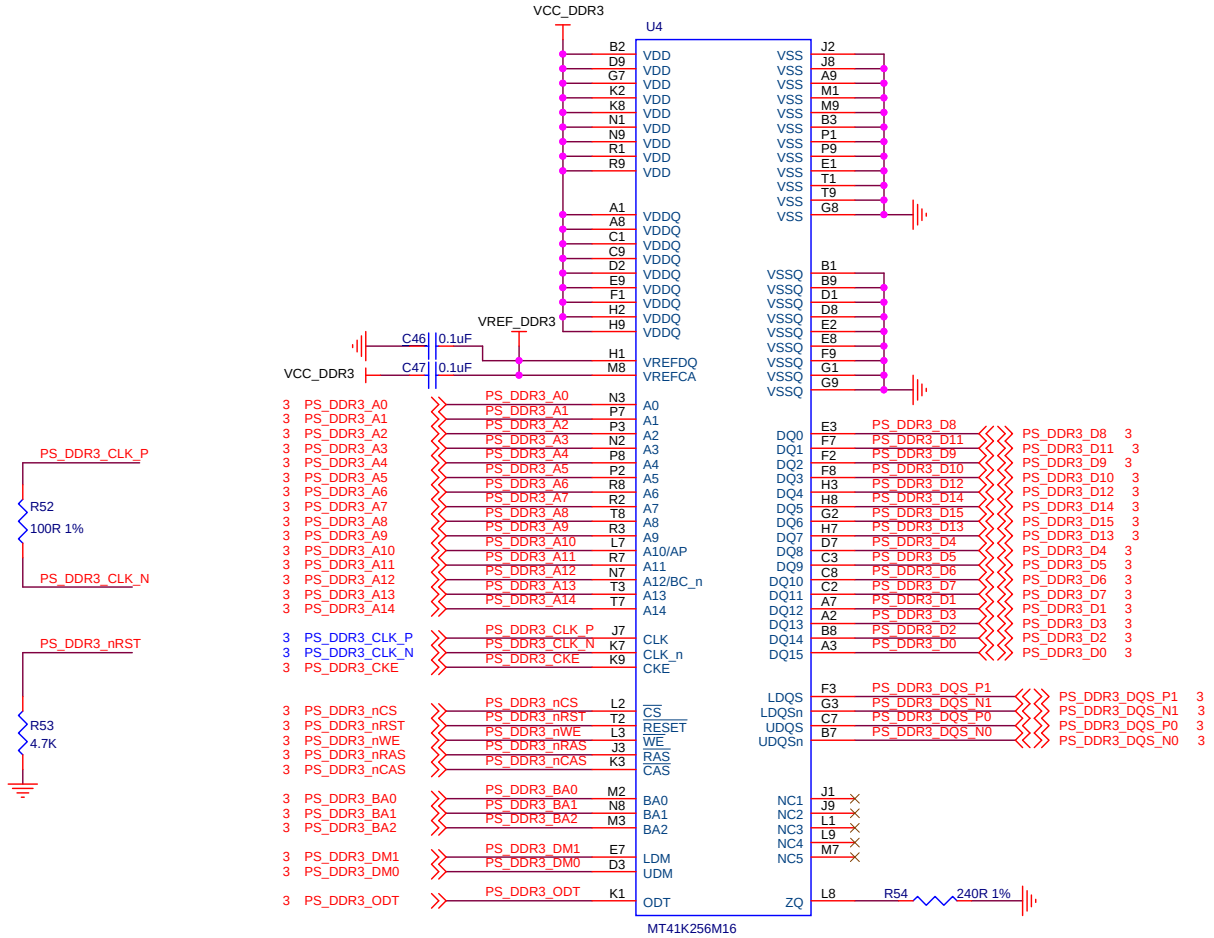
Title: Z7-Lite Board

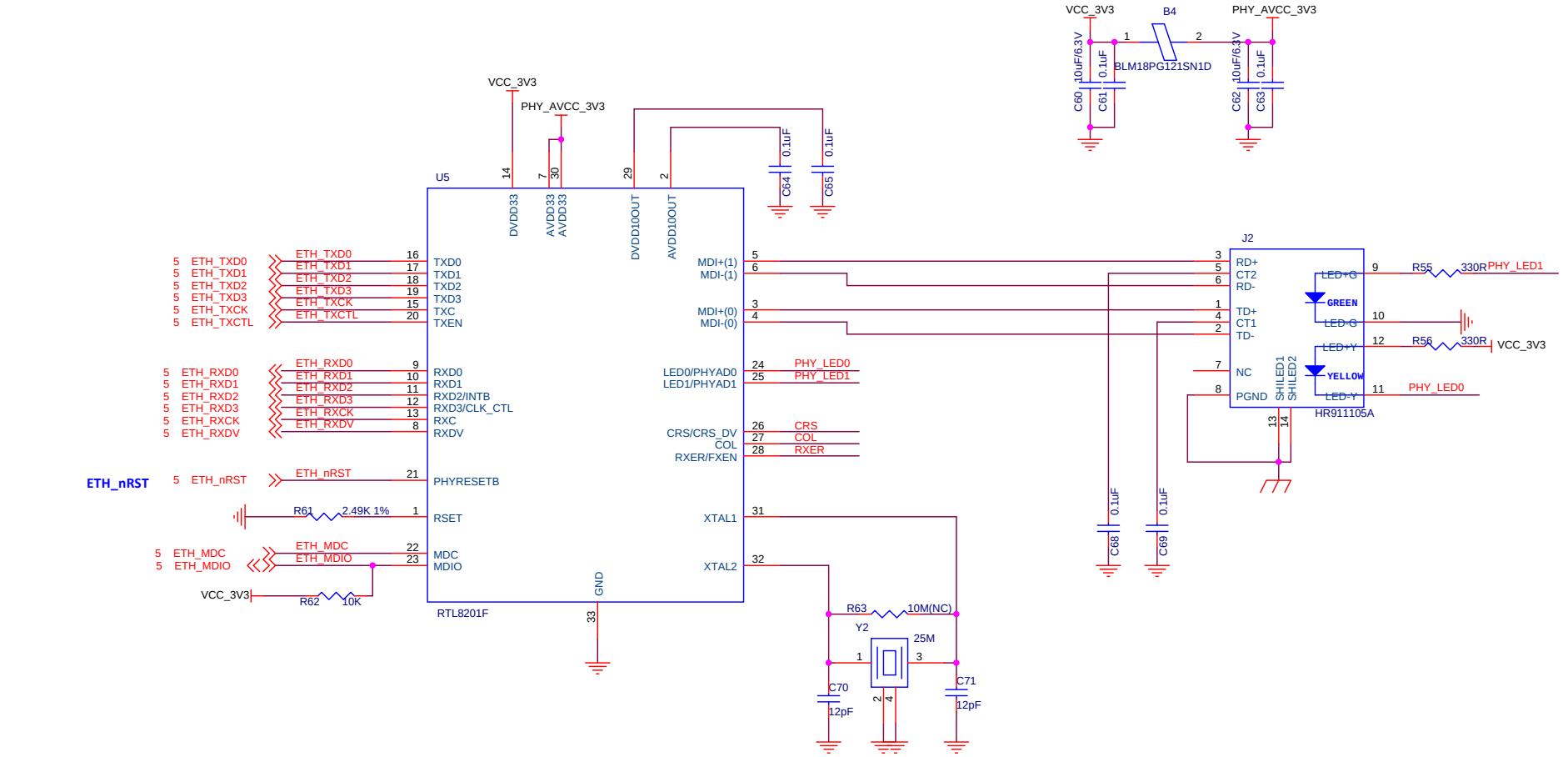
Size: B | Document Number: ZYNQ Power | Rev: 1.0

Date: Monday, July 20, 2020 | Sheet 6 of 14

PS_DDR3



MicroPhase	MicroPhase Inc. www.microphase.cn
Title	Z7-Lite Board
Size B	Document Number DDR3 RAM
Rev	1.0
Date:	Monday, July 20, 2020
Sheet	7 of 14



MicroPhase	MicroPhase Inc. www.microphase.cn		
Title	Z7-Lite Board		
Size B	Document Number PS ETHERNET		Rev 1.0
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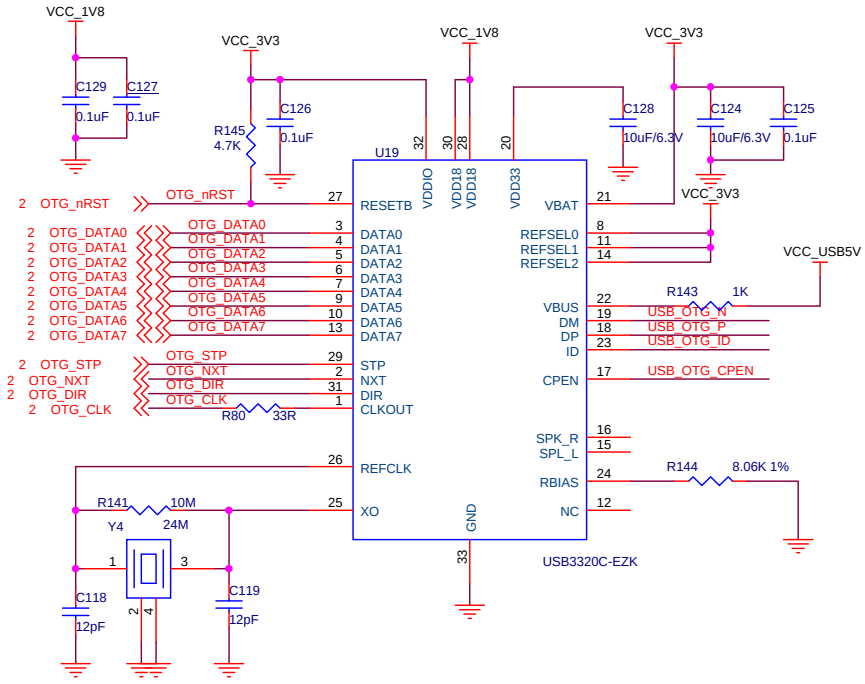
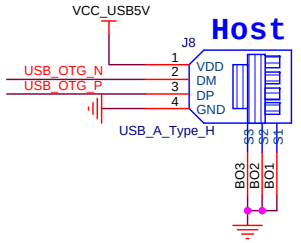
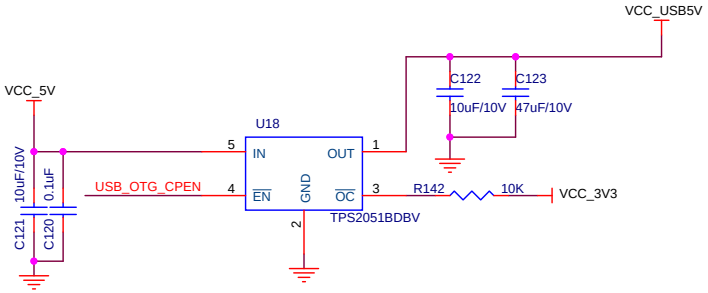
PS USB OTG







Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4 MHz
0	1	0	12 MHz
0	1	1	27 MHz
1	0	0	13 MHz
1	0	1	19.2 MHz
1	1	0	26 MHz
1	1	1	24 MHz

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Title: Z7-Lite Board

Size: B | Document Number: PS USB | Rev: 1.0

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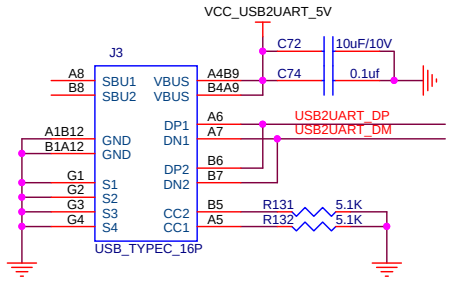

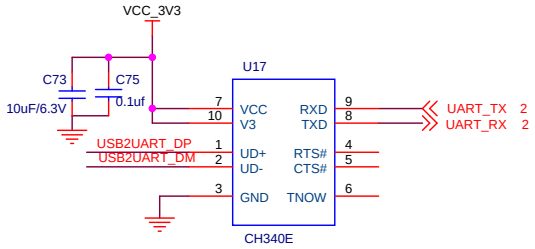

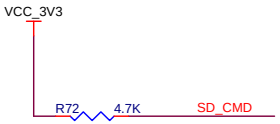

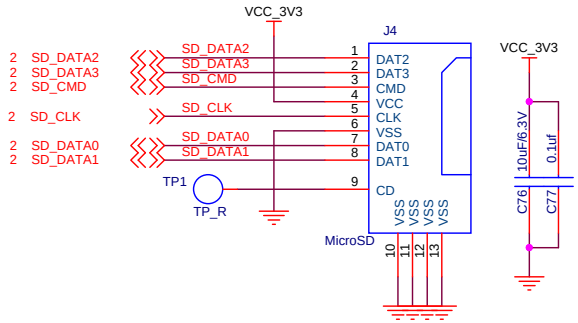

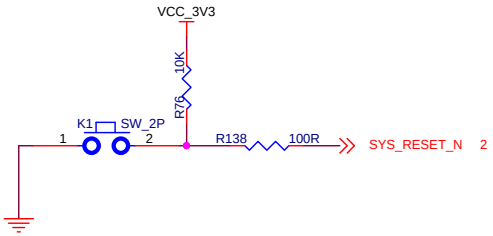

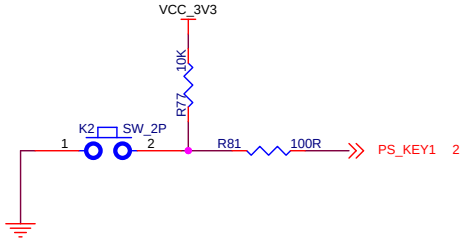

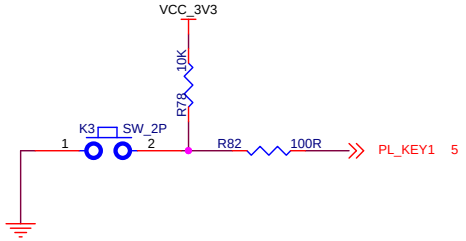

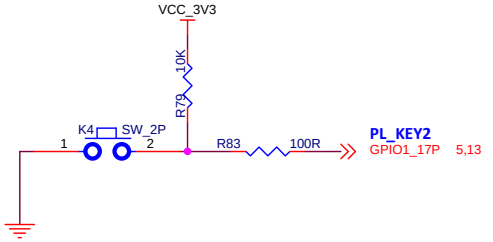

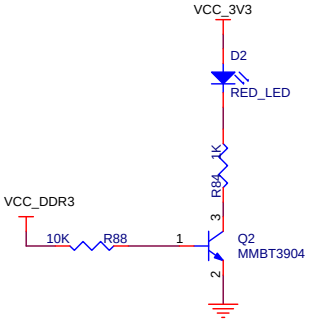

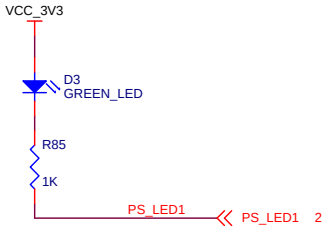

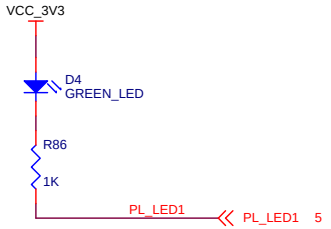

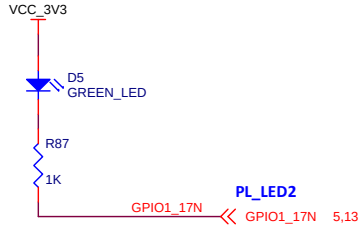

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Title: Z7-Lite Board

Size: B | Document Number: PS UART SD | Rev: 1.0

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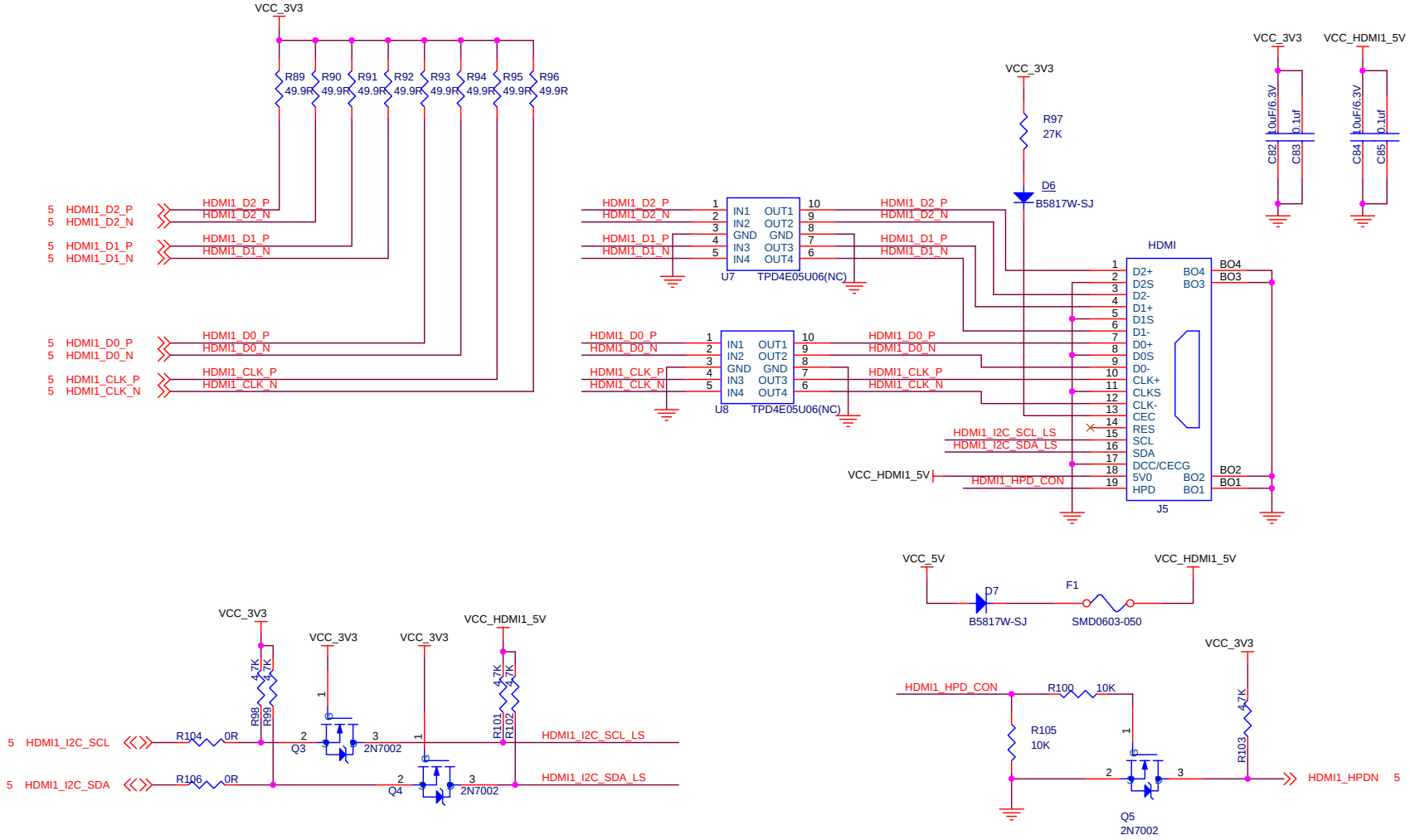

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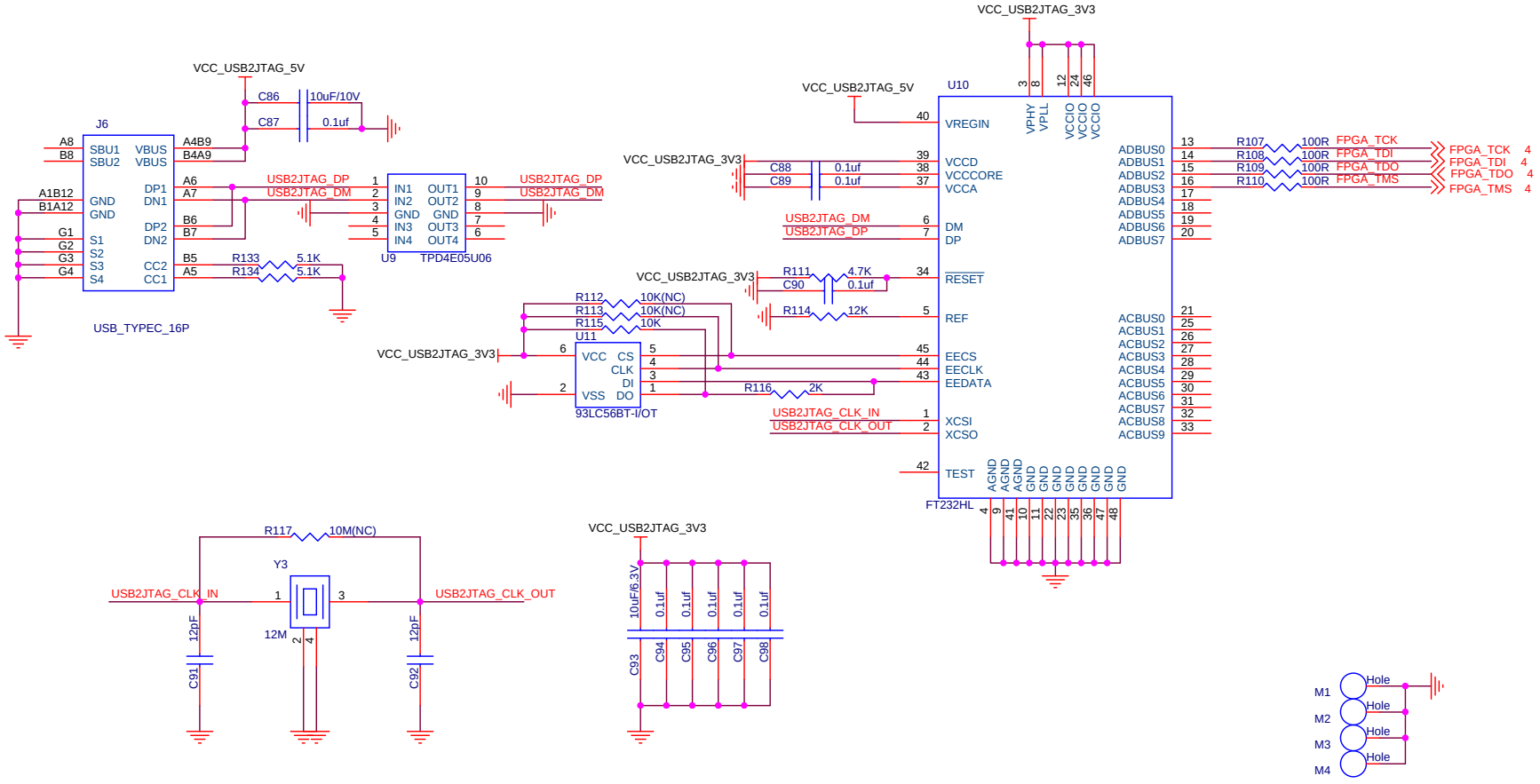
Title: Z7-Lite Board		
Size: B	Document Number: HDMI TX	Rev: 1.0
Date: Monday, July 20, 2020	Sheet 11 of 14	



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Title	Z7-Lite Board	
Size B	Document Number USB-JTAG	Rev 1.0
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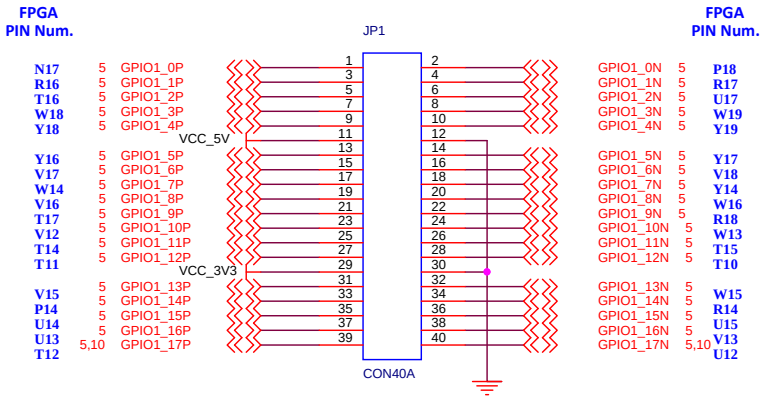
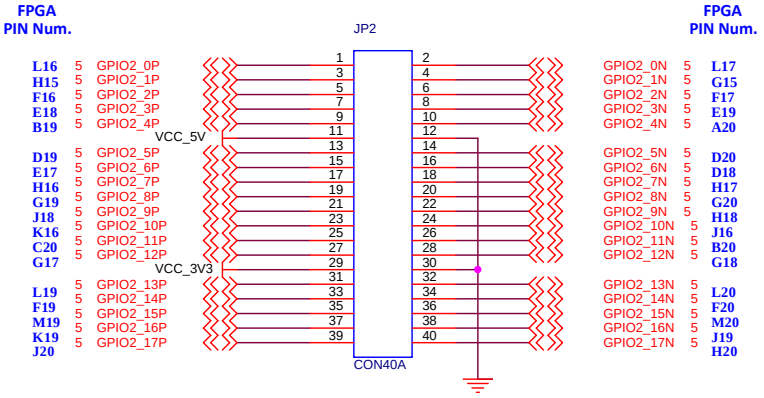
GPIO Interface





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Title: Z7-Lite Board

Size	Document Number	Rev
B	GPIO	1.0

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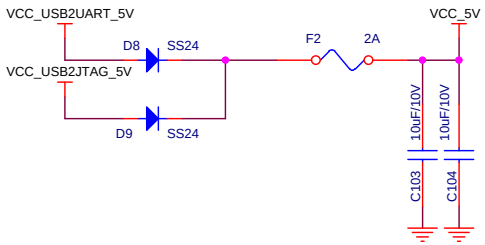
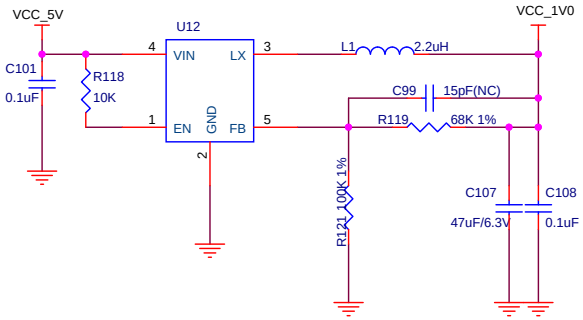
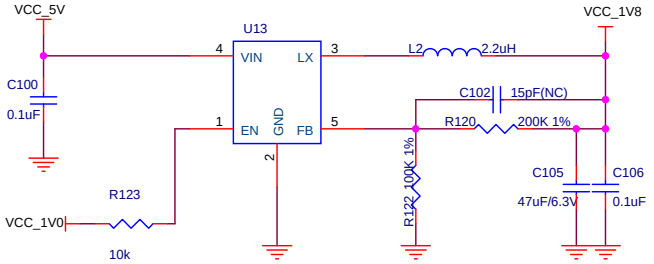




Vref = 0.6V VOUT = 1.0V



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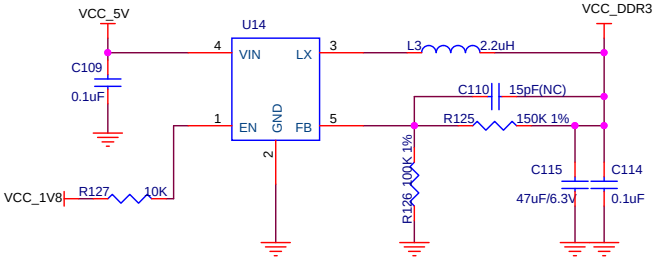
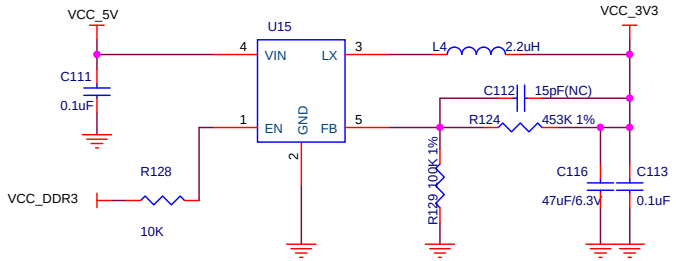


Vref = 0.6V VOUT = 1.5V



Vref = 0.6V VOUT = 3.3V

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Title: Z7-Lite Board

Size	Document Number	Rev
B	Power	1.0

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