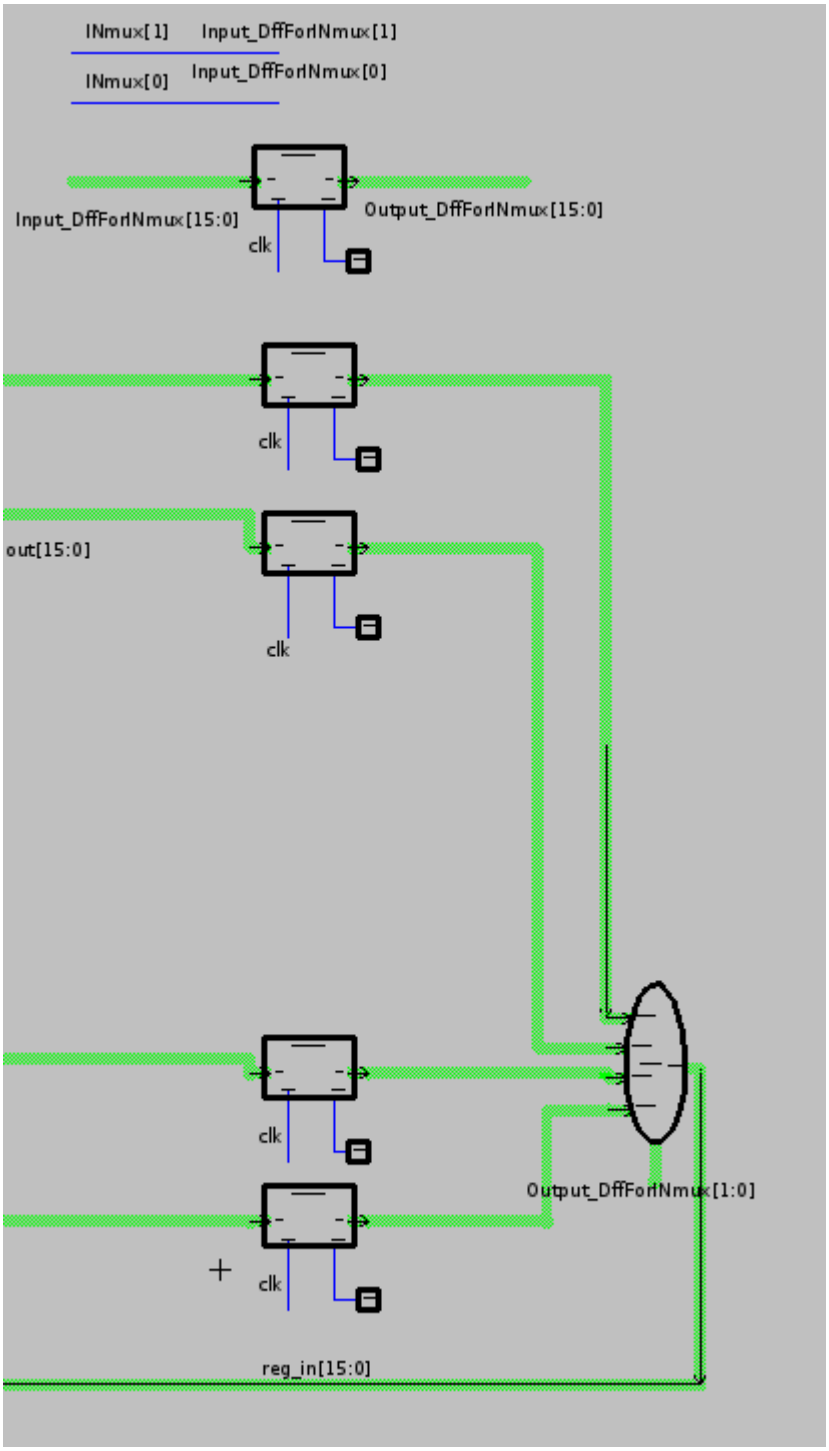
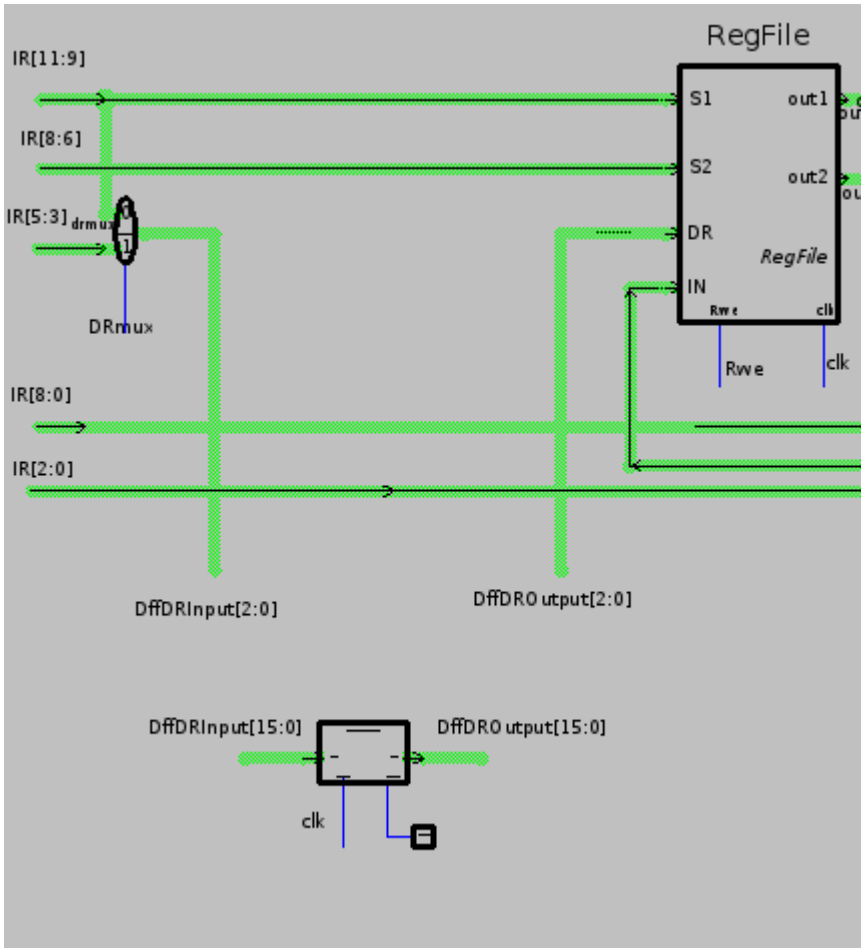
Pipeline level1:
[process]:
1.add DFFs before result mux whose output will be written to RegFile
2.add DFF before control signal INmux[1:0]
3.add DFF before DR[2:0], which make the output of mux and DR synchronous.





[result]:
pipeline: level1:

==========(1500)==========

R0[0000] R1[0000] R2[0000] R3[0000] R4[0000] R5[0000] R6[0000] R7[0000]

---- Memory ----
addr ---- content---- translation
---- ---------- ----------
01fc: 1111111111111111 unknown instruction
01fd: 1111111111111111 unknown instruction
01fe: 1111111111111111 unknown instruction
01ff: 1111111111111111 unknown instruction
PC==> 0200: 0001111101011110 <== LIM DR7 15e
0201: 0000111111001000 ALU SR7 SR7 DR1 ADD
0202: 0000000001010100 ALU SR0 SR1 DR2 SUB
0203: 0100011000000000 LEA DR3
0204: 0001100000000110 LIM DR4 006
0205: 0010101011000000 LDR DR5 AR3

==========

```
======================(3500)===========

 R0[0000] R1[0000] R2[0000] R3[0000] R4[0000] R5[0000] R6[0000] R7[0000]

            ---- Memory ----
     addr      ---- content----       translation
     ----      ----------------       ----------------
     01fd:     1111111111111111       unknown instruction
     01fe:     1111111111111111       unknown instruction
     01ff:     1111111111111111       unknown instruction
     0200:     0001111101011110       LIM  DR7  15e
PC==> 0201:    0000111111001000 <==   ALU  SR7  SR7  DR1 ADD
     0202:     0000000001010100       ALU  SR0  SR1  DR2 SUB
     0203:     0100011000000000       LEA  DR3
     0204:     0001100000000110       LIM  DR4  006
     0205:     0010101011000000       LDR  DR5  AR3
     0206:     0011000011000000       STR  SR0  AR3
            ----------------
==========================================

======================(5500)===========

 R0[0000] R1[0000] R2[0000] R3[0000] R4[0000] R5[0000] R6[0000] R7[ff5e]

            ---- Memory ----
     addr      ---- content----       translation
     ----      ----------------       ----------------
     01fe:     1111111111111111       unknown instruction
     01ff:     1111111111111111       unknown instruction
     0200:     0001111101011110       LIM  DR7  15e
     0201:     0000111111001000       ALU  SR7  SR7  DR1 ADD
PC==> 0202:    0000000001010100 <==   ALU  SR0  SR1  DR2 SUB
     0203:     0100011000000000       LEA  DR3
     0204:     0001100000000110       LIM  DR4  006
     0205:     0010101011000000       LDR  DR5  AR3
     0206:     0011000011000000       STR  SR0  AR3
     0207:     0000011100110000       ALU  SR3  SR4  DR6 ADD
            ----------------
==========================================
```

[analysis]
after two clock cycles, ff5e is written to R7 register successfully.