ARM®-based 32-bit Cortex®-M4F MCU+FPU with 64 to 256 KB Flash, sLib, USB, 2 CANs, 12 timers, 2 ADCs, 13 communication interfaces

Feature

- **Core: ARM® 32-bit Cortex®-M4F CPU with FPU**
  - 200 MHz maximum frequency, with a memory protection unit (MPU)
  - Single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 64 to 256 Kbytes of Flash instruction/data memory
  - sLib: configurable part of main Flash set as a libruary area with code excutable but secured, non-readable
  - SPIM interface: Extra interfacing up to 16 Mbytes of the external SPI Flash (as instruction/data memory)
  - Up to 64 Kbytes of SRAM
- **Clock, reset, and supply management**
  - 2.6 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4 to 25 MHz crystal oscillator
  - Internal 48 MHz factory-trimmed RC (accuracy 1 % at T_A = 25 °C, 2.5 % at T_A = -40 to +105 °C), with automaitc clock calibration (ACC)
  - Internal 40 kHz RC oscillator
  - 32 kHz oscillator with calibration
- **Low power**
  - Sleep, Stop, and Standby modes
  - V_{BAT} supply for RTC and forty-two 16-bit backup registers
- **2 x 12-bit, 0.5 µs A/D converters (up to 16 channels)**
  - Conversion range: 0 to 3.6V
  - Double sample-and-hold capability
  - Temperature sensor
- **DMA: 14-channel DMA controller**
  - Supported peripherals: timers, ADCs, SDIOs, I²Ss, SPIs, I²Cs, and USARTs
- **Debug mode**
  - Serial wire debug (SWD) and JTAG interfaces
- **Up to 55 fast I/O**
  - 27/39/55 multi-functional bi-directional I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
  - All fast I/Os, control registers accessable with f_{AHB} speed
- **Up to 12 timers**
  - Up to 5 x 16-bit timers + 2 x 32-bit timers, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Up to 2 x 16-bit motor control PWM advanced timers with dead-time generator and emergency stop
  - 2 x watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
- **Up to 13 communication interfaces**
  - 2 x I²C interfaces (SMBus/PMBus)
  - Up to 5 x USARTs (ISO7816 interface, LIN, IrDA capability, modem control)
  - 2 x SPIs (50 Mbit/s), both with I²S interface multiplexed
  - 2 x CAN interface (2.0B Active)
  - USB 2.0 full speed interface supporting crystal-less
  - SDIO interfaces
- **CRC calculation unit, 96-bit unique ID**
- **Packages**
  - LQFP64 10 x 10 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm
  - QFN32 4 x 4 mm

Table 1. Device summary

Internal Flash	Part number
256 KBytes	AT32F413RCT7, AT32F413CCT7, AT32F413CCU7, AT32F413KCU7-4
128 KBytes	AT32F413RBT7, AT32F413CBT7, AT32F413CBU7, AT32F413KBU7-4
64 KBytes	AT32F413C8T7

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the AT32F413 microcontrollers.

The AT32F413 datasheet should be read in conjunction with the AT32F413 reference manual.

For information on programming, erasing, and protection of the internal Flash memory please also refer to the AT32F413 reference manual.

For information on the Cortex®-M4 core please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website at the following address:

http://infocenter.arm.com

2 Description

The AT32F413 incorporates the high-performance ARM® Cortex®-M4F 32-bit RISC core operating at 200 MHz. The Cortex®-M4F core features a Floating point unit (FPU) single precision which supports all ARM single-precision data processing instructions and data type. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F413 incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, 64 Kbytes of SRAM), the extensive external SPI Flash (up to 16 Mbytes addressing capability), and enhanced I/Os and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the sLib, functioning as a security area with code-excutable only.

The AT32F413 offers two 12-bit ADC, five general-purpose 16-bit timers plus two general-purpose 32-bit timers, and up to two PWM timers for motor control, as well as standard and advanced communication interfaces, up to two I^2Cs, two SPIs (all multiplexed as I^2Ss), an SDIOs, five USARTs, an USB, and two CANs.

The AT32F413 operates in the -40 to +105 °C temperature range, from a 2.6 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

2.1 Device overview

The AT32F413 offers devices in four different package types: from 32 pins to 64 pins. Depending on the different packages, the pin-to-pin is completely compatible among devices, and also the software and functionality. Only different sets of peripherals are included. The description below gives an overview of the complete range of peripherals proposed in different devices.

Table 2. AT32F413 features and peripheral counts

Part Number		AT32F413xxU7-4		AT32F413xxU7		AT32F413xxT7				
		KB	KC	CB	CC	C8	CB	CC	RB	RC
CPU frequency (MHz)		200								
Int. Flash(1)	ZW (KBytes)(2)	96		96		64	96		96	
	NZW (KBytes)(2)	32	160	32	160	0	32	160	32	160
	Total (KBytes)	128	256	128	256	64	128	256	128	256
SRAM (KBytes)(2)		32 / 64 / 16 (configurable)				32	32 / 64 / 16 (configurable)			
Timers	Advanced-control(3)	1	1	1	2	1	1	2	1	2
	32-bit general-purpose	2		2		2			2	
	16-bit general-purpose	5		5		5			5	
	SysTick	1		1		1			1	
	IWDG	1		1		1			1	
	WWDG	1		1		1			1	
	RTC	1		1		1			1	
Communication	I^2C	2		2		2			2	
	SPI/I^2S	2/2(4)		2/2(4)		2/2(4)			2/2	
	USART+UART	2+0		3+0		3+0			3+2	
	SDIO	1(5)		1(5)		1(5)			1	
	USB Device	1		1		1			1	
	CAN	2		2		2			2	
Analog	12-bit ADC numbers	2								
	channels	10		10		10			16	
GPIO		27		39		39			55	
SPIM(6)		1 ch / up to 16 MB								
Operating temperatures		-40 to +105 °C								
Packages		QFN32 4 x 4 mm		QFN48 6 x 6 mm		LQFP48 7 x 7 mm			LQFP64 10 x 10 mm	

(1) ZW = zero wait-state, up to SYSCLK 200 MHz
NZW = non-zero wait-state
(2) The internal Flash and SRAM sizes are configurable with user's option bytes. Take the AT32F413RCT7 as an example, on which the Flash/SRAM can be configured into three options below:
- ZW: 96 KBytes, NZW: 160 KBytes, SRAM: 32 KBytes (factory-shipping default);
- ZW: 64 KBytes, NZW: 192 KBytes, SRAM: 64 KBytes;
- ZW: 112 KBytes, NZW: 144 KBytes, SRAM: 16 KBytes.

(3) For advanced-control timers, AT32F413RCT7 and AT32F413CCx7 support TMR1 and TMR8, others support only TMR1.
(4) Only I^2S1 supports MCK pin.
(5) SDIO supports maximum 4-bit (D0~D3) mode.
(6) SPIM = External SPI Flash memory extension (for both program execution and data storage) with encryption capability.

2.2 Overview

2.2.1 ARM® Cortex®-M4F with FPU core and DSP instruction set

The ARM Cortex®-M4F with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

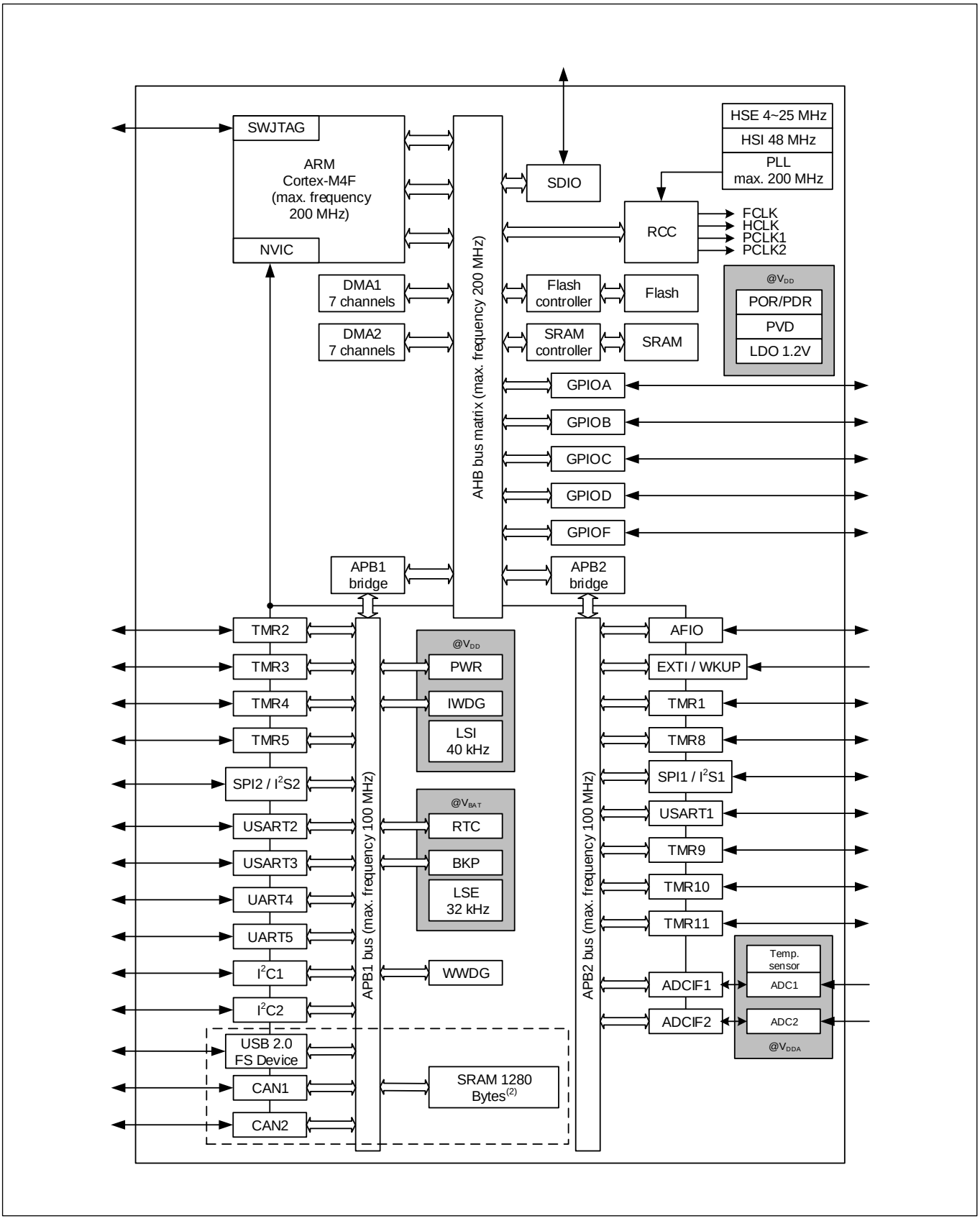
The ARM Cortex®-M4F with FPU 32-bit RISC processor features exceptional code efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the AT32F413 is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the AT32F413.

Note: Cortex®-M4F with FPU is binary compatible with Cortex®-M3.

Figure 1. AT32F413 block diagram(1)



(1) Operating temperatures: -40 to +105 °C. Junction temperature reaches 125 °C.
(2) USB and CANs share dedicated 1280-Byte SRAM configurable as four options:
- USB: 1280 Bytes;
- USB: 1024 Bytes, CAN1: 256 Bytes;
- USB: 1024 Bytes, CAN2: 256 Bytes;
- USB: 768 Bytes, CAN1: 256 Bytes, CAN2: 256 Bytes.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.3 Flash memory

Up to 256 Kbytes of embedded Flash is available for storing programs and data. User can configure any part of the embedded Flash memory protected by the sLib, functioning as a security area with code-excutable only but non-readable. sLib is a mechanism that protects the intelligence of solution venders and facilitates the second-level development by customers.

The AT32F413 provides extra interface called SPIM (SPI memory), which interfaces the external SPI Flash memory storing programs and data. With maximum 16 MBytes addressing capability, SPIM can be used as an extensive Flash memory Bank 3. SPIM additionally exists encryption to protect contents inside, enabling through the option bytes and determining the encryption area through a control register.

2.2.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

2.2.5 Embedded SRAM

Up to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.6 Nested vectored interrupt controller (NVIC)

The AT32F413 embed a nested vectored interrupt controller able to manage 16 priority levels and handle up to 63 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4F.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.7 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

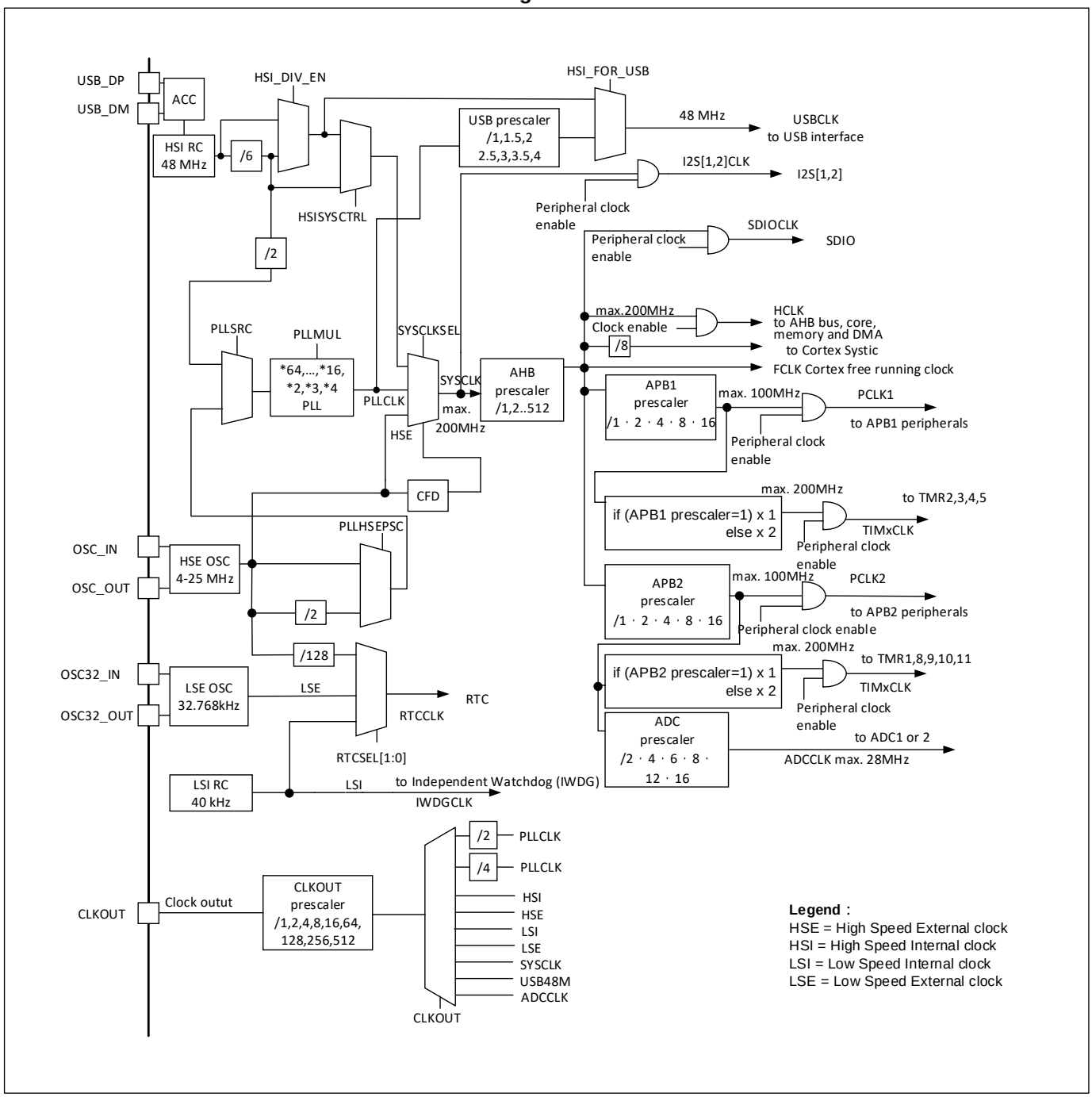
2.2.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 48 MHz oscillator (HSI) through a divided-by-6 divider (8 MHz) is selected as default CPU clock on reset. An external 4 to 25 MHz clock (HSE) can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 200 MHz. The maximum allowed frequency of the APB domains are 100 MHz. See *Figure 2* for details on the clock tree.

The AT32F413 embeded an automatic clock calibration (ACC) block, which calibrates the internal RC 48 MHz oscillator. This assures the most precise accuracy of the HSI in the full ragne of the operating temperatures.

Figure 2. Clock tree



(1) When using USB function and its clock source is from PLL, CPU frequency must be 48 MHz, 72 MHz, 96 MHz, 120 MHz, 144 MHz, or 192 MHz; when its clock source is direct from HSI 48 MHz, CPU frequency can be any frequency from 48 MHz to 192 MHz.

2.2.9 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is stored in system memory. It is used to reprogram the Flash memory through USART1, USART2, or USB. If configuring SPIM_IO0/1 pins on USB pins, the Flash memory Bank 3 cannot be reprogrammed through USB. *Table 3* provides the supporting interfaces of the Bootloader to different AT32F413 part numbers and pin configurations.

Table 3. The Bootloader supporting part numbers and pin configurations

Interface	Pin
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX(1) PA3: USART2_RX(1)
USB	PA11: USB_DM PA12: USB_DP

(1) Note that pins used are not 5 V tolerant.

2.2.10 Power supply schemes

- V_{DD} = 2.6～3.6 V: external power supply for I/Os and the internal regulator provided externally through V_{DD} pins.
- V_{DDA} = 2.6～3.6 V: external analog power supplies for ADC. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8～3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more detail on how to connect power pins, refer to *Figure 10.*

2.2.11 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 11* for the characteristic values of $V_{POR/PDR}$ and V_{PVD}.

2.2.12 Voltage regulator

The regulator has two operation modes: main (MR) and power down.

- Main mode (MR) is used in the nominal regulation mode (Run) and in the Stop mode
- Power down mode is used in Standby mode: the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption of the regulator (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.2.13 Low-power modes

The AT32F413 supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator is put in normal mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, or the USB wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.14 Direct Memory Access Controller (DMA)

The flexible 14-channel general-purpose DMAs (7 channels for DMA1 and 7 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and advanced-control timers TMRx, I^2S, SDIO, and ADC.

2.2.15 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied with V_{DD}. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator, or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using a divied-by-64 output of TAMPER pin to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.16 Timers and watchdogs

The AT32F413 devices include up to 2 advanced-control timers, up to 7 general-purpose timers, 2 watchdog timers, and a SysTick timer.

The table below compares the features of the advanced-control, general-purpose, and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TMR1, TMR8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TMR2, TMR5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR3, TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR9	16-bit	Up	Any integer between 1 and 65536	No	2	No
TMR10, TMR11	16-bit	Up	Any integer between 1 and 65536	No	1	No

Advanced-control timers (TMR1 and TMR8)

The two advanced-control timers (TMR1 and TMR8) can each be seen a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR timers which have the same architecture. The advanced-control timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

General-purpose timers (TMRx)

There are 7 synchronizable general-purpose timers embedded in the AT32F413.

- **TMR2, TMR3, TMR4, and TMR5**

  The AT32F413 has 4 full- featured general-purpose timers: TMR2, TMR3, TMR4, and TMR5.The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16- bit auto-reload up/down counter and a 16-bit prescaler. They all feature four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs.

  The TMR2, TMR3, TMR4, and TMR5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers via the link feature for synchronization or event chaining. In debug mode, their counter can be frozen. Any of these general-purpose timers can be used to generate PWM outputs.

  The TMR2, TMR3, TMR4, and TMR5 are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TMR9**

  TMR9 is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-pulse mode output. It can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. It can also be used as simple time base.

- **TMR10 and TMR11**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when

a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.17 Inter-integrated-circuit interface (I^2C)

Two I^2C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.18 Universal synchronous/asynchronous receiver transmitters (USART)

The AT32F413 embeds 3 universal synchronous/asynchronous receiver transmitters (USART1, USART2, and USART3) and 2 universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability.

These five interfaces are able to communicate at speeds of up to 6.25 Mbit/s.

USART1, USART2, and USART3 provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.2.19 Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 50 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC modes.

Both SPIs can be served by the DMA controller.

2.2.20 Inter-integrated sound interface (I^2S)

Two standard I^2S interfaces (multiplexed with SPI) are available, that can be operated in master or slave mode in half-duplex mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.2.21 Secure digital input/output interface (SDIO)

One SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different data bus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different data bus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC/eMMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.22 Controller area network (CAN)

Two CANs are compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.2.23 Universal serial bus (USB)

AT32F413 embeds a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL or direct from the 48 MHz HSI.

2.2.24 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked, if needed, in order to avoid spurious writing to the I/Os registers by following a specific sequence.

2.2.25 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 5*; it shows the list of remappable alternate functions and the pins onto

which they can be remapped. See the AT32F413 reference manual for software considerations.

2.2.26 Analog to digital converter (ADC)

Two 12-bit analog-to-digital converters are embedded into AT32F413 devices and they share up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hole
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced-control timers (TMR1 and TMR8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.2.27 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.6 V ≤ V_{DDA} ≤ 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.28 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure 3. AT32F413 LQFP64 pinout

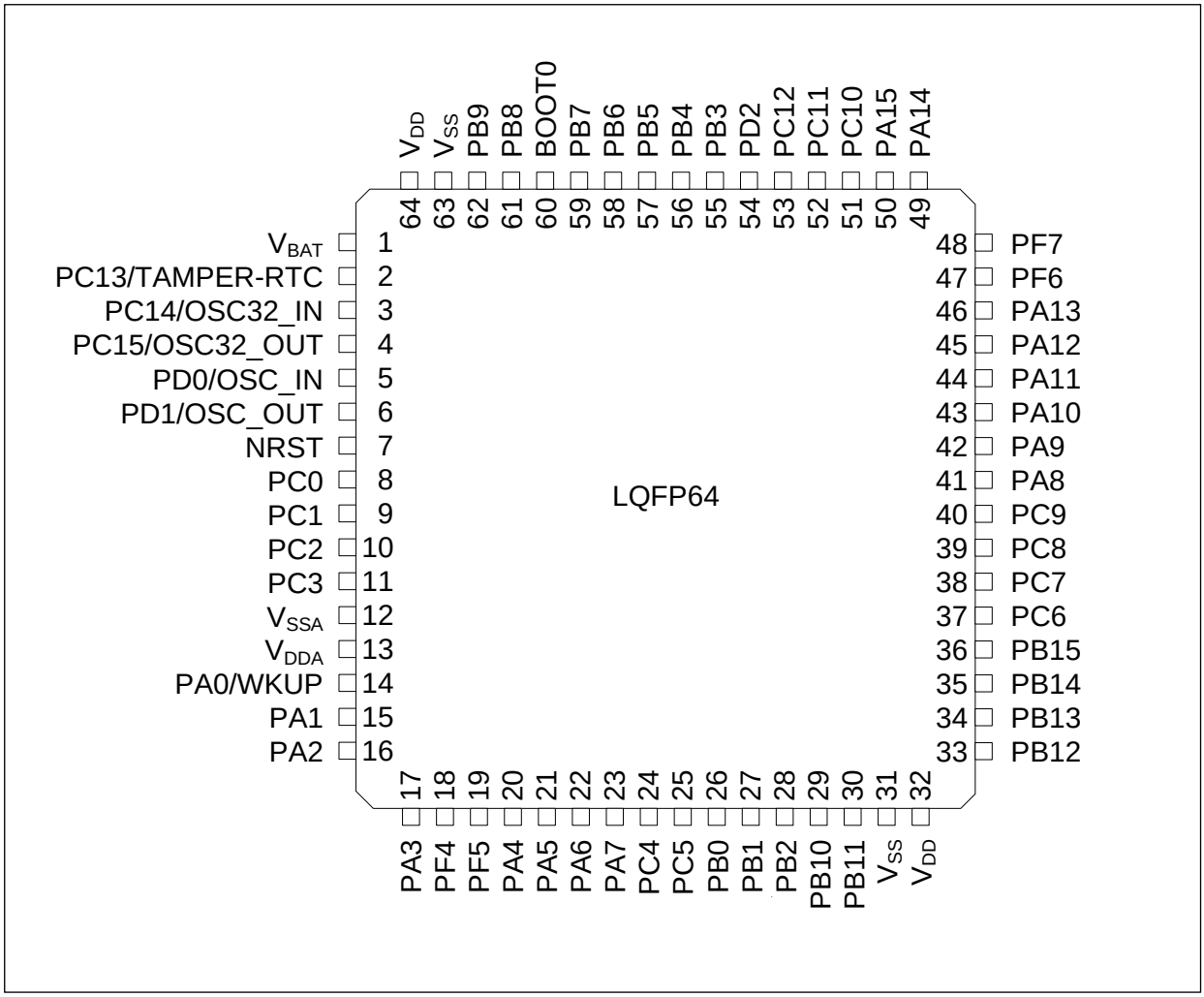


Figure 4. AT32F413 LQFP48 pinout

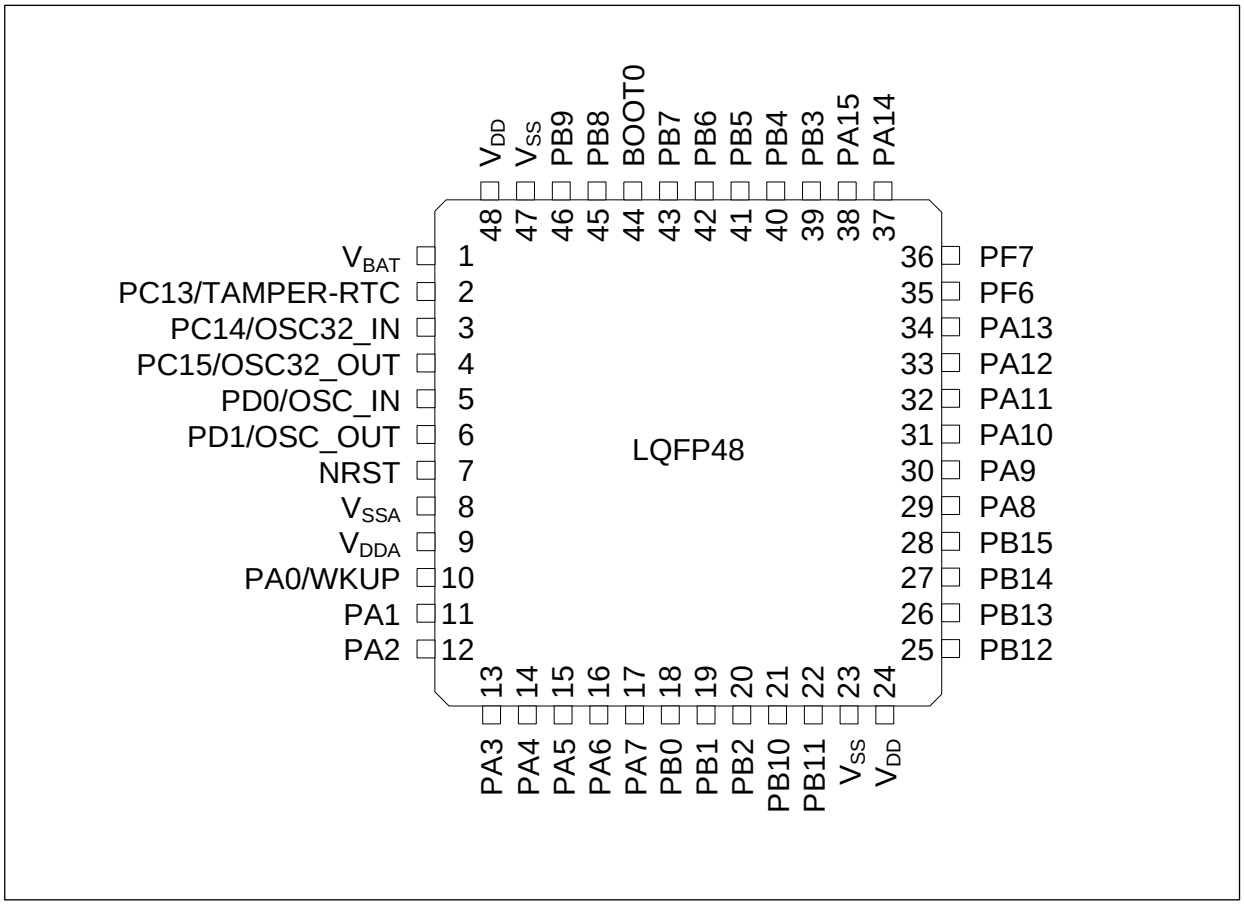


Figure 5. AT32F413 QFN48 pinout

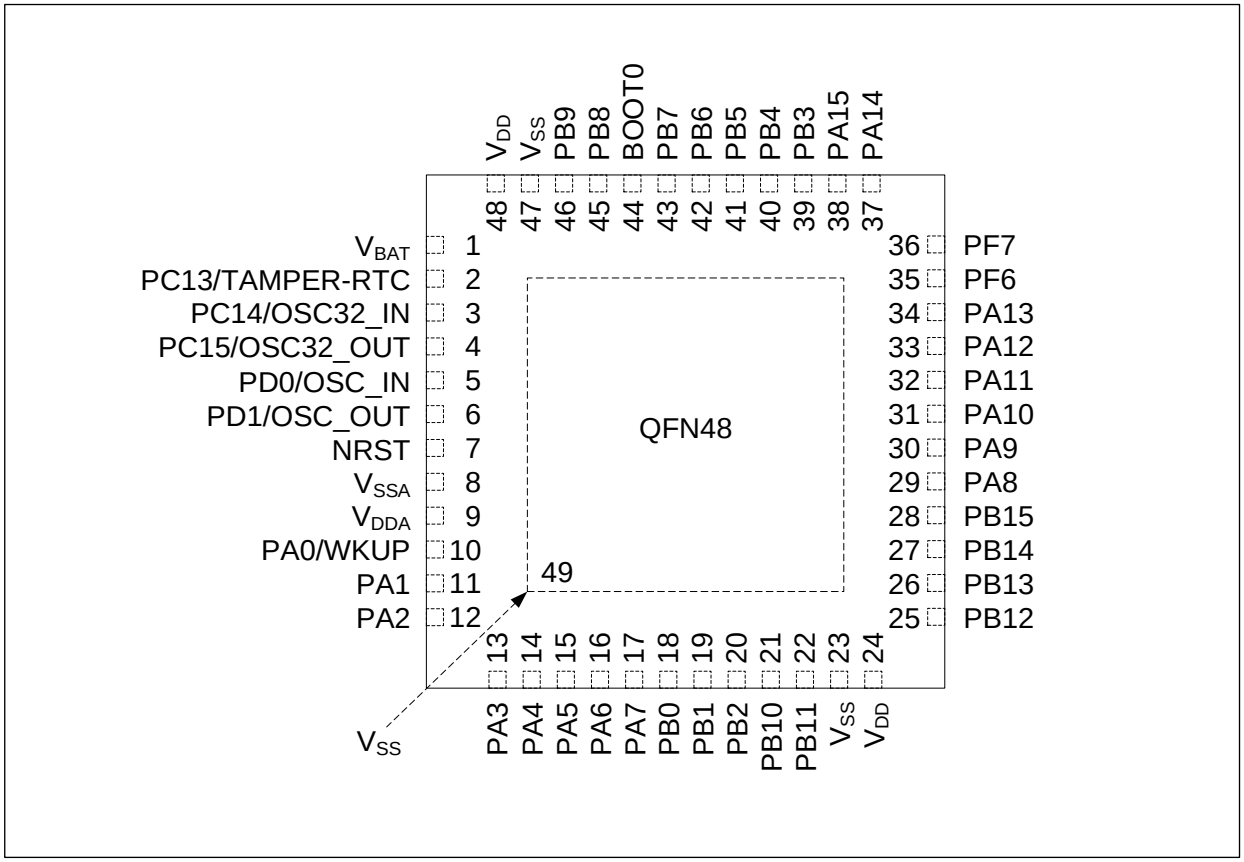
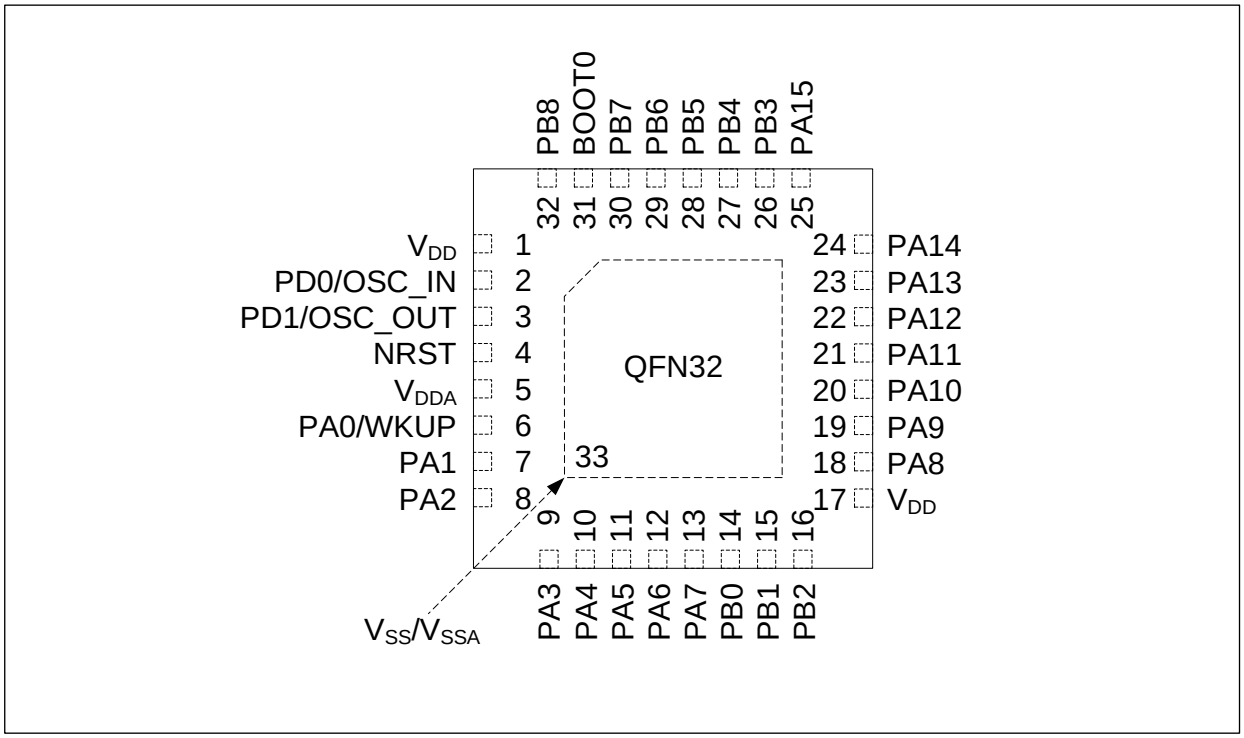


Figure 6. AT32F413 QFN32 pinout



The table below is the pin definition of the AT32F413. ”-” presents there is no such pinout on the related package. The multi-functions list follows priority from high to low. In principle, the analog signals have higher priority than the digital signals, and the digital output signals have higher priority than the digital input signals.

Table 5. AT32F413 series pin definitions

Pin number			Pin name	Type(1)	IO level(2)	Main function(3)	Alternate functions (4)	
QFN32	LQFP48 / QFN48	LQFP64					Default	Remap
-	1	1	V_{BAT}	S	-	V_{BAT}	-	-
-	2	2	PC13(4)	I/O	-	PC13	TAMPER-RTC(5)	-
-	3	3	PC14(4)	I/O	-	PC14	OSC32_IN(5)	-
-	4	4	PC15(4)	I/O	-	PC15	OSC32_OUT(5)	-
2	5	5	PD0(6)	I/O	-	OSC_IN	OSC_IN	PD0
3	6	6	PD1(6)	I/O	-	OSC_OUT	OSC_OUT	PD1
4	7	7	NRST	I/O	-	NRST	-	-
-	-	8	PC0	I/O	-	PC0	ADC12_IN10	SDIO_D0
-	-	9	PC1	I/O	-	PC1	ADC12_IN11	SDIO_D1
-	-	10	PC2	I/O	-	PC2	ADC12_IN12	SDIO_D2
-	-	11	PC3	I/O	-	PC3	ADC12_IN13	SDIO_D3
-	8	12	V_{SSA}	S	-	V_{SSA}	-	-
5	9	13	V_{DDA}	S	-	V_{DDA}	-	-
6	10	14	PA0-WKUP	I/O	-	PA0	ADC12_IN0 / WKUP / USART2_CTS / TMR2_CH1(7) / TMR2_ETR(7) / TMR5_CH1(7) / TMR8_ETR	-
7	11	15	PA1	I/O	-	PA1	ADC12_IN1 / USART2_RTS / TMR2_CH2(7) / TMR5_CH2(7)	-
8	12	16	PA2	I/O	-	PA2	ADC12_IN2 / USART2_TX / TMR2_CH3(7) / TMR5_CH3 / TMR9_CH1(7) /	SDIO_CK
9	13	17	PA3	I/O	-	PA3	ADC12_IN3 / USART2_RX / TMR2_CH4(7) / TMR5_CH4 / TMR9_CH2(7)	SDIO_CMD
-	-	18	PF4	I/O	FT	PF4	-	UART4_TX / TMR5_CH1
-	-	19	PF5	I/O	FT	PF5	-	UART4_RX / TMR5_CH2
10	14	20	PA4	I/O	-	PA4	ADC12_IN4 / USART2_CK / SPI1_NSS(7) / I2S1_WS(7)	SDIO_D4 / SDIO_D0
11	15	21	PA5	I/O	-	PA5	ADC12_IN5 / SPI1_SCK(7) / I2S1_CK(7)	SDIO_D5 / SDIO_D1
12	16	22	PA6	I/O	-	PA6	ADC12_IN6 / SPI1_MISO(7) / TMR3_CH1(7) / TMR8_BKIN	SDIO_D6 / SDIO_D2 / TMR1_BKIN / TMR10_CH1
13	17	23	PA7	I/O	-	PA7	ADC12_IN7 / SPI1_MOSI(7) / I2S1_SD(7) / TMR3_CH2(7) / TMR8_CH1N	SDIO_D7 / SDIO_D3 / TMR1_CH1N / TMR11_CH1
-	-	24	PC4	I/O	-	PC4	ADC12_IN14	SDIO_CK
-	-	25	PC5	I/O	-	PC5	ADC12_IN15	SDIO_CMD

Pin number			Pin name	Type(1)	IO level(2)	Main function(3)	Alternate functions (4)	
QFN32	LQFP48 / QFN48	LQFP64					Default	Remap
14	18	26	PB0	I/O	-	PB0	ADC12_IN8 / I2S1_MCK(7) / TMR3_CH3(7) / TMR8_CH2N	TMR1_CH2N
15	19	27	PB1	I/O	-	PB1	ADC12_IN9 / SPIM_SCK / TMR3_CH4(7) / TMR8_CH3N	TMR1_CH3N
16	20	28	PB2	I/O	FT	PB2/ BOOT1	-	-
-	21	29	PB10	I/O	FT	PB10	I2C2_SCL(7) / USART3_TX(7)	SPIM_IO0 / TMR2_CH3
-	22	30	PB11	I/O	FT	PB11	I2C2_SDA(7) / USART3_RX(7)	SPIM_IO1 / TMR2_CH4
-	23	31	V_{SS}	S	-	V_{SS}	-	-
17	24	32	V_{DD}	S	-	V_{DD}	-	-
-	25	33	PB12	I/O	FT	PB12	USART3_CK(7) / I2C2_SMBA(7) / SPI2_NSS(7) / I2S2_WS(7) / CAN2_RX(7) / TMR1_BKIN(7)	-
-	26	34	PB13	I/O	FT	PB13	SPI2_SCK(7) / I2S2_CK(7) / USART3_CTS / CAN2_TX(7) / TMR1_CH1N(7) /	-
-	27	35	PB14	I/O	FT	PB14	USART3_RTS / SPI2_MISO(7) / TMR1_CH2N(7)	TMR9_CH1
-	28	36	PB15	I/O	FT	PB15	SPI2_MOSI(7) / I2S2_SD(7) / TMR1_CH3N(7) /	TMR9_CH2
-	-	37	PC6	I/O	FT	PC6	I2S2_MCK(7) / SDIO_D6 / TMR8_CH1	TMR3_CH1
-	-	38	PC7	I/O	FT	PC7	SDIO_D7 / TMR8_CH2	I2S2_MCK / TMR3_CH2
-	-	39	PC8	I/O	FT	PC8	SDIO_D0 / TMR8_CH3	TMR3_CH3
-	-	40	PC9	I/O	FT	PC9	SDIO_D1 / TMR8_CH4	I2C2_SDA / TMR3_CH4
18	29	41	PA8	I/O	FT	PA8	CLKOUT / USART1_CK / SPIM_NSS / USB_SOF / TMR1_CH1	I2C2_SCL
19	30	42	PA9	I/O	FT	PA9	USART1_TX(7) / TMR1_CH2	I2C2_SMBA
20	31	43	PA10	I/O	FT	PA10	USART1_RX(7) / TMR1_CH3	-
21	32	44	PA11	I/O	-	PA11	USB_DM / SPIM_IO0(7) / USART1_CTS / CAN1_RX(7) / TMR1_CH4	-
22	33	45	PA12	I/O	-	PA12	USB_DP / SPIM_IO1(7) / USART1_RTS / CAN1_TX(7) / TMR1_ETR	-
23	34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
-	35	47	PF6	I/O	FT	PF6	-	I2C1_SCL / I2C2_SCL
-	36	48	PF7	I/O	FT	PF7	-	I2C1_SDA / I2C2_SDA
24	37	49	PA14	I/O	FT	JTCK-SWCLK	-	PA14
25	38	50	PA15	I/O	FT	JTDI	-	PA15 / SPI1_NSS / I2S1_WS / SPI2_NSS / I2S2_WS TMR2_CH1 / TMR2_ETR /

Pin number			Pin name	Type(1)	IO level(2)	Main function(3)	Alternate functions (4)	
QFN32	LQFP48 / QFN48	LQFP64					Default	Remap
-	-	51	PC10	I/O	FT	PC10	UART4_TX(7) / SDIO_D2	USART3_TX
-	-	52	PC11	I/O	FT	PC11	UART4_RX(7) / SDIO_D3	USART3_RX
-	-	53	PC12	I/O	FT	PC12	UART5_TX / SDIO_CK	USART3_CK
-	-	54	PD2	I/O	FT	PD2	UART5_RX / SDIO_CMD / TMR3_ETR	-
26	39	55	PB3	I/O	FT	JTDO	-	PB3 / TRACESWO / SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / TMR2_CH2 /
27	40	56	PB4	I/O	FT	NJTRST	-	PB4 / SPI1_MISO / SPI2_MISO / I2C2_SDA / TMR3_CH1
28	41	57	PB5	I/O	-	PB5	I2C1_SMBA	SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / CAN2_RX / TMR3_CH2
29	42	58	PB6	I/O	FT	PB6	I2C1_SCL(7) / SPIM_IO3 / TMR4_CH1	USART1_TX / CAN2_TX / I2S1_MCK
30	43	59	PB7	I/O	FT	PB7	I2C1_SDA(7) / SPIM_IO2 / TMR4_CH2	USART1_RX
31	44	60	BOOT0	I	-	BOOT0	-	-
32	45	61	PB8	I/O	FT	PB8	TMR10_CH1(7) / SDIO_D4 / TMR4_CH3	I2C1_SCL / CAN1_RX
-	46	62	PB9	I/O	FT	PB9	TMR11_CH1(7) / SDIO_D5 / TMR4_CH4	I2C1_SDA / CAN1_TX
-	47	63	V_{SS}	S	-	V_{SS}	-	-
1	48	64	V_{DD}	S	-	V_{DD}	-	-
-	-/49	-	V_{SS}	S	-	V_{SS}	-	-
33	-	-	V_{SS}/V_{SSA}	S	-	V_{SS}/V_{SSA}	-	-

(1) I = input, O = output, S = supply.

(2) FT = 5 V-tolerant I/O.

(3) Function availability depends on the chosen device.

(4) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the normal sourcing/sinking strength should be used with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

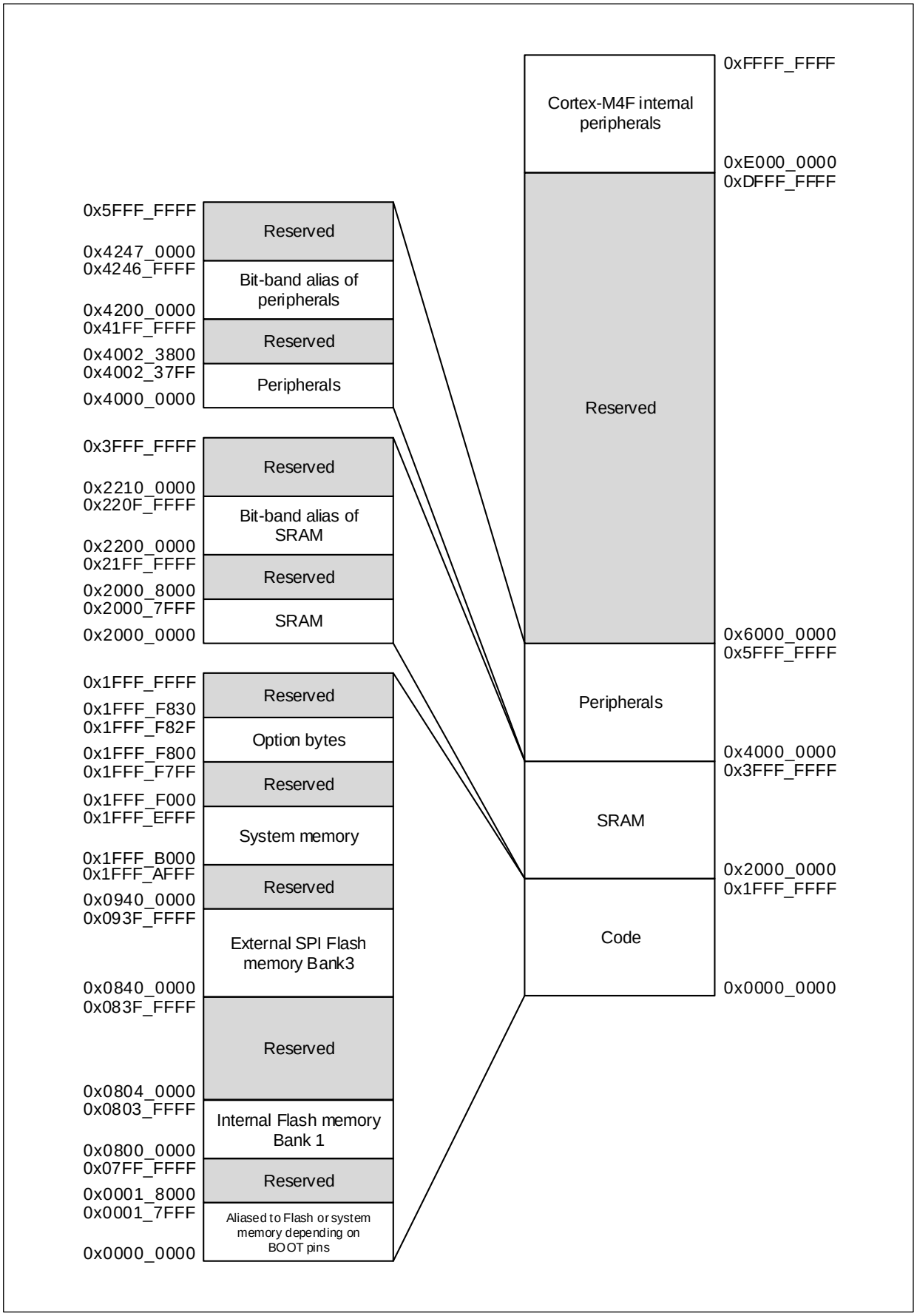
(5) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the AT32F413 reference manual.

(6) The pins number 5 and 6 (LQFP64, LQFP48, and QFN48), and the pins number 2 and 3 (QFN32) are configured as OSC_IN/OSC_OUT after reset, the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to Alternate function I/O and debug configuration section in the AT32F413 reference manual.

(7) This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the AT32F413 reference manual.

4 Memory mapping

Figure 7. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production with an ambient temperature at T_A = 25 °C and T_A = T_A max.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V. They are given only as design guidelines and are not tested.

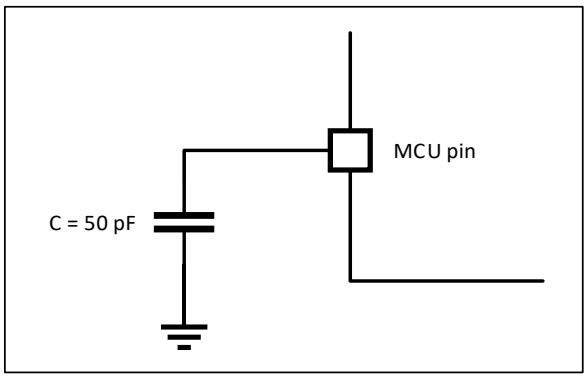
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

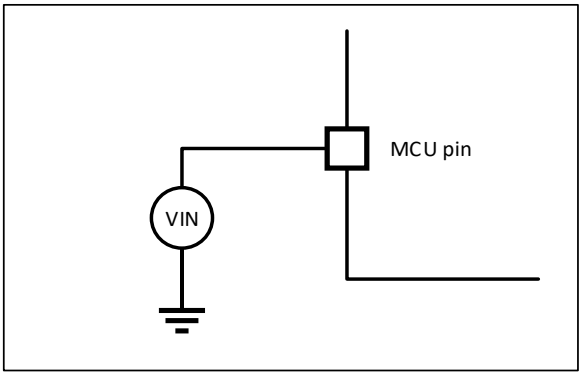
Figure 8. Pin loading conditions



5.1.5 Pin input voltage

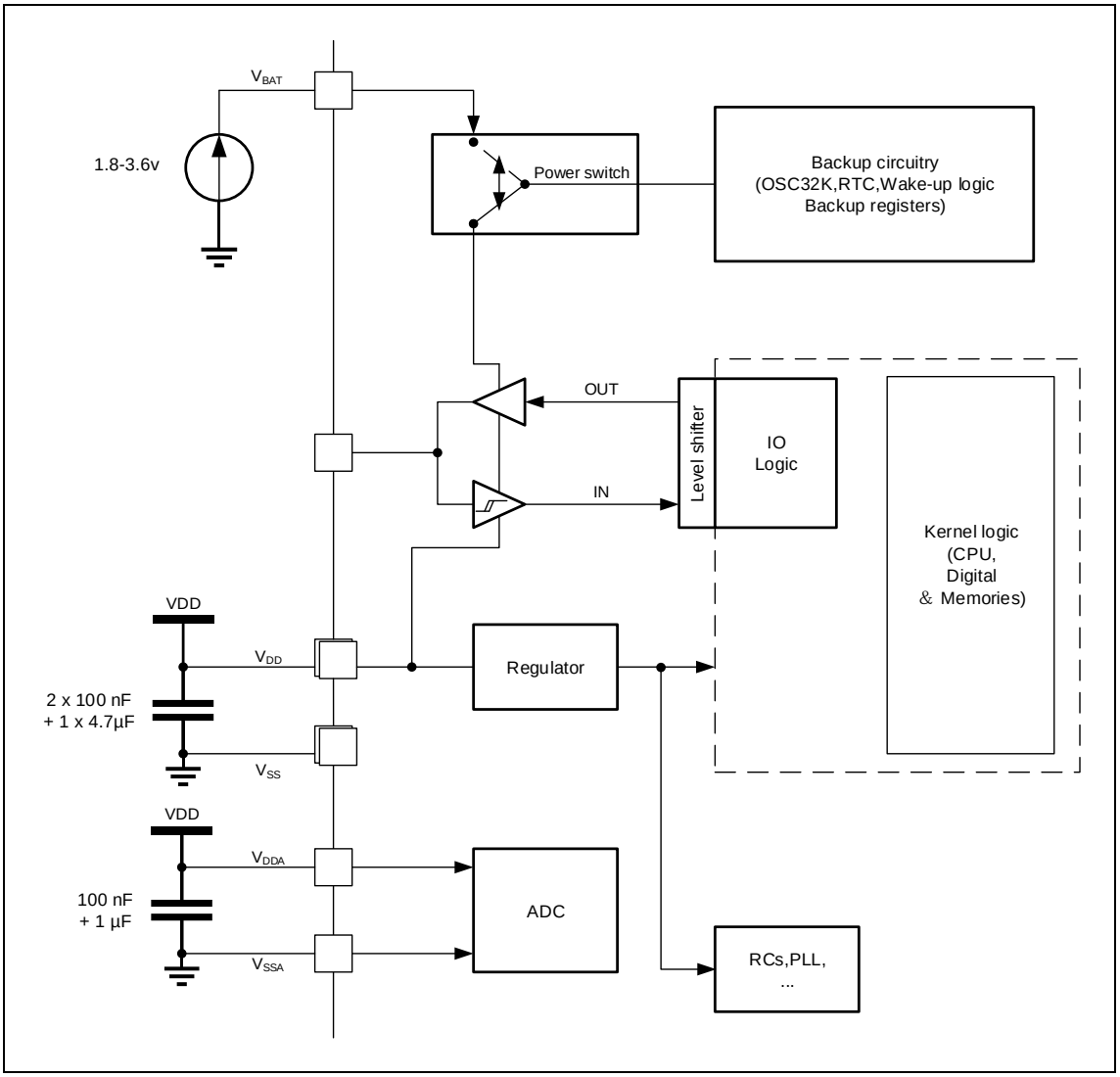
The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 9. Pin input voltage



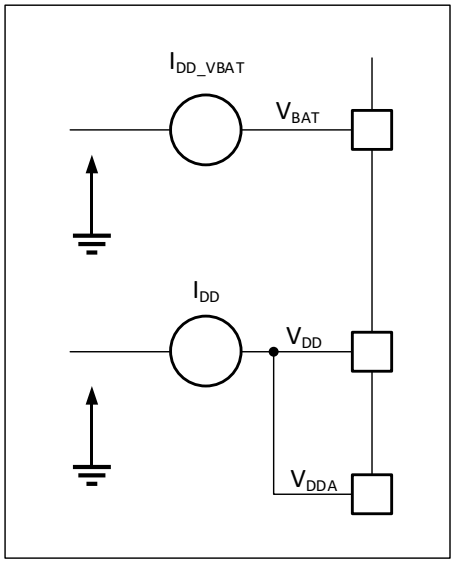
5.1.6 Power supply scheme

Figure 10. Power supply scheme



5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6*, *Table 7*, and *Table 8* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on FT I/Os	V_{SS}-0.3	6.0	
	Input voltage on other I/Os	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 7. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Bank 3 not used	0	200	MHz
		Bank 3 used	0	120	
f_{PCLK1}	Internal APB1 clock frequency	-	0	100	
f_{PCLK2}	Internal APB2 clock frequency	-	0	100	
V_{DD}	Standard operating voltage	-	2.6	3.6	V
V_{DDA}(1)	Analog operating voltage	Must be the same potential as V_{DD}(1)	2.6	3.6	V
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
P_D	Power dissipation: T_A = 105 °C	LQFP64	-	289	mW
		LQFP48	-	313	
		QFN48	-	394	
		QFN32	-	334	
T_A	Ambient temperature	-	-40	105	°C

(1) It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Operating conditions at power-up / power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in *Table 9*.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞(1)	ms/V
	V_{DD} fall time rate		20	∞	μs/V

(1) If V_{DD} rising time rate is slower than 80 ms/V, the code should access the backup registers after V_{DD} higher than V_{POR} + 0.1V.

5.3.3 Embedded reset and power control block characteristics

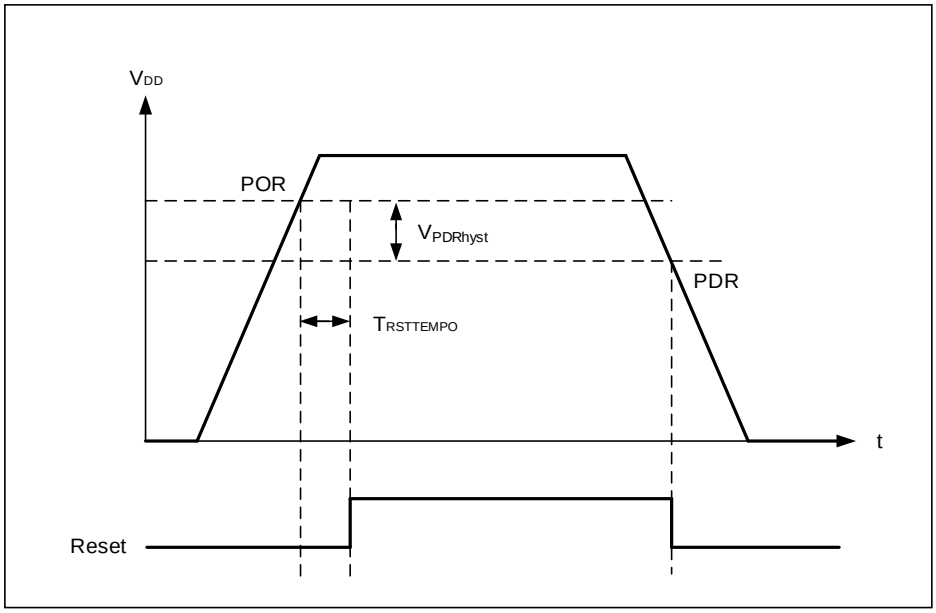
The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0] = 001 (rising edge)(1)	2.19	2.28	2.37	V
		PLS[2:0] = 001 (falling edge)(1)	2.09	2.18	2.27	V
		PLS[2:0] = 010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0] = 010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0] = 011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0] = 011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0] = 100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0] = 100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0] = 101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0] = 101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0] = 110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0] = 110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0] = 111 (rising edge)	2.76	2.88	3	V
		PLS[2:0] = 111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$(3)	Power on/power down reset threshold	Falling edge	1.8	2.0	2.25	V
		Rising edge	1.95	2.16	2.45	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	160	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	-	8	-	ms

(1) PLS[2:0] = 001 may be not available for its voltage detector level may be lower than $V_{POR/PDR}$.
(2) Guaranteed by design, not tested in production.
(3) The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

Figure 12. Power on reset/power down reset waveform



5.3.4 Embedded reference voltage

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
T_{Coeff}(2)	Temperature coefficient	-	-	-	120	ppm/°C

(1) Shortest sampling time can be determined in the application by multiple iterations.
(2) Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, and executed binary code.

The current consumption is measured as described in *Figure 11*.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled except when explicitly mentioned
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling
- When the peripherals are enabled:
  - $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$ if $f_{HCLK} > 100$ MHz
  - $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$ if $f_{HCLK} \leq 100$ MHz
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 13. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(2)	200 MHz	60.5	28.1	mA
			144 MHz	44.2	20.6	
			100 MHz	38.2	15.0	
			72 MHz	28.4	11.5	
			48 MHz	19.4	8.07	
			36 MHz	14.9	6.34	
			24 MHz	10.3	4.62	
			16 MHz	7.25	3.48	
			8 MHz	3.97	2.10	
			4 MHz	2.51	1.58	
			2 MHz	1.79	1.33	
			1 MHz	1.43	1.20	
			500 kHz	1.25	1.41	
			125 kHz	1.11	1.09	
		Running on high speed internal RC (HSI)	200 MHz	60.4	28.0	mA
			144 MHz	44.0	20.5	
			100 MHz	38.1	14.9	
			72 MHz	28.3	11.4	
			48 MHz	19.3	7.95	
			36 MHz	14.7	6.23	
			24 MHz	10.2	4.51	
			16 MHz	7.14	3.36	
			8 MHz	3.67	1.76	
			4 MHz	2.20	1.52	
			2 MHz	1.48	1.01	
			1 MHz	1.11	0.88	
			500 kHz	0.93	1.09	
			125 kHz	0.80	0.77	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(2) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Table 14. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(2)	200 MHz	48.3	6.51	mA
			144 MHz	35.3	5.02	
			100 MHz	32.1	4.16	
			72 MHz	23.9	3.73	
			48 MHz	16.4	2.89	
			36 MHz	12.6	2.46	
			24 MHz	8.79	2.04	
			16 MHz	6.26	1.77	
			8 MHz	3.29	1.07	
			4 MHz	2.08	0.98	
			2 MHz	1.48	0.93	
			1 MHz	1.18	0.91	
			500 kHz	1.03	0.90	
			125 kHz	0.92	0.89	
		Running on high speed internal RC (HSI)	200 MHz	48.2	6.40	mA
			144 MHz	35.2	4.90	
			100 MHz	31.9	4.05	
			72 MHz	23.8	3.61	
			48 MHz	16.3	2.76	
			36 MHz	12.5	2.34	
			24 MHz	8.67	1.92	
			16 MHz	6.14	1.64	
			8 MHz	3.17	0.95	
			4 MHz	1.96	0.85	
			2 MHz	1.35	0.80	
			1 MHz	1.05	0.78	
			500 kHz	0.90	0.77	
			125 kHz	0.79	0.76	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(2) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled except when explicitly mentioned
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling
- When the peripherals are enabled:
  - $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$ if $f_{HCLK} > 100$ MHz
  - $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$ if $f_{HCLK} \leq 100$ MHz

The parameters given in *Table 15* and *Table 16* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 15. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	200 MHz	69.1	mA
			144 MHz	52.0	
			100 MHz	46.0	
			72 MHz	35.6	
			48 MHz	26.2	
			36 MHz	21.4	
			24 MHz	16.7	
			16 MHz	13.5	
			8 MHz	10.1	
		External clock(2), all peripherals disabled	200 MHz	34.5	mA
			144 MHz	26.8	
			100 MHz	21.1	
			72 MHz	17.5	
			48 MHz	14.0	
			36 MHz	12.3	
			24 MHz	10.6	
			16 MHz	9.40	
			8 MHz	8.02	

(1) Guaranteed by characterization results, not tested in production.
(2) External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 16. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	200 MHz	56.5	mA
			144 MHz	42.8	
			100 MHz	39.6	
			72 MHz	31.0	
			48 MHz	23.1	
			36 MHz	19.1	
			24 MHz	15.1	
			16 MHz	12.4	
			8 MHz	9.32	
		External clock(2), all peripherals disabled	200 MHz	12.4	mA
			144 MHz	10.9	
			100 MHz	10.0	
			72 MHz	9.53	
			48 MHz	8.70	
			36 MHz	8.27	
			24 MHz	7.85	
			16 MHz	7.57	
			8 MHz	6.86	

(1) Guaranteed by characterization results, not tested in production.
(2) External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max(2)		Unit
			V_{DD}/V_{BAT} = 2.6 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	480	490	3800	6670	µA
	Supply current in Standby mode	Low-speed oscillator and RTC OFF	7.1	9.9	13.9	16.9	
		Low-speed oscillator and RTC ON	7.7	11.6	14.9	18.3	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 13. Typical current consumption in Stop mode vs. temperature at different V_{DD}

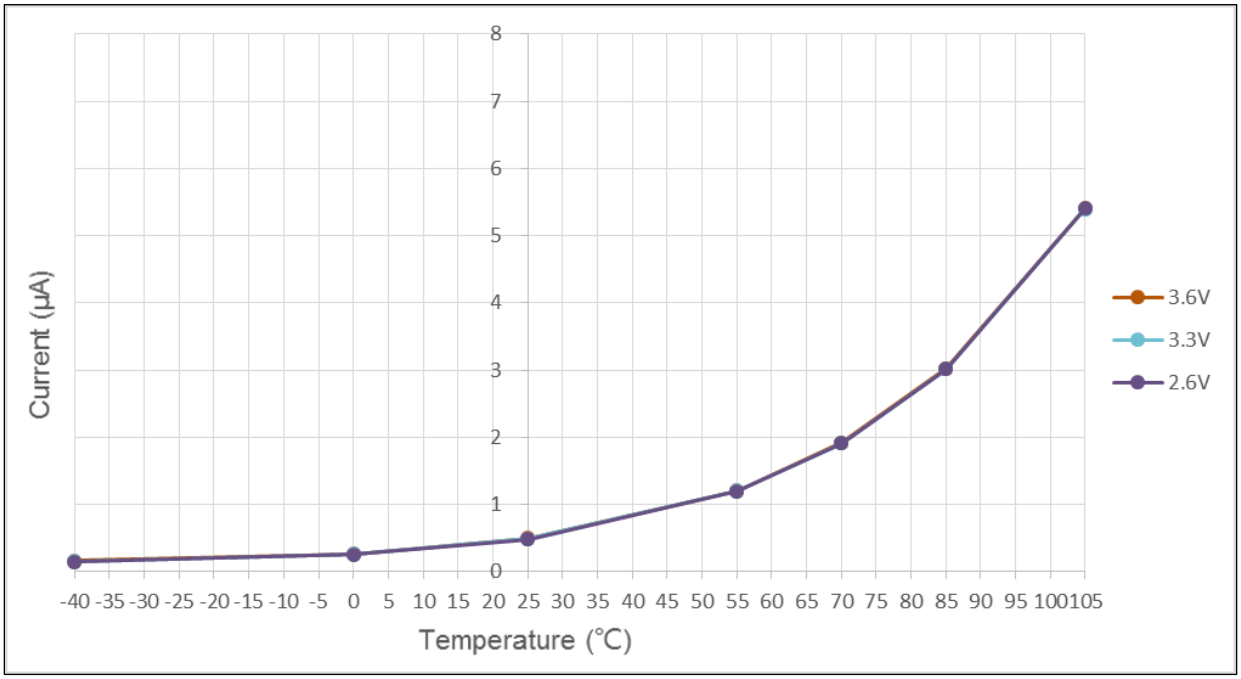


Figure 14. Typical current consumption in Standby mode vs. temperature at different V_{DD}

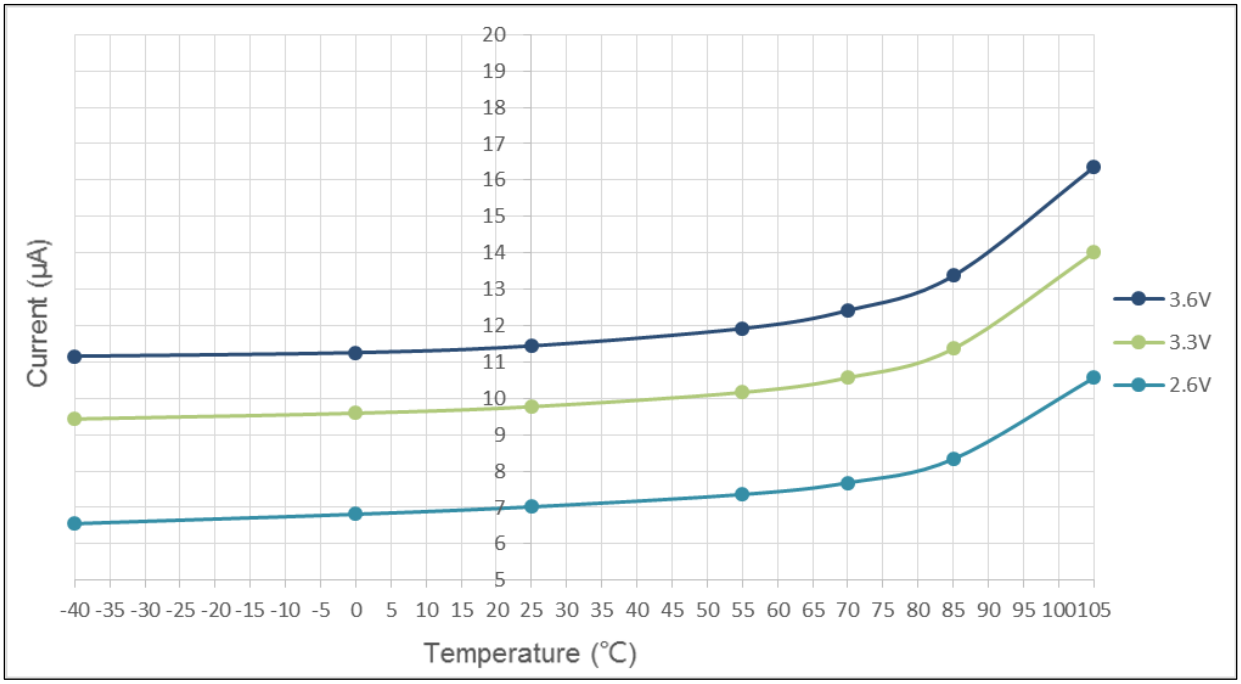
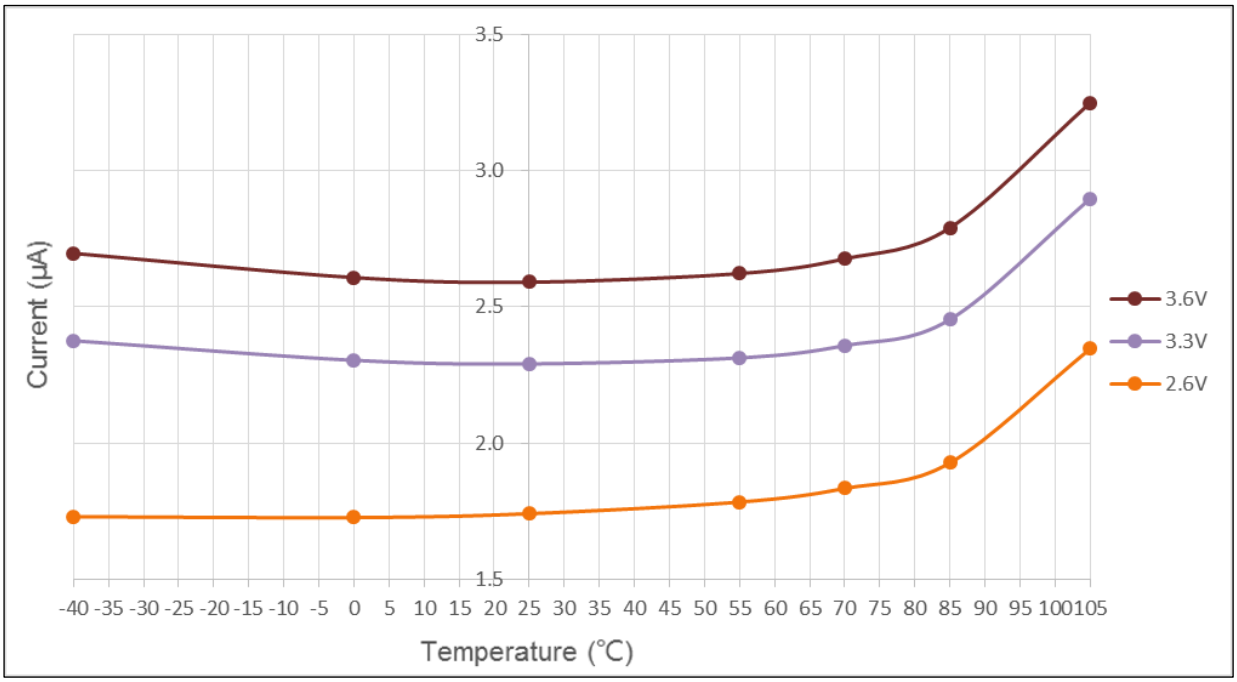


Table 18. Typical and maximum current consumptions on V_{BAT}

Symbol	Parameter	Conditions	Typ(1)			Max(2)		Unit
			V_{BAT} = 2.0 V	V_{BAT} = 2.6 V	V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Supply current of backup domain	Low-speed oscillator and RTC ON, $V_{DD} < V_{PDR}$	1.5	1.7	2.3	3.0	3.5	µA

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 15. Typical current consumption on V_{BAT} with LSE and RTC on vs. temperature at different V_{BAT}



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled except when explicitly mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 19. Peripheral current consumption

Peripheral		Typ	Unit
AHB (up to 200 MHz)	DMA1	9.45	μA/MHz
	DMA2	9.58	
	GPIOA	1.22	
	GPIOB	1.20	
	GPIOC	1.29	
	GPIOD	1.23	
	GPIOF	1.19	
	CRC	1.57	
	SDIO	18.5	
APB1 (up to 100 MHz)	TMR2	8.65	
	TMR3	6.50	
	TMR4	6.57	
	TMR5	8.76	
	SPI2/I^2S2	2.80	
	USART2	2.50	
	USART3	2.49	
	UART4	2.54	
	UART5	2.54	
	I^2C1	2.47	
	I^2C2	2.50	
	USB	6.76	
	CAN1	3.92	
	CAN2	3.91	
	WWDG	0.44	
	PWR	0.41	
	BKP	73.6	

Peripheral		Typ	Unit
APB2 (up to 100 MHz)	AFIO	2.13	μA/MHz
	SPI1/I^{2}S1	2.64	
	USART1	2.48	
	TMR1	9.23	
	TMR8	9.18	
	TMR9	3.80	
	TMR10	2.66	
	TMR11	2.62	
	ADC1	6.54	
	ADC2	6.35	
	ACC	0.97	

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

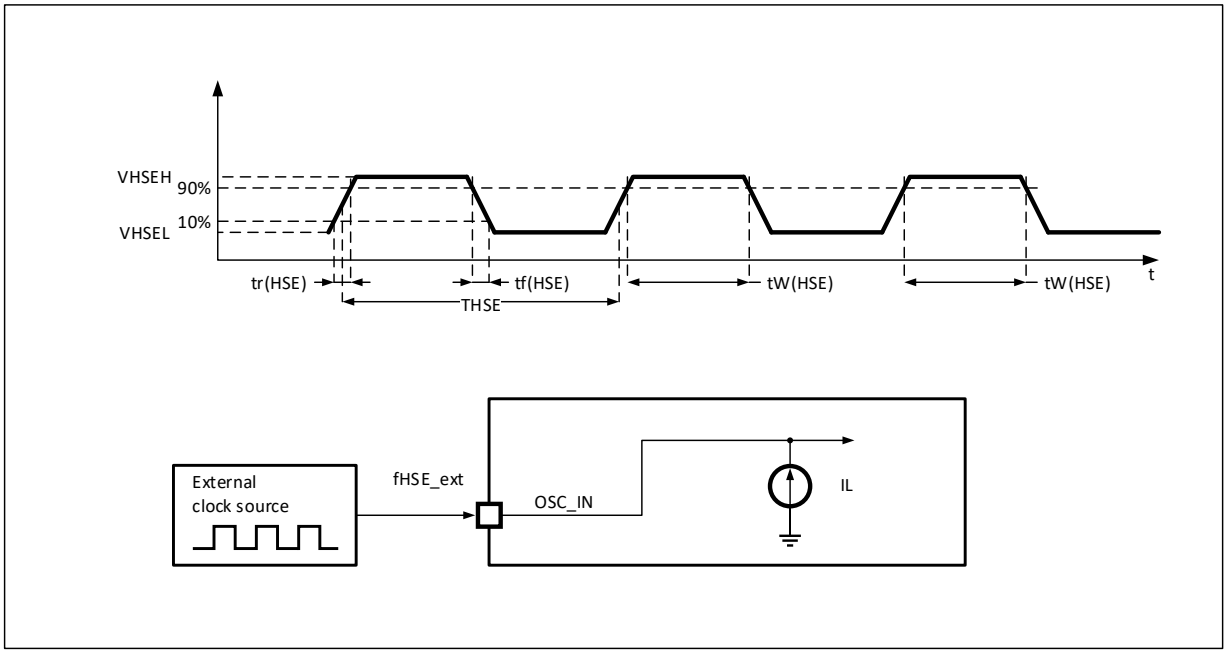
The characteristics given in the table below result from tests performed using a high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 16. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

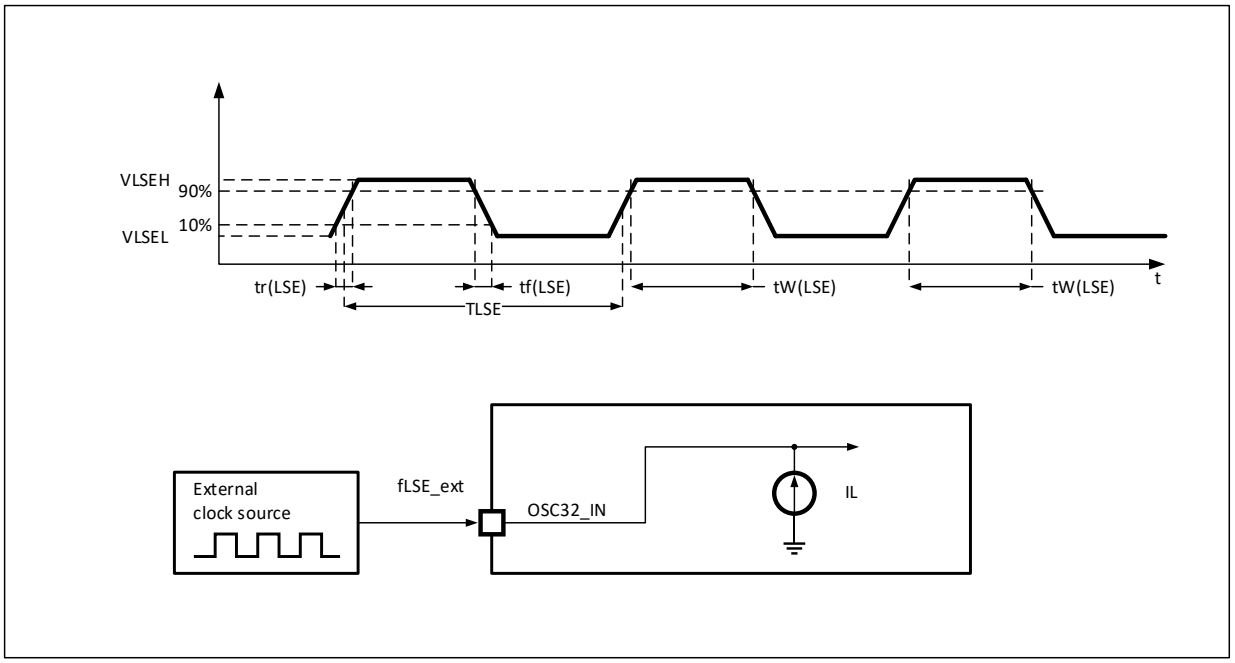
The characteristics given in the table below result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)	-	-	-	50	ns
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 17. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

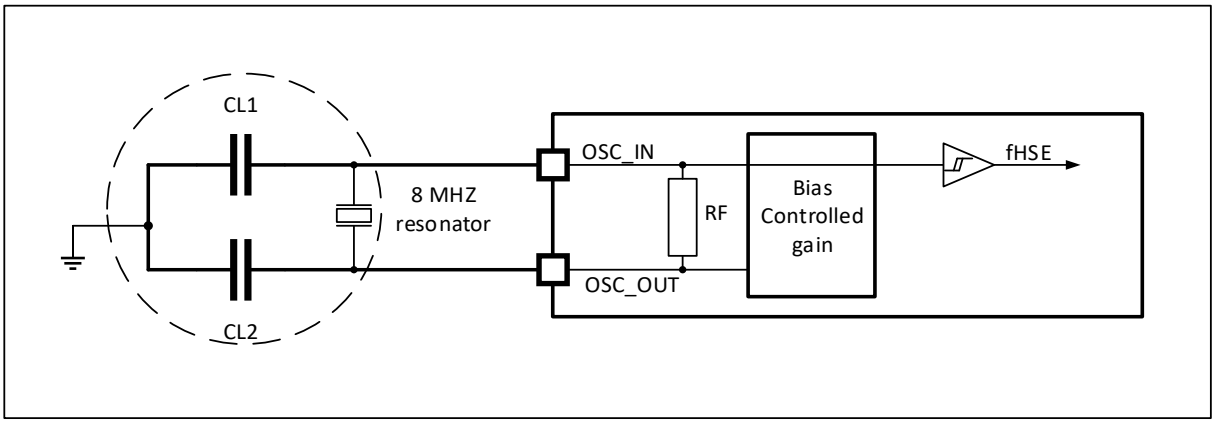
Table 22. HSE 4-25 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	1.2	-	ms

(1) Resonator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1}和C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 18. Typical application with an 8 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

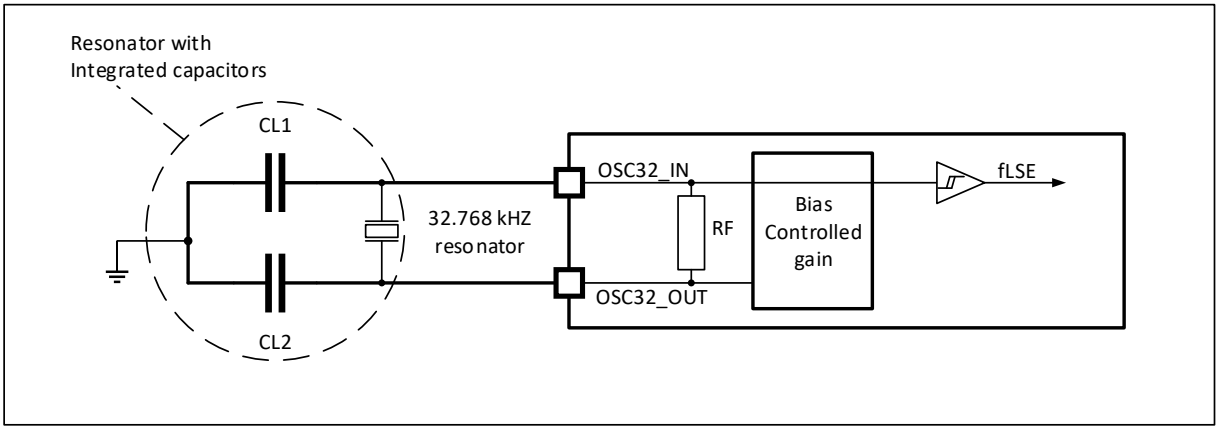
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LSE)}$	Startup time	V_{DD} is stabilized	-	150	-	ms

(1) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 19. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

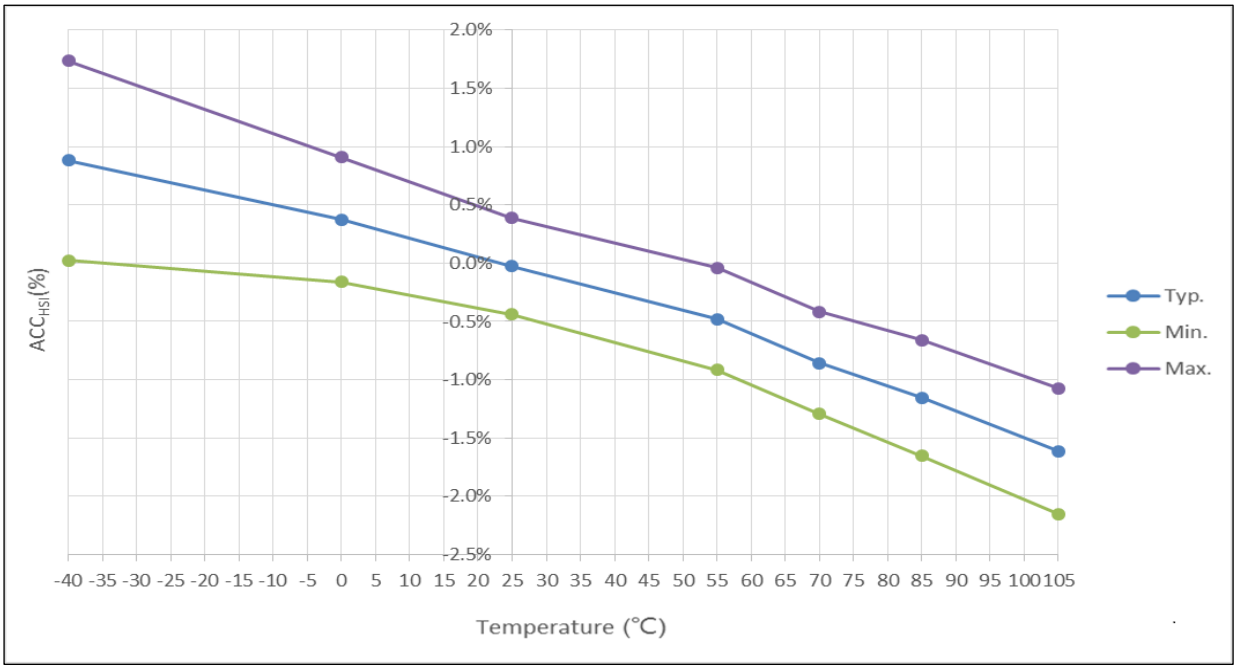
High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	48	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CTRL register		-	-	1(2)	%
		ACC-trimmed		-	-	0.25(2)	
		Factory-calibrated(3)	T_A = -40 ~ 105 °C	-2.5		2.5	%
			T_A = -40 ~ 85 °C	-2	-	2	
			T_A = 0 ~ 70 °C	-1.5	-	1.5	
			T_A = 25 °C	-1	-	1	
$t_{SU(HSI)}$(3)	HSI oscillator startup time	-		-	-	10	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-		-	190	200	µA

(1) V_{DD} = 3.3 V, T_A = -40~105 °C, unless otherwise specified.
(2) Guaranteed by design, not tested in production.
(3) Guaranteed by characterization results, not tested in production.

Figure 20. HSI oscillator frequency accuracy vs. temperature



Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	-	30	40	60	kHz

(1) V_{DD} = 3.3 V, T_A = -40 to 105 °C, unless otherwise specified.
(2) Guaranteed by characterization results, not tested in production.

5.3.8 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the HSI RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	3.3	μs
t_{WUSTOP}(1)	Wakeup from Stop mode	280	μs
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	3.6	ms

(1) The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.9 PLL characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	200	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by characterization results, not tested in production.
(2) Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.10 Memory characteristics

The characteristics in *Table 28* are given at T_A = 25 °C and V_{DD} = 3.3 V.

Table 28. Internal Flash memory characteristics

Symbol	Parameter	Conditions	Typ					Unit
			f_{HCLK}					
			200	144	72	48	8	MHz
T_{PROG}	Programming time	-	50					µs
t_{ERASE}	Page (2 KB) erase time	AT32F413xC	50					ms
	Page (1 KB) erase time	AT32F413xB AT32F413x8	40					
t_{ME}	Mass erase time	-	800					ms
I_{DD}	Supply current	Programming mode	27.5	20.1	11.1	7.8	1.8	mA
		Erase mode	35.3	26.9	16.9	13.1	6.4	

Table 29. Internal Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 30. EMS characteristics

Symb	Parameter	Conditions	Level/Class
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, HSE, f_{HCLK} = 200 MHz, conforms to IEC 61000-4-4	4A (4kV)
		V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, HSE, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	
		V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, HSI, f_{HCLK} = 200 MHz, conforms to IEC 61000-4-4	
		V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, HSI, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	
		V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, HSI, f_{HCLK} = 8 MHz, conforms to IEC 61000-4-4	

(1) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JS-001-2017/JS-002-2014 standard.

Table 31. ESD absolute maximum ratings

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	5000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2014	III	1000	

(1) Guaranteed by characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on 6 parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (200 mA)

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symb	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input(1) low level voltage	-	–0.3	-	0.28 * V_{DD} + 0.1	V
V_{IH}	Standard I/O input high level voltage	-	0.31 * V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT I/O input(1) high level voltage			-	5.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	FT I/O Schmitt trigger voltage hysteresis(2)		5% V_{DD}	-	-	
I_{lkg}	Input leakage current(3)	$V_{SS} \le V_{IN} \le V_{DD}$ standard I/Os(4)	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5V$ FT I/Os	-	-	±10	
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	60	70	100	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)(5)	$V_{IN} = V_{DD}$	70	80	120	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

(1) FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
(2) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(3) Leakage could be higher than max if negative current is injected on adjacent pins.
(4) Each of PA11 and PA12 has a weak pull-down resistor 330 kΩ which is permanently enabled.
(5) The pull-down resistor of BOOT0 exists permanently.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all I/Os on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
MDEx[1:0] = 11 (Maximum sourcing/sinking strength)					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 45 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
MDEx[1:0] = 01 (Large sourcing/sinking strength)					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 3 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 20 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	
MDEx[1:0] = 10 (Normal sourcing/sinking strength)					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage		V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage		2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage		V_{DD}-1.3	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Unless otherwise specified, the parameters given below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 35. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	10	-	ns

5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

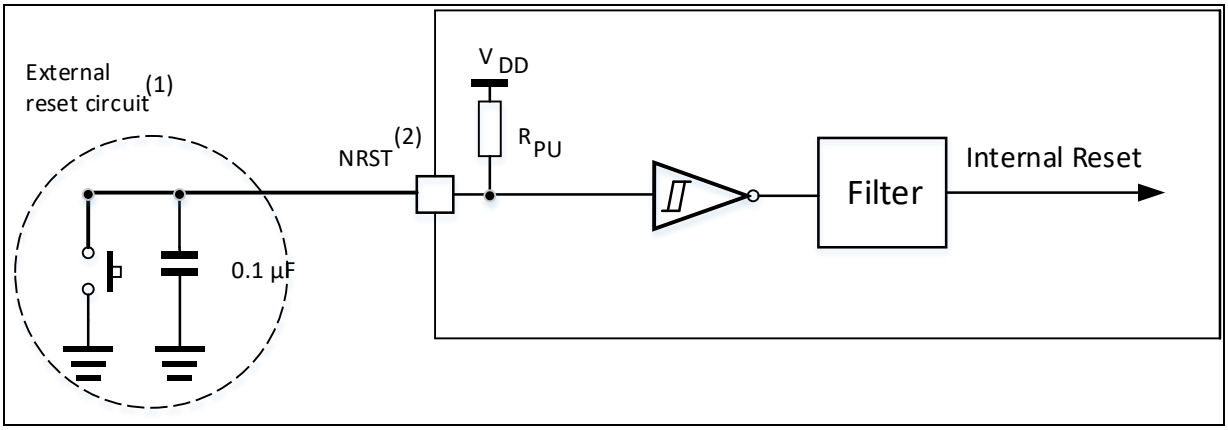
Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	500	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	25	33.3	μs
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	66.7	45	-	μs

(1) Guaranteed by design.

Figure 21. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the V_{IL} (NRST) max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

5.3.15 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to *5.3.13 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 37. TMRx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 200 MHz	5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz
				50	MHz

(1) TMRx is used as a general term to refer to the TMR1 to TMR5 and TMR8 to TMR11.

5.3.16 Communications interfaces

I²C interface characteristics

The AT32F413 I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL mapped to are not ”true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in the table below. Refer also to *5.3.13 I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 38. I²C characteristics

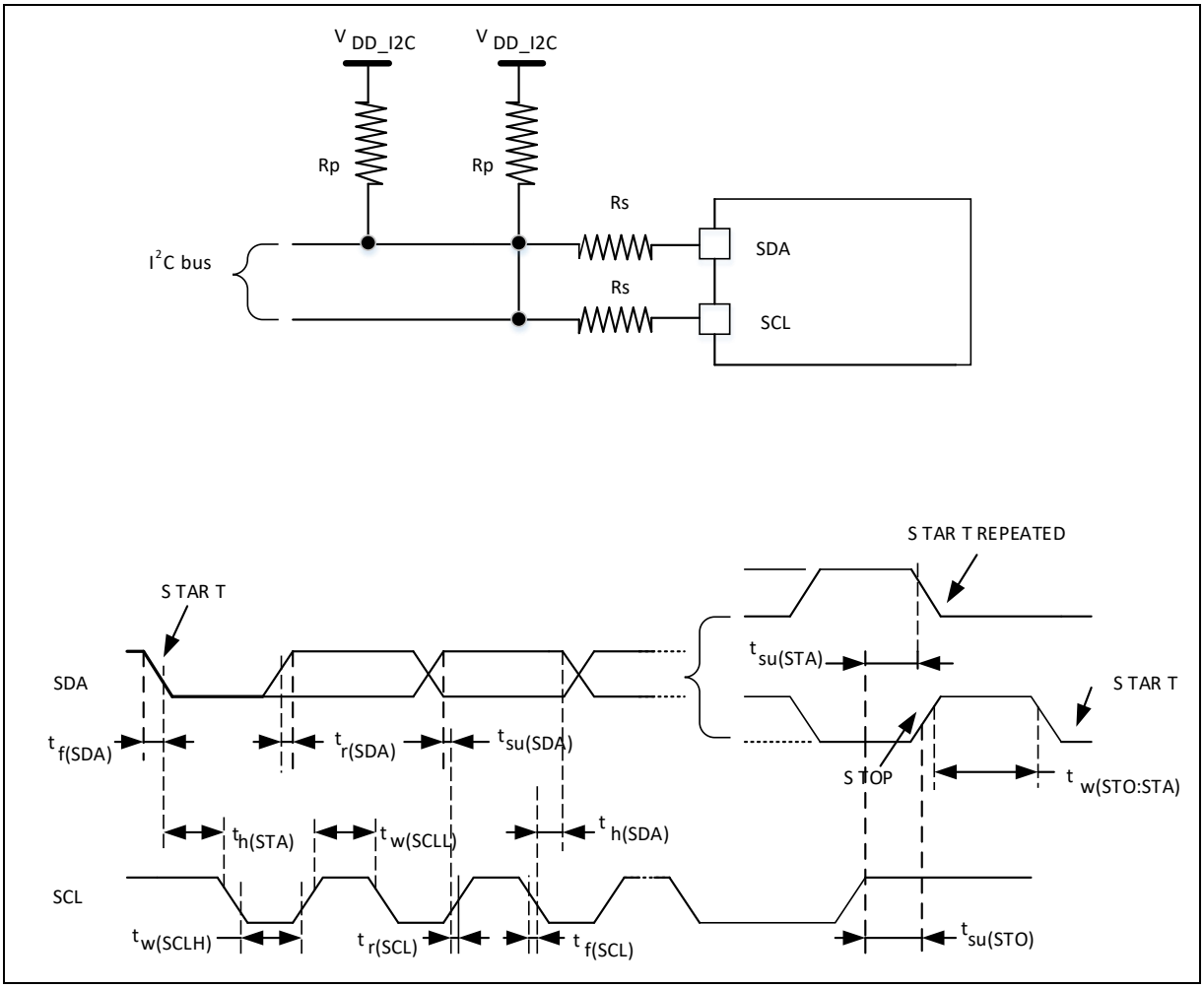
Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

(1) Guaranteed by design, not tested in production.

(2) f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve the fast mode I²C frequencies.

(3) The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.

Figure 22. I²C bus AC waveforms and measurement circuit(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 39. SCL frequency (f_{PCLK1} = 36 MHz, V_{DD} = 3.3 V)(1)(2)

f_{SCL}(kHz)	I2C_CLKCTRL value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

(1) R_P = External pull-up resistance, f_{SCL} = I²C speed.
(2) For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI-I²S and SPIM characteristics

Unless otherwise specified, the parameters given in *Table 40* for SPI and SPIM or in *Table 41* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *5.3.13 I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 40. SPI and SPIM characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	SPI1~4 master mode	-	50	MHz
		SPI1~4 slave mode	-	$f_{PCLK}/2$	
		SPIM	-	60	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 100 MHz, prescaler = 4	15	25	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{su(SI)}$(1)		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{h(SI)}$(1)		Slave mode	4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

(1) Guaranteed by characterization results, not tested in production.
(2) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(3) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 23. SPI timing diagram - slave mode and CPHA = 0

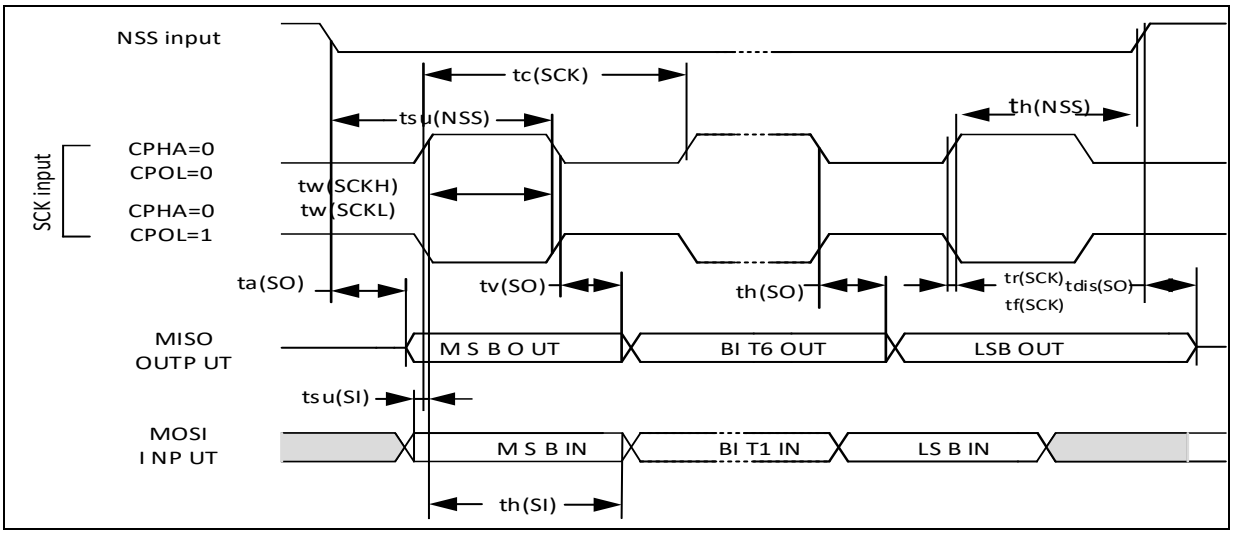
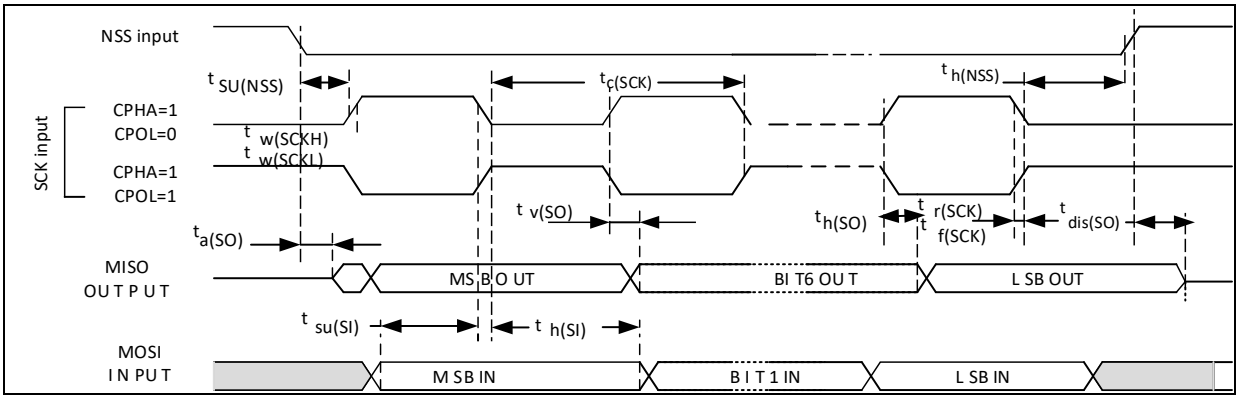
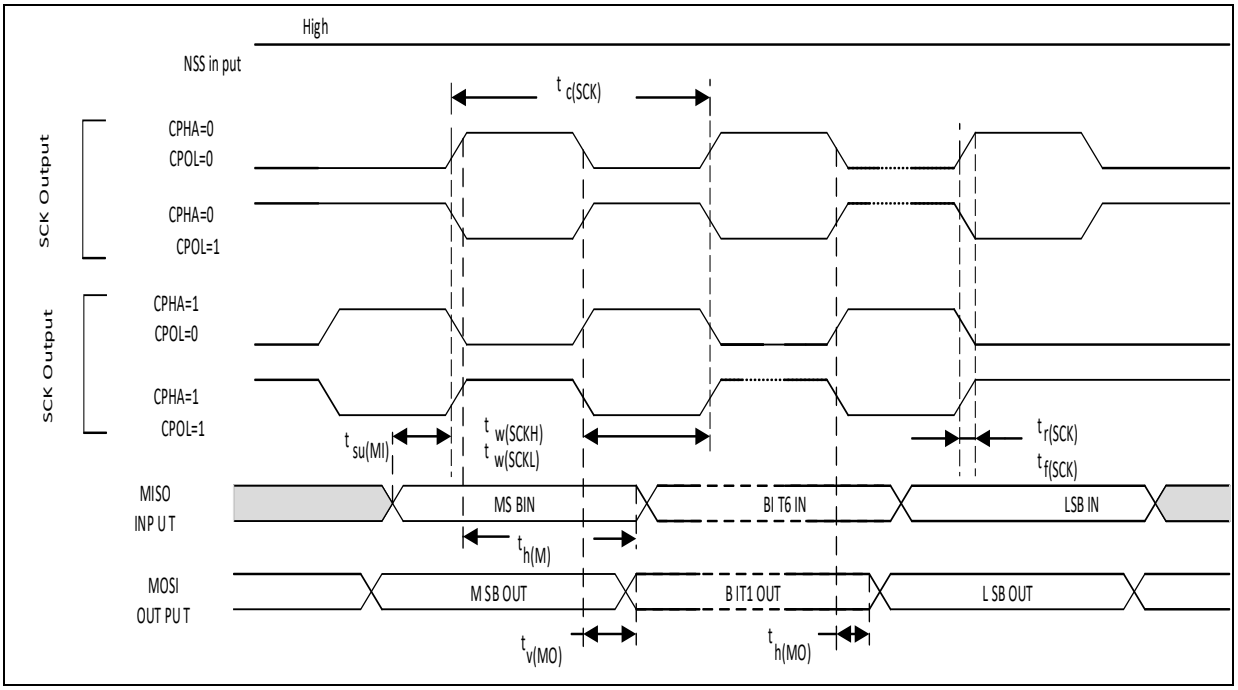


Figure 24. SPI timing diagram - slave mode and CPHA = 1(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 25. SPI timing diagram - master mode(1)



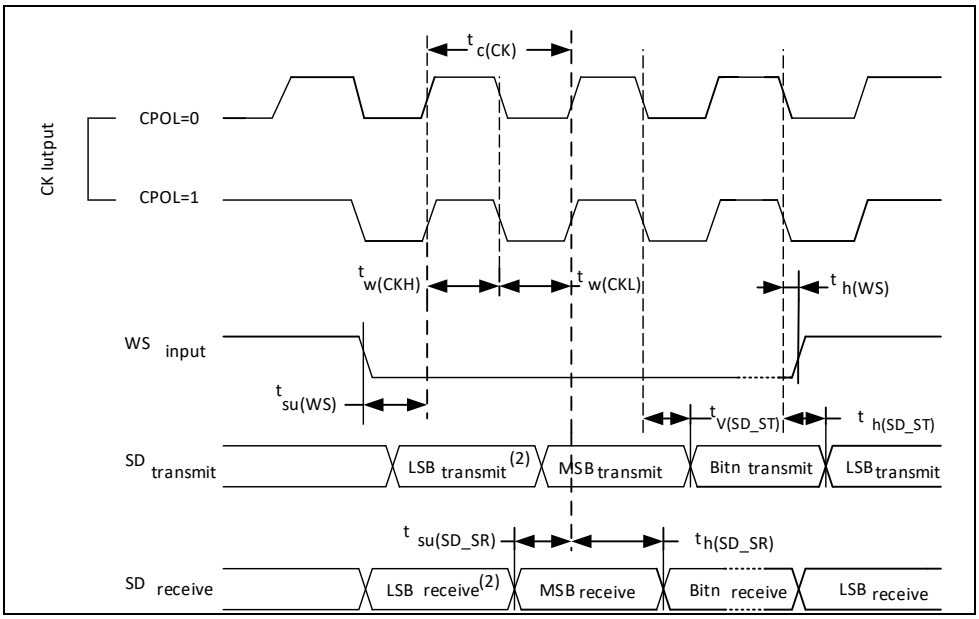
(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 41. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I²S clock frequency	Master mode (data: 16 bits, audio frequency = 48 kHz)	1.522	1.525	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 50 pF	-	8	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	3	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	2	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	4	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{w(CKH)}$(1)	CK high and low time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz	312.5	-	
$t_{w(CKL)}$(1)			345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6.5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	18	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	11	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

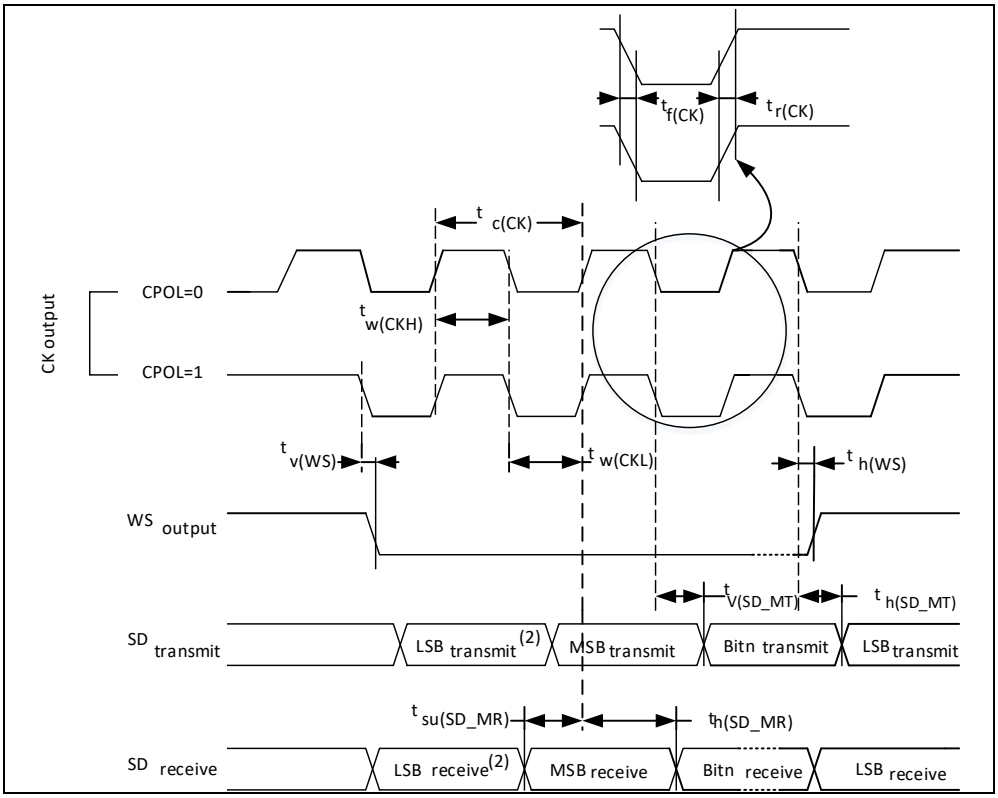
(1) Guaranteed by design and/or characterization results.
(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 26. I²S slave timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.
(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I²S master timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *5.3.13 I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 28. SDIO high-speed mode

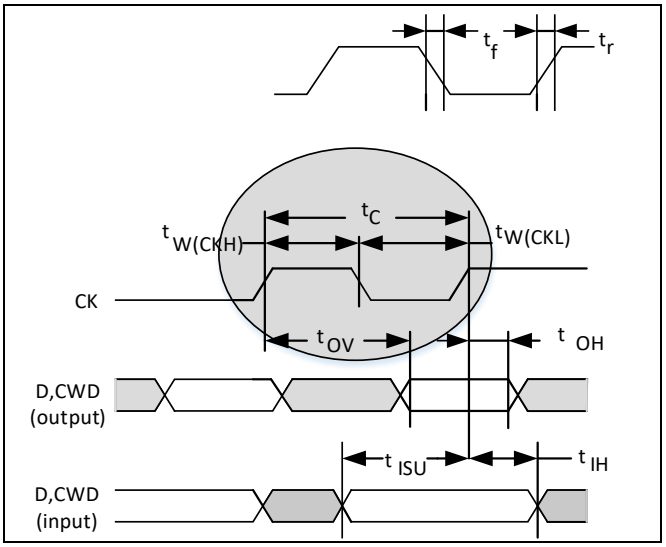


Figure 29. SD default mode

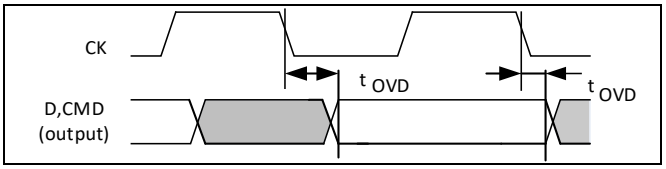


Table 42. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \le 30$ pF	0	48	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	$C_L \le 30$ pF	32	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 16 MHz	$C_L \le 30$ pF	30	-	
t_r	Clock rise time	$C_L \le 30$ pF	-	4	
t_f	Clock fall time	$C_L \le 30$ pF	-	5	
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \le 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \le 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \le 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \le 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \le 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \le 30$ pF	0.5	-	

(1) Refer to SDIO_CLKCTRL, the SDIO clock control register to control the CK output.

USB characteristics

Table 43. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

(1) Guaranteed by design, not tested in production.

Table 44. USB DC electrical characteristics

Symbol		Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels	V_{DD}	USB operating voltage	-	3.0(2)		3.6	V
	V_{DI}(3)	Differential input sensitivity	I (USB_DP, USB_DM)	0.2		-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8		2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3		2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8		3.6	
R_{PU}		USB_DP internal pull-up	V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ

(1) All the voltages are measured from the local ground potential.
(2) The AT32F413 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V V_{DD} voltage range.
(3) Guaranteed by characterization results, not tested in production.
(4) R_L is the load connected on the USB drivers.

Figure 30. USB timings: definition of data signal rise and fall time

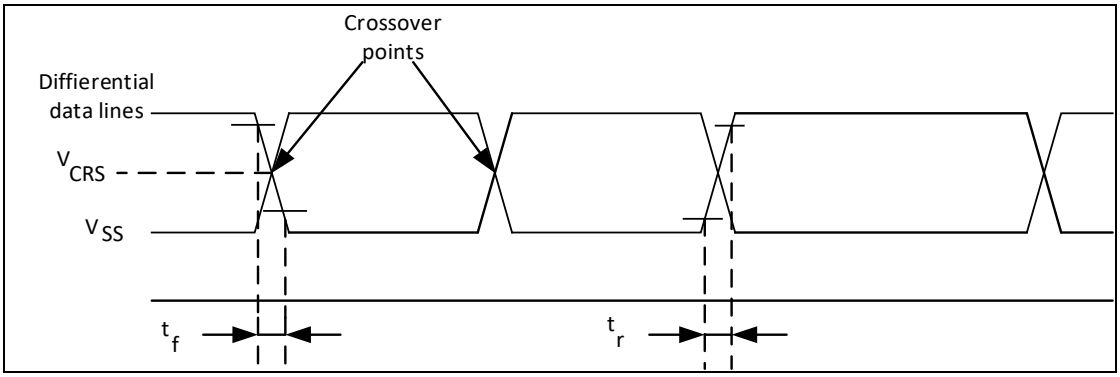


Table 45. USB full-speed electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
t_r	Rise time (2)	C_L ≤ 50 pF	4	20	ns
t_f	Fall Time (2)	C_L ≤ 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to *5.3.13 I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Table 46. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.6	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	790(1)	900	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(2)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-} tied to ground))	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table* 47 and *Table* 48 for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	15	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.14			μs
		-	172			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	μs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 46*.

Table 47 and *Table 48* are used to determine the maximum external impedance allowed for an error below 1/4 of LSB.

Table 47. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.2
7.5	0.54	1.0
13.5	0.96	2.0
28.5	2.04	4.2
41.5	2.96	6.0
55.5	3.96	8.5
71.5	5.11	11
239.5	17.11	32

(1) Guaranteed by design.

Table 48. R_{AIN} max for f_{ADC} = 28 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	0.4
13.5	0.48	0.9
28.5	1.02	2.1
41.5	1.48	3.0
55.5	1.98	4.0
71.5	2.55	5.0
239.5	8.55	19

(1) Guaranteed by design.

Table 49. ADC accuracy (V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C)(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C Measurements made after ADC calibration	±2	±3	LSB
EO	Offset error		±1	±2	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±0.5	±1	
EL	Integral linearity error		±0.6	±1	

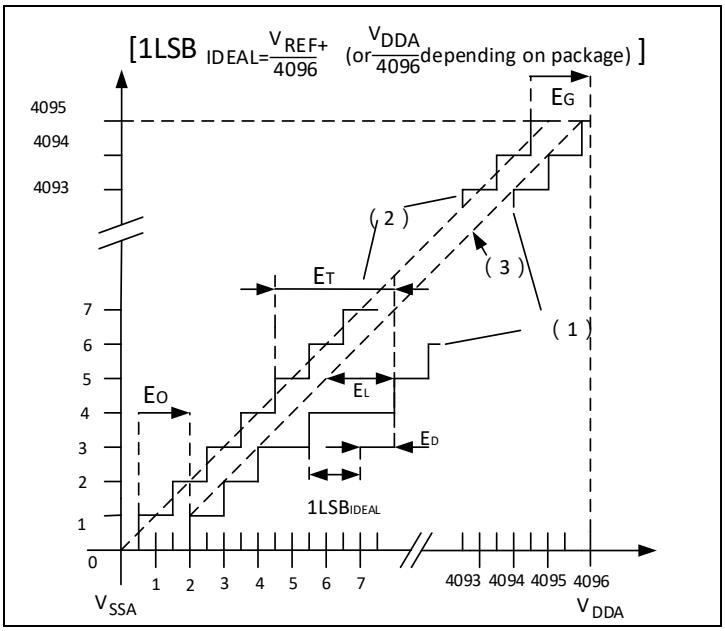
(1) ADC DC accuracy values are measured after internal calibration.
(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
(3) Guaranteed by characterization results, not tested in production.

Table 50. ADC accuracy (V_{DDA} = 2.6 to 3.6 V, T_A = -40 to +105 °C)(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.6 to 3.6 V Measurements made after ADC calibration	±2	±4	LSB
EO	Offset error		±1	±2.5	
EG	Gain error		±1.5	±3.5	
ED	Differential linearity error		±0.5	±1	
EL	Integral linearity error		±0.6	±1.2	

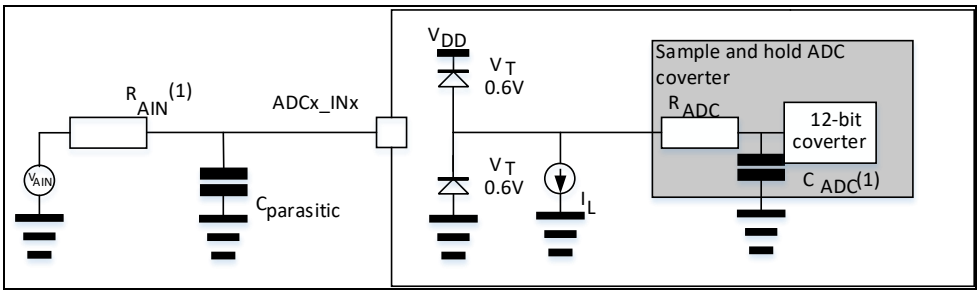
(1) ADC DC accuracy values are measured after internal calibration.
(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
(3) Guaranteed by characterization results, not tested in production.

Figure 31. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 32. Typical connection diagram using the ADC

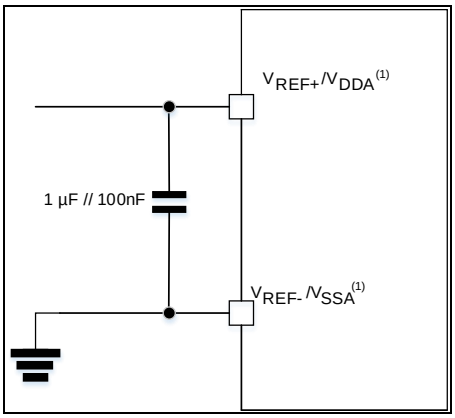


(1) Refer to *Table 46* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 33*. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 33. Power supply and reference decoupling



5.3.18 Temperature sensor characteristics

Table 51. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±2	±5	ºC
Avg_Slope(1(2))	Average slope	-4.13	-4.20	-4.35	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	1.18	1.28	1.38	V
t_{START}(3)	Startup time	-	-	100	µs
T_{S_temp}(3)(4)	ADC sampling time when reading the temperature	-	-	17.1	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.
(4) Shortest sampling time can be determined in the application by multiple iterations.

Obtain the temperature using the following formula:

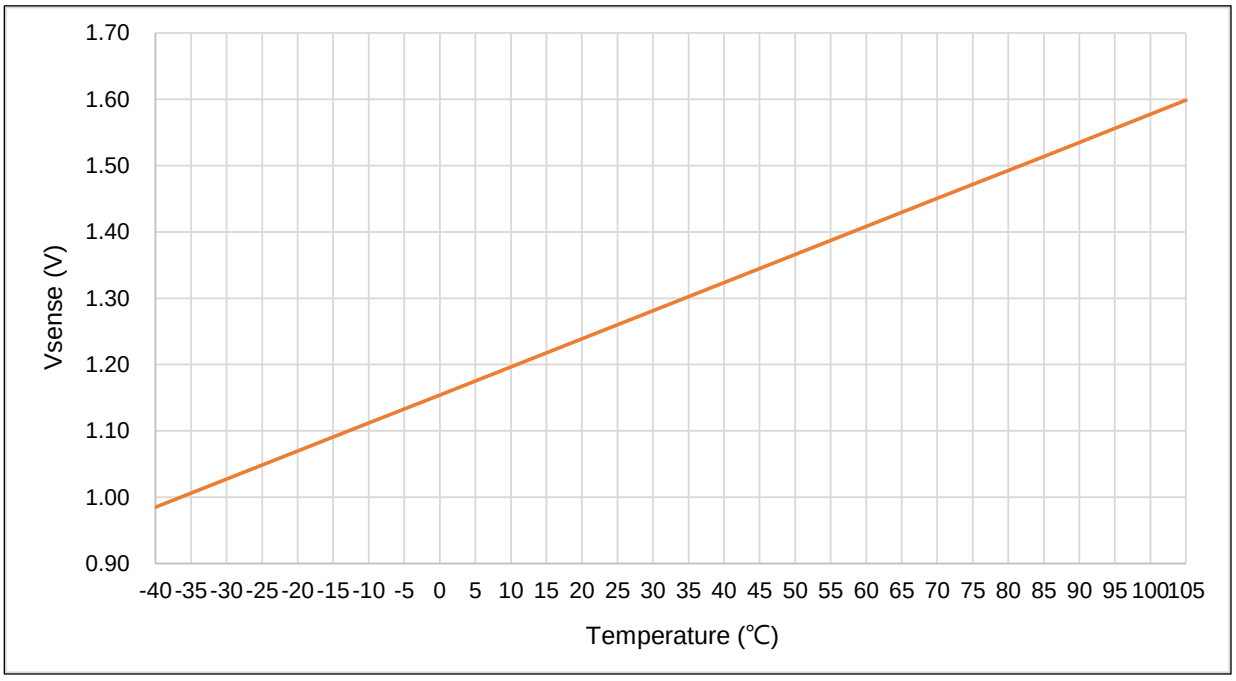
Temperature (in °C) = {(V_{25} - V_{SENSE}) / Avg_Slope} + 25.

Where,

V_{25} = V_{SENSE} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{SENSE} (given in mV/° C).

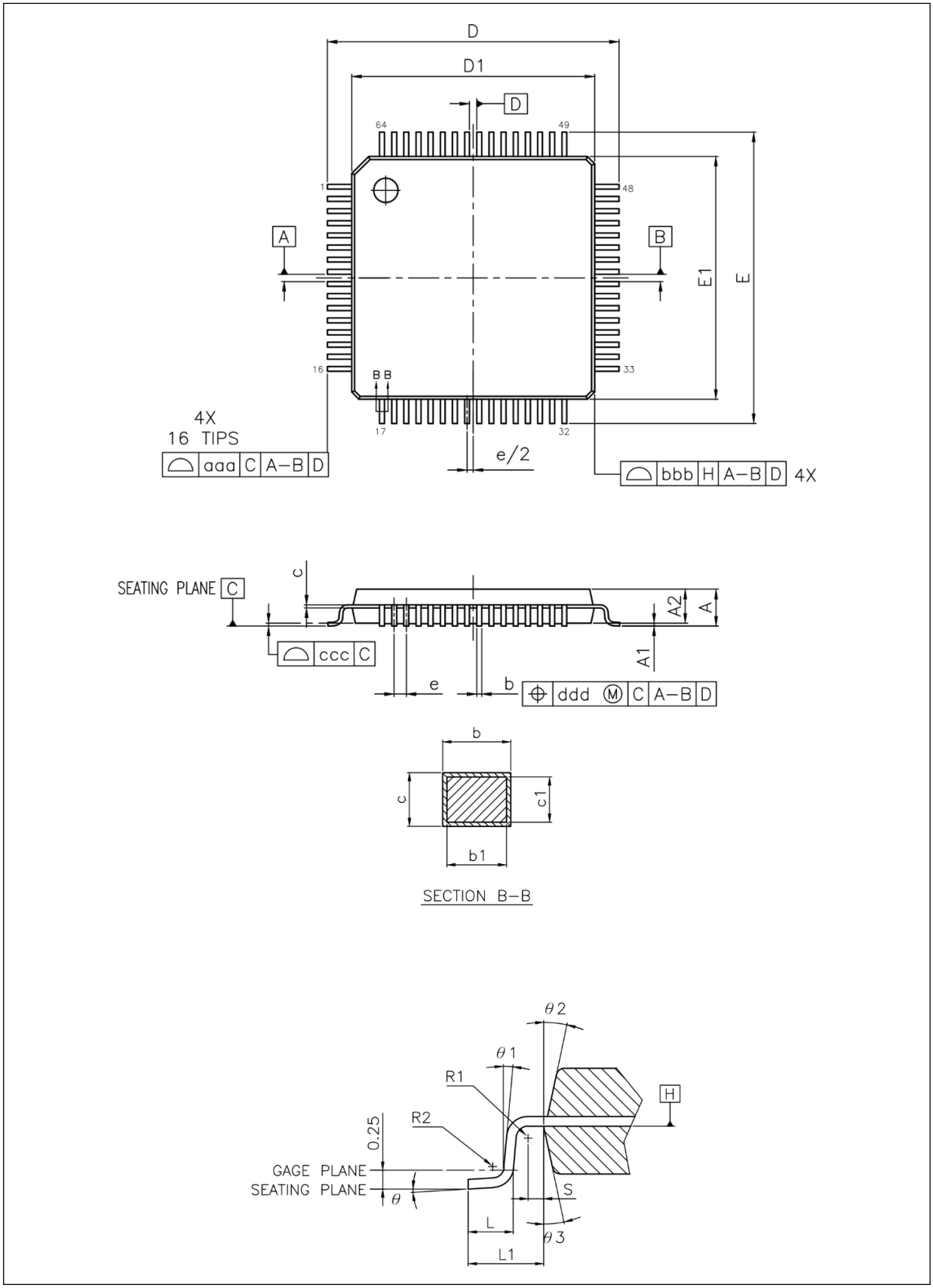
Figure 34. V_{SENSE} vs. temperature



6 Package information

6.1 LQFP64 package information

Figure 35. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 52. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

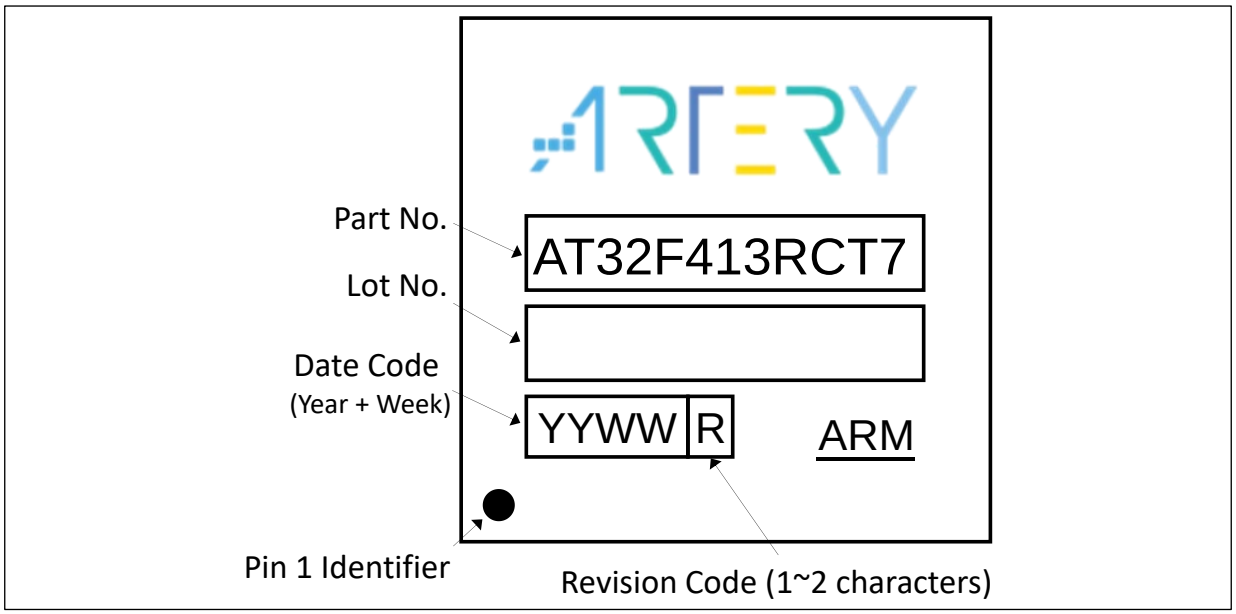
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.09	-	0.20	0.004	-	0.008
D	11.75	12.00	12.25	0.463	0.472	0.482
D1	9.90	10.00	10.10	0.390	0.394	0.398
E	11.75	12.00	12.25	0.463	0.472	0.482
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	0.50 BSC.			0.020 BSC.		
Θ	3.5° REF.			3.5° REF.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
ccc	0.08			0.003		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP64

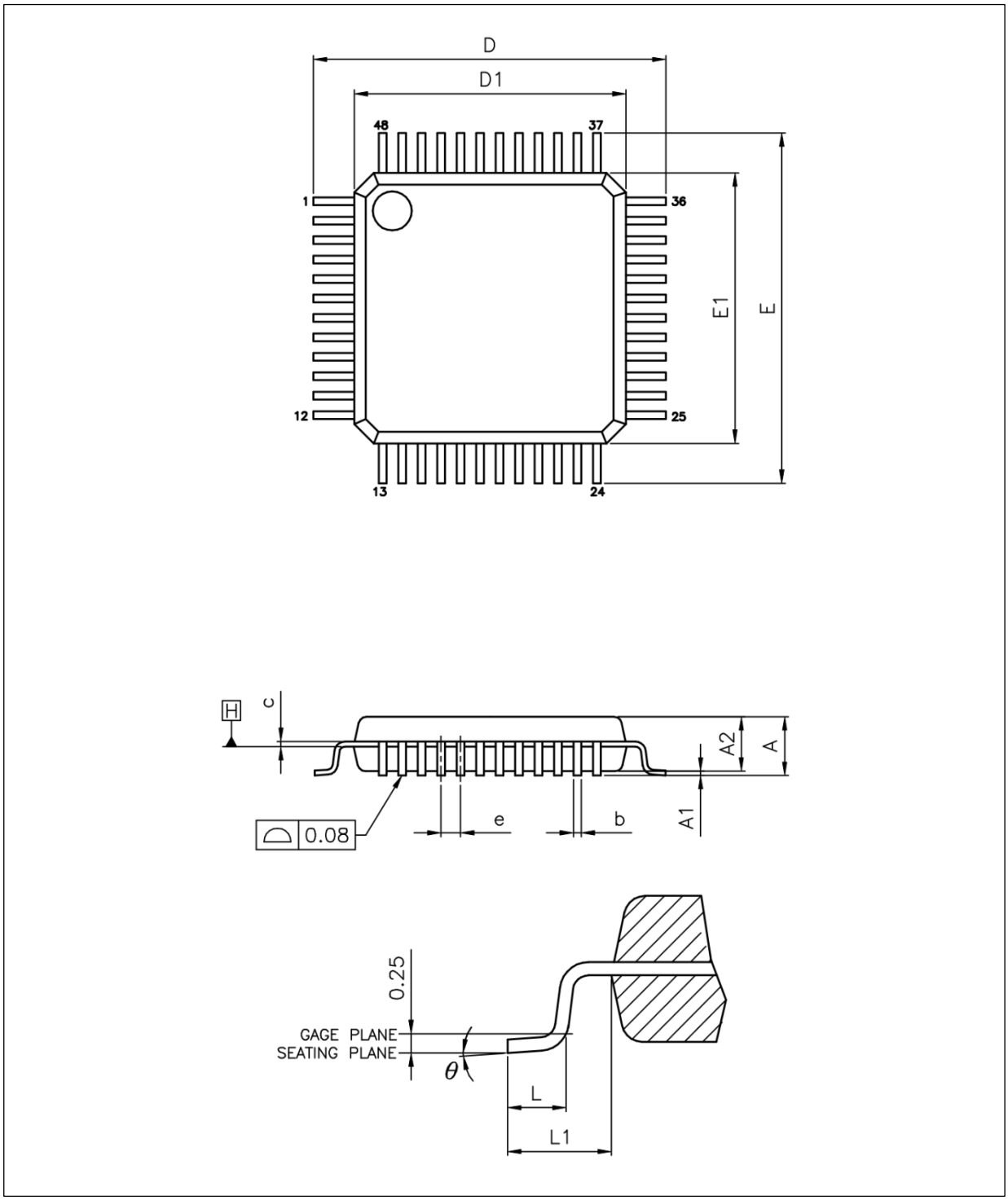
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 36. LQFP64 – 10 x 10 mm marking example (package top view)



6.2 LQFP48 package information

Figure 37. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 53. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

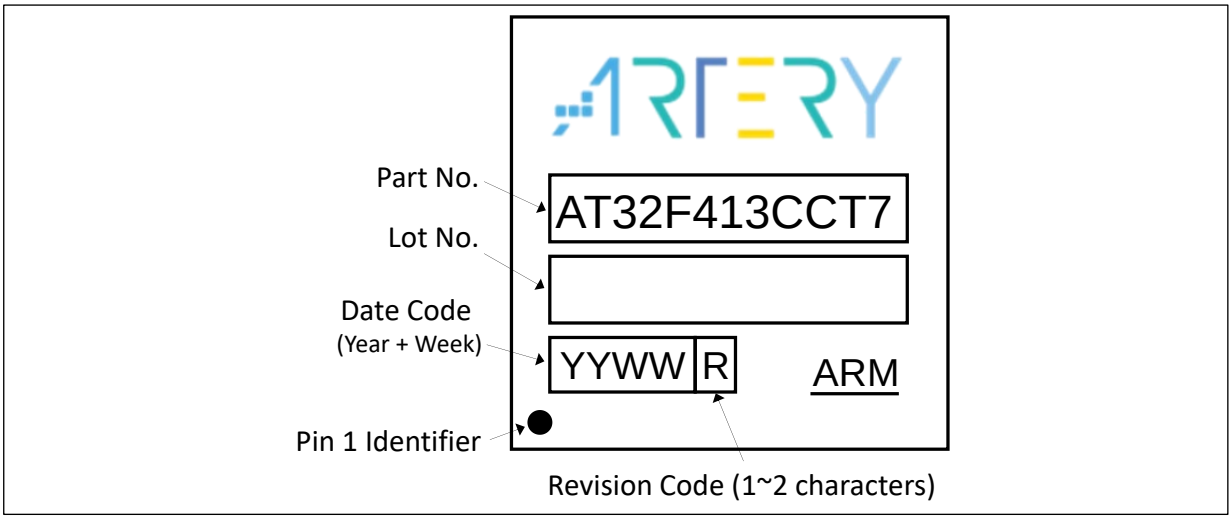
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	-	0.20	0.004	-	0.008
D	9.00 BSC			0.345 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.345 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC.			0.020 BSC.		
Θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP48

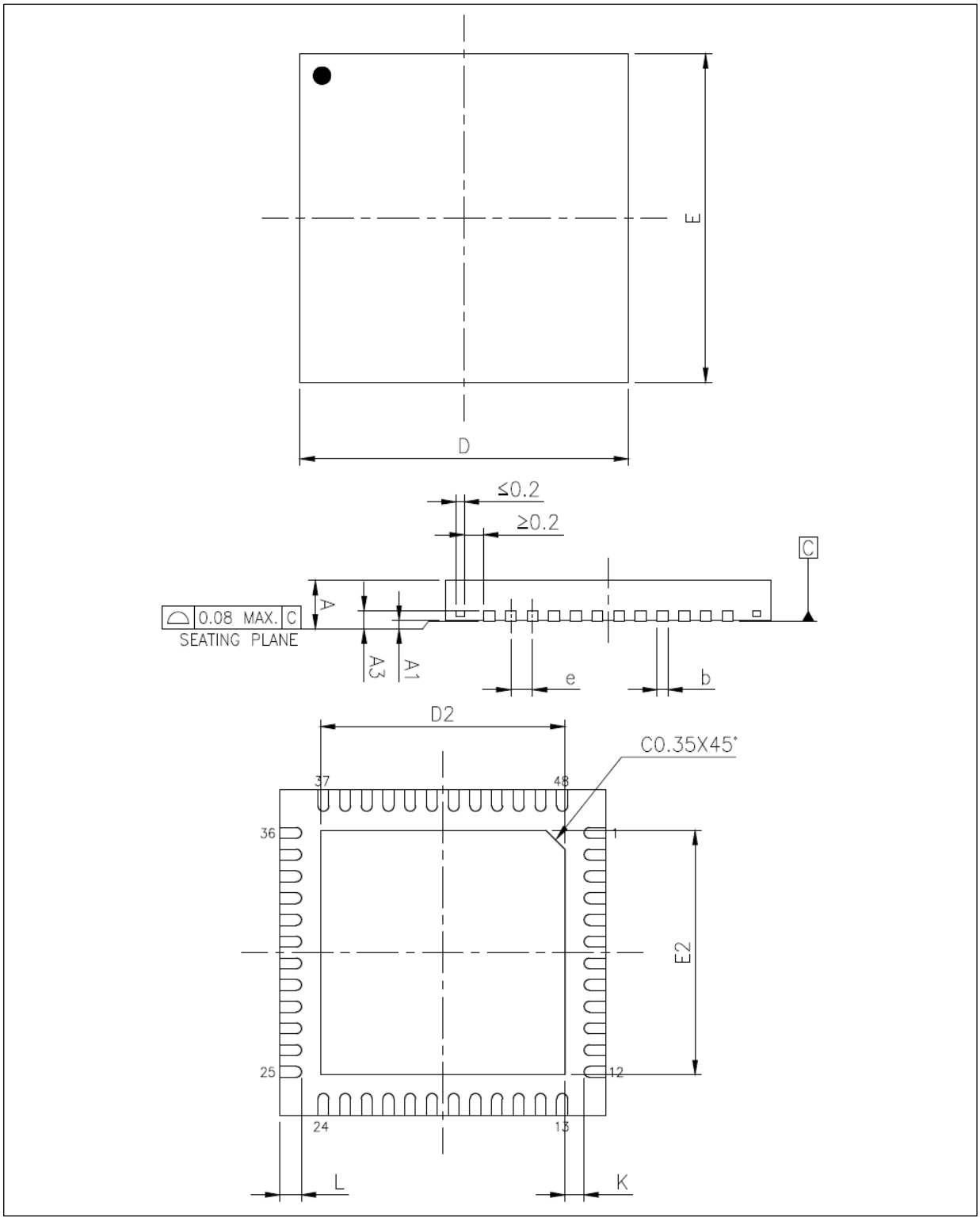
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 38. LQFP48 – 7 x 7 mm marking example (package top view)



6.3 QFN48 package information

Figure 39. QFN48 – 6 x 6 mm 48 pin fine-pitch quad flat package outline



(1) Drawing is not in scale.

Table 54. QFN48 – 6 x 6 mm 48 pin fine-pitch quad flat package mechanical data

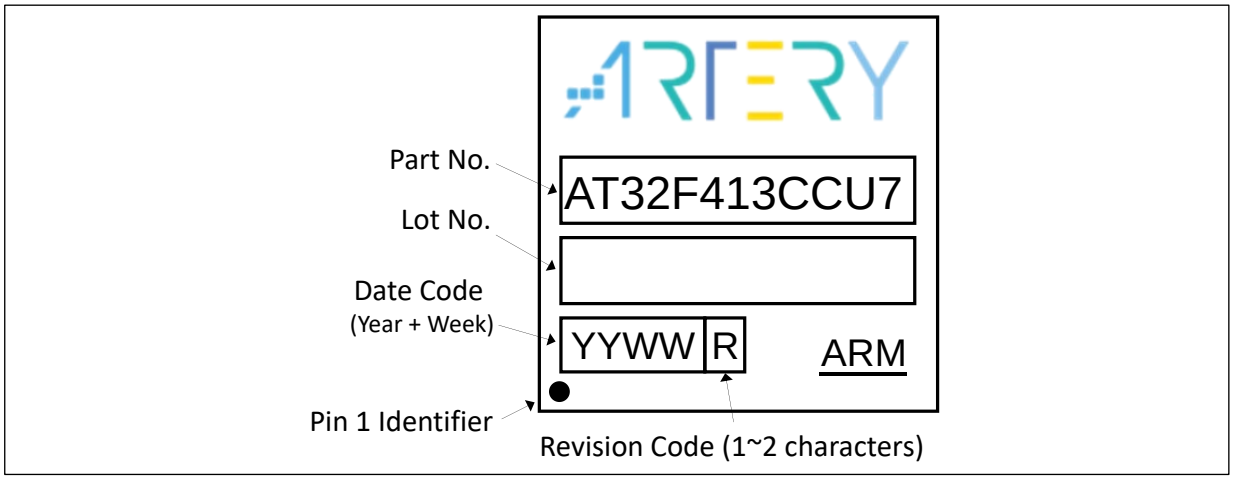
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 BSC.			0.236 BSC.		
D2	4.45	4.50	4.55	0.175	0.177	0.179
E	6.00 BSC.			0.236 BSC.		
E2	4.45	4.50	4.55	0.175	0.177	0.179
e	0.40 BSC.			0.016 BSC.		
K	0.20	-	-	0.008	-	-
L	0.35	0.40	0.45	0.014	0.016	0.018

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for QFN48

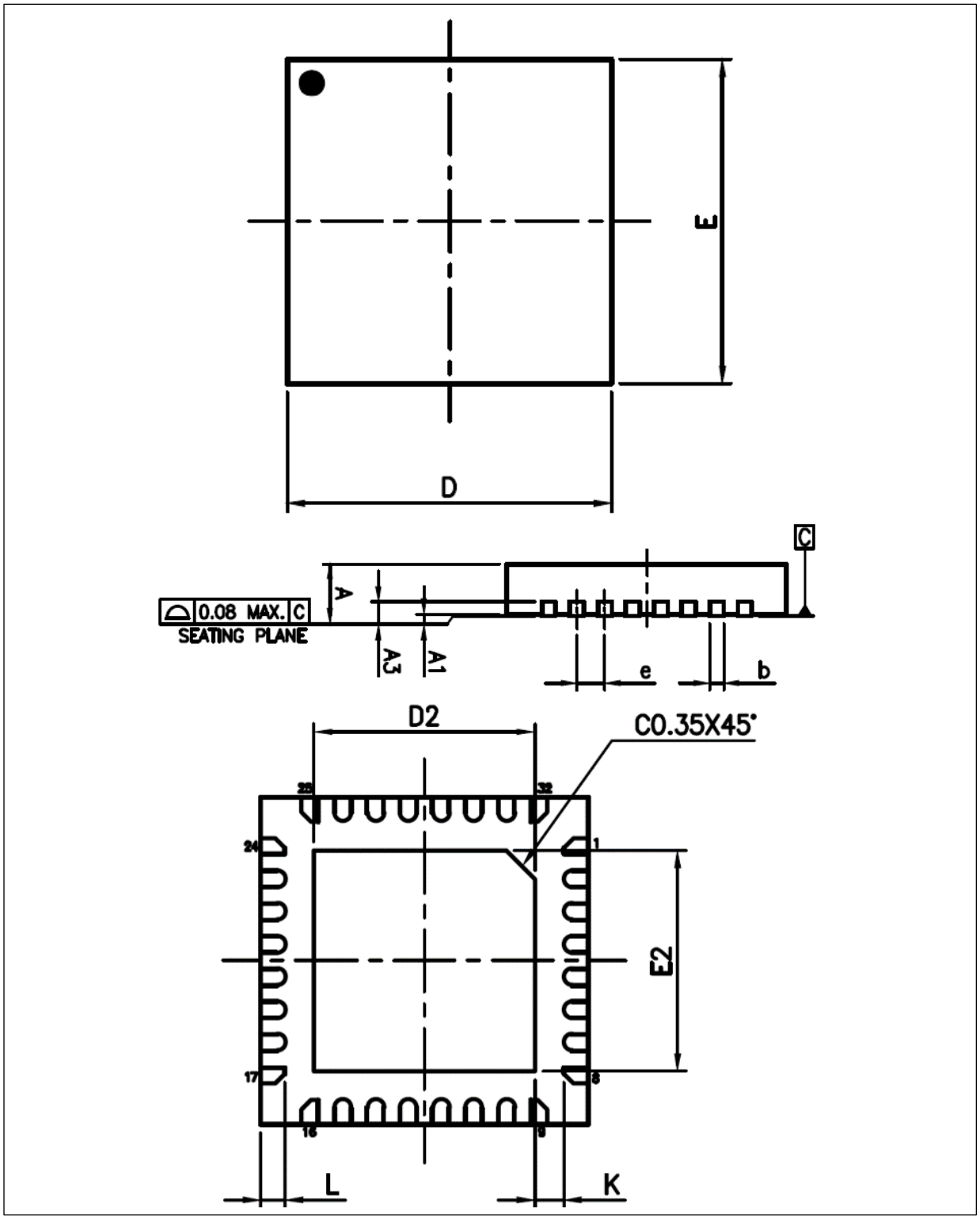
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. QFN48 – 6 x 6 mm marking example (package top view)



6.4 QFN32 package information

Figure 41. QFN32 – 4 x 4 mm 32 pin fine-pitch quad flat package outline



(1) Drawing is not in scale.

Table 55. QFN32 – 4 x 4 mm 32 pin fine-pitch quad flat package mechanical data

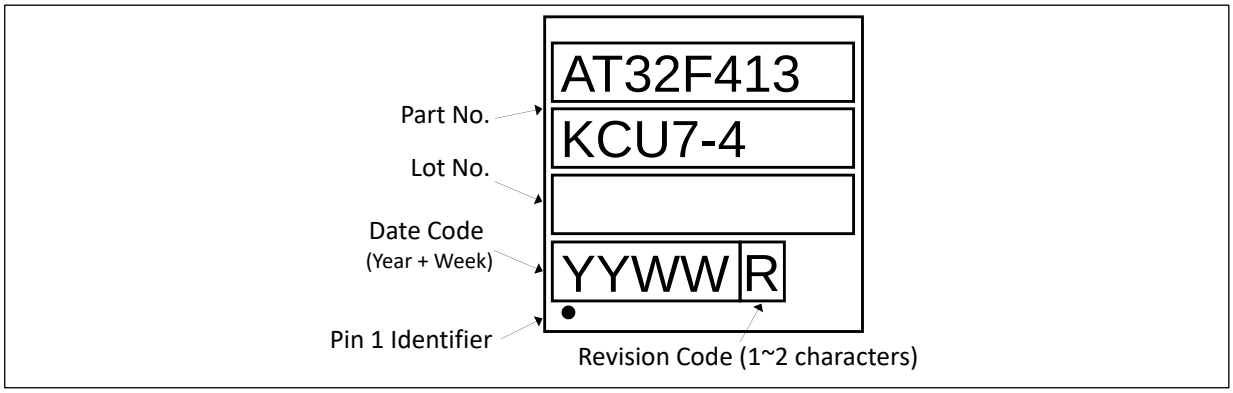
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.00 BSC.			0.157 BSC.		
D2	2.65	2.70	2.75	0.104	0.106	0.108
E	4.00 BSC.			0.157 BSC.		
E2	2.65	2.70	2.75	0.104	0.106	0.108
e	0.40 BSC.			0.016 BSC.		
K	0.20	-	-	0.008	-	-
L	0.25	0.30	0.35	0.010	0.012	0.014

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for QFN32

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. QFN32 – 4 x 4 mm marking example (package top view)



6.5 Thermal characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 9*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_j max = T_a max + (P_d max \times \Theta_{JA})$$

Where:

- $T_a$max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_d$max is the sum of P_{INT}max and $P_{I/O}$max ($P_d max = P_{INT} max + P_{I/O} max$),
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins where:

$$P_{I/O} max = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 56. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP64 – 10 × 10 mm / 0.5 mm pitch	69.2	°C/W
	Thermal resistance junction-ambient LQFP48 – 7 × 7 mm / 0.5 mm pitch	63.8	
	Thermal resistance junction-ambient QFN48 – 6 × 6 mm / 0.4 mm pitch	50.8	
	Thermal resistance junction-ambient QFN32 – 4 × 4 mm / 0.4 mm pitch	59.9	

7 Part numbering

Table 57. AT32F413 ordering information scheme

Example: AT32 F 4 1 3 K C U 7 -4

Product family

AT32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4

Product series

1 = Valued line

Product application

3 = CAN + USB series

Pin count

K = 32 pins

C = 48 pins

R = 64 pins

Internal Flash memory size

8 = 64 KBytes of the internal Flash memory

B = 128 KBytes of the internal Flash memory

C = 256 KBytes of the internal Flash memory

Package

T = LQFP

U = QFN

Temperature range

7 = -40 °C to +105 °C

Package details

-4 = QFN32 - 4 x 4 mm

Blank = Other packages

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Artery sales office.

8 Revision history

Table 58. Document revision history

Date	Version	Change
2018.11.23	1.00	Initial release.
2019.2.25	1.01	1. Corrected the maximum PLL input clock as 16 MHz in *Table 27* 2. Deleted note (4) of *Table 40* 3. Corrected the number of USART/UART in *Table 2* 4. Seperated the original Table 15 as *Table 17* and *Table 18* 5. Modified part of values in *Table 11*, *Table 13*, *Table 14*, *Table 15*, *Table 16*, *Table 17*, *Table 18*, *Table 19*, *Table 20*, *Table 24*, and *Table 26* 6. Added conditions of *Table 30* 7. Modified the maximum HBM value as 5000 V in *Table 31*
2019.3.25	1.02	1. Added AT32F413CBU7 2. Corrected CAN descriptions in sector *2.2.22* 3. Added sector *2.2.25*
2019.4.16	1.03	1. Modified AT32F413KxU7 as AT32F413KxU7-4 2. Modifed the description of MDEx[1:0] in *Table 34* 3. Corrected *Figure 42*
2019.8.6	1.04	1. Added CLKOUT prescaler in *Figure 2* 2. Added the package dimemsion in *Table 2* 3. Added the maximum rising rate of V_{DD} as note (1) of *Table 10*
2020.3.10	1.05	1. Corrected DMA2 as 7 channels 2. Added *Table 35* 3. Added USB_SOF function on PA8 4. Corrected the note of *Figure 2* about the CPU maximum speed limitation when the USB clock is direct from HSI 48 MHz 5. Correct the maximum accessable speed of I/O control registers as f_{AHB} on the cover page

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