EE 361L University of Hawaii

Lab 4.1. Verilog HDL and FPGAs: Part I

- **Objective:** Become familiar with Electronic Design Automation (EDA). Not much design here, just become familiar with the tools. You will be using software from Xilinx and an FPGA development board from Digilentinc:
  - Xilinx Vivaldo WebPACK (license free) (this has a link to the download web site but note it requires registration). This software includes an HDL editor (including module wizards), HDL simulator (including testbench wizards), and synthesizer (that converts HDL to configuration files for FPGAs). You can get a copy for free though you will have to register first. The files are large, so it will take time to download. The free versions of software will only allow you to work on verilog or VHDL. Choose verilog for this course.
  - Digilent Basys3: This is an inexpensive FPGA development board for beginners. It has a Xilinx Artix 7 FPGA. The FPGA is connected to LEDs, switches, external clocks, and other devices on the board. You can configure the board using Webpack to generate bit files, and Digilentinc's Adept Suite software to load bit files into the FPGA. Here is the datasheet for the board: https://reference.digilentinc.com/_media/basys3:basys3_rm.pdf
    Here is the schematic which shows the pin numbers of the FPGA connected to the devices on the board: https://reference.digilentinc.com/_media/basys3:basys3_sch.pdf
- **Assignment:**
  - Attached is a tutorial document. Follow the tutorial It has a Figure 1 on page 12 which shows how the FPGA is connected some of the components on the board.
- **Lab Report:** In your lab report, explain what you and your lab team did, and describe any problems that you encountered. The lab TA will explain more about what to write in your report and how long it should be. Grading style is *loose grading*.