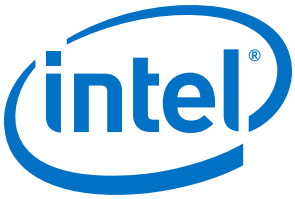

Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide

UG-01157
2016.12.09


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Contents

1 Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide

This user guide provides a brief overview of the various tabs in the device-specific PDN tool 2.0. You can quickly and accurately design a robust power delivery network with the PDN tool 2.0. This is done by calculating an optimum number of capacitors that meet the target impedance requirements for a given power supply.

Note: The PDN tool 2.0 only supports Microsoft Excel 2007 and newer, and either US or UK English language.

Table 1. PDN Tool 2.0 Software Verification

Intel® has tested and verified that the PDN tool 2.0 is compatible with these platforms and software versions.

Operating System	Excel Versions
Windows 10 (64-bit)	2013, 2016
Windows 8 (32-bit)	2007, 2010, 2013
Windows 8 (64-bit)	2010, 2013
Windows 7 (32-bit)	2007, 2010, 2013
Windows 7 (64-bit)	2010, 2013
Windows XP	2007, 2010

1.1 Overview

The Intel PDN tool 2.0 helps PCB designers estimate the number, value, and type of decoupling capacitors needed to develop an efficient PCB decoupling strategy. It allows you to do this during the early design phase, without going through extensive pre-layout simulations.

The PDN tool 2.0 is a Microsoft Excel-based spreadsheet that calculates an impedance profile based on your input. For a given power supply, the spreadsheet only requires basic design information to calculate the impedance profile and the optimum number of capacitors to meet the desired impedance target (Z_{TARGET}). Basic design information includes the board stackup, transient current information, and ripple specifications, for example. The tool also provides the device- and power rail-specific PCB decoupling cut-off frequency ($F_{EFFECTIVE}$). The results obtained through the PDN tool 2.0 are intended only as a preliminary estimate and not as a specification. For an accurate impedance profile, Intel recommends a post-layout simulation approach using any available EDA tool, such as Cadence PowerSI, Ansys SIWave, and Cadence Allegro PCB PI.

There are two versions of the PDN tool 2.0. One version is for 20-nm devices (which also includes the 14-nm Stratix® 10 devices), and one version is for 28-nm devices. The device families supported by the Intel device-specific PDN tool 2.0 are shown at the top of the **Release Notes** tab and they include:

- 14-nm devices:
  - Stratix 10
- 20-nm devices:
  - Arria® 10
  - MAX® 10
- 28-nm devices:
  - Arria II GZ
  - Arria V
  - Arria V GZ
  - Cyclone IV E
  - Cyclone IV GX
  - Cyclone® V
  - Stratix V

1.2 PDN Decoupling Methodology Review

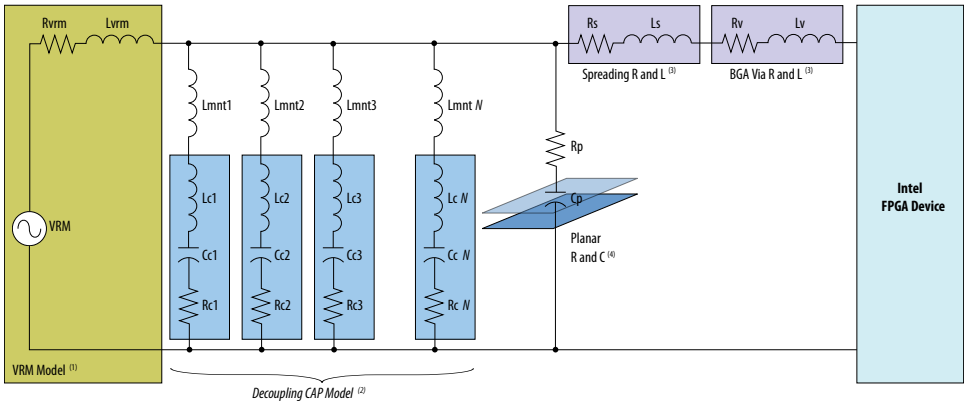
The PDN tool 2.0 provides two parameters for guiding PCB decoupling design: Z_{TARGET} and $F_{EFFECTIVE}$.

1.2.1 PDN Circuit Topology

The PDN tool 2.0 is based on a lumped equivalent model representation of the power delivery network topology.

Figure 1. PDN Topology Modeled as Part of the Tool

The PDN impedance profile is the impedance-over-frequency looking outward from the device.



Notes:
1. You can define or change VRM parameters in the Library sheet of the PDN tool.
2. You can define or change Decoupling Caps parameters in the Cap Mount, X2Y Mount, and Library sheets of the PDN tool.
3. R* and L* are parasitic capacitances and inductances from BGA balls and PCB traces and connections.
4. Represents PCB layers dedicated to power and ground planes.

For a first order analysis, the VRM can be simply modeled as a series-connected resistor and inductor as shown above. This is a result of the typical proportional, integral, derivative (PID) voltage regulation loop compensation configuration of many regulators. The VRM has a very low impedence and can respond to the instantaneous current requirements of the FPGA up to between 50 KHz and 150 KHz, depending on the voltage regulation loop crossover (0 dB) frequency.

The equivalent series resistance (ESR) and equivalent series inductance (ESL) values can be obtained from the VRM manufacturer. At higher frequencies, the VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement.

PCB decoupling capacitors are used for reducing the PDN impedance up to 50-100 MHz. The on-board discrete decoupling capacitors provide the required low impedance. This depends on the capacitor-intrinsic parasitics (R_{cN}, C_{cN}, L_{cN}) and the capacitor mounting inductance (L_{mntN}). The inter-planar capacitance between the power-ground planes typically has lower inductance than the discrete decoupling capacitor network, making it more effective at higher frequencies up to 100 MHz. As frequency increases, the PCB decoupling capacitors become less effective. The limitation comes from the parasitic inductance seen with respect to the FPGA. FPGA parasitic inductance includes capacitor mounting inductance, PCB spreading inductance, ball grid array (BGA) via inductance, and packaging parasitic inductance. All of these parasitics are modeled in the PDN tool 2.0 to capture the effect of the PCB decoupling capacitors accurately. To simplify the circuit topology, all parasitics are represented with lumped inductors and resistors despite the distributed nature of PCB spreading inductance.

1.2.1.1 Z_{TARGET}

According to Ohm's law, voltage drop across a circuit is proportional to the current flow through the circuit, and impedance of the circuit. The dynamic component of PDN current gives rise to voltage fluctuation within the PDN, which may lead to logic and timing issues. You can reduce excessive voltage fluctuation by reducing PDN impedance. One design guideline is target impedance, Z_{TARGET}. Z_{TARGET} is defined using the maximum allowable noise tolerance and dynamic current change, and is calculated as follows.

Figure 2. Z_{TARGET} Equation

$$Z_{TARGET} = \frac{\text{Voltage Rail} \times \left(\frac{\text{Noise Tolerance\%}}{100}\right)}{\text{Maximum Dynamic Current Change}}$$

For example, to reliably decouple a 1.8-V power rail that allows 5% of noise tolerance and a maximum 2 A current draw, 50% of which is dynamically changing, the desired target impedance is calculated as follows.

Figure 3. Z_{TARGET} Example Equation

$$Z_{TARGET} = \frac{1.8 \times 0.05}{2 \times 0.5} = 0.09\,\Omega$$

To accurately calculate the Z_{TARGET} for any power rail, you must know the following information:

- The maximum dynamic current change requirements for the FPGA that is powered by the power rail under consideration. You can obtain this information from respective device datasheet. You can calculate the maximum dynamic current change of a device using the maximum total current and the dynamic current change percentage.

  Note: The dynamic current change is intended to parameterize the high-frequency current draws required to provide the energy for CMOS transistors changing state. In the case of the core rail, the transients are generated by switching inside the FPGA core. Thus, a design which involves extensive logical switching generates higher % transients (dynamic current change) than a more static design. For information about recommended settings, refer to the table in the **Introduction** tab of the PDN tool 2.0.

  Note: You can obtain accurate estimations on the maximum total current for Intel FPGA devices using the *PowerPlay Early Power Estimator (EPE)* tool or the Quartus® Prime PowerPlay Power Analyzer tools. When using the data from the EPE, be sure to use only the dynamic power for each section for the PDN calculation.

- The maximum allowable noise tolerance on the power rail is given as a percentage of the supply voltage.

Device switching activity leads to transient noise (high frequency spikes) seen on the power supply rails. This noise can cause functionality issues if they are too high. The noise must be damped within a range defined as a percentage of power supply voltage. The recommended values for the maximum allowable noise tolerance are listed in the respective device datasheet and in the **Introduction** tab of the PDN tool 2.0. Different rails have different specifications because of their sensitivity to the transient voltage noise as well as how much current is used by the power rail.

Refer to the **Introduction** tab of the PDN tool 2.0 for more information about Z_{TARGET}.

Table 2. Settings for the Stratix 10 Device Power Rails

This information is from the PDN tool 2.0 for a Stratix 10 device.

Rail Name	Default Voltage (V)	Noise Tolerance (%) [1]	Dynamic Current Change (%) [1]	Description
VCC	0.8 - 0.94 [2]	5	30 - 50	Core (30% for high dynamic current; 50% for low dynamic current)
VCCERAM	0.9	5	50	Programmable Power Tech Aux
VCCR_GXB	1.03/1.12 [2]	3	30	RX Analog
VCCT_GXB	1.03/1.12 [2]	2	60	TX Analog
VCCPT	1.8	5	50	Programmable Power Tech
VCCA_PLL	1.8	5	10	PLL Analog

continued...

1 These settings will be updated in a future release of this document.

2 For more information about power rail functions, refer to the Pin Connection Guidelines for the selected device family.

Rail Name	Default Voltage (V)	Noise Tolerance (%) [1]	Dynamic Current Change (%) [1]	Description
VCCH_GXB	1.8	3	15	Transceiver I/O Buffer Block
VCCIO	1.2/1.25/1.35/1.5/1.8	5	100	I/O Banks
VCCP	0.8 - 9.4 [2]	5	33	Periphery Power Supply
VCCBAT	1.2/1.5/1.8	5	100	Battery Back-up Power Supply

Related Links

- PowerPlay Early Power Estimator (EPE)
- Stratix 10 GX and SX Device Family Pin Connection Guidelines
- *Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*.
- *MAX 10 Device Family Pin Connection Guidelines*.
- *Stratix V E, GS, and GX Device Family Pin Connection Guidelines*.
- *Stratix V GT Device Family Pin Connection Guidelines*.
- *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*.
- *Arria II Device Family Pin Connection Guidelines*.
- *Cyclone V Device Family Pin Connection Guidelines*.
- *Cyclone IV Device Family Pin Connection Guidelines*.

1.2.1.2 $F_{EFFECTIVE}$

As previously described, a capacitor reduces PDN impedance by providing a least-impedance route between power and ground for transient current. Impedance of a capacitor at high frequency is determined by its parasitics (ESL and ESR). For a PCB with capacitors mounted, the parasitics include not only the parasitic from the capacitors themselves but also those associated with mounting, PCB spreading, and packaging. Therefore, PCB capacitor parasitics are generally higher than on-die capacitance. As a result, decoupling using PCB capacitors becomes ineffective at higher frequencies. Using PCB capacitors for PDN decoupling beyond their effective frequency range brings no improvement to PDN performance and raises the bill of materials (BOM) cost.

To help reduce over-design of PCB decoupling, this release of the PDN tool provides a suggested PCB decoupling design cut-off frequency ($F_{EFFECTIVE}$) as another guideline. You only need to design PCB decoupling that keeps Z_{EFF} under Z_{TARGET} up to $F_{EFFECTIVE}$. Z_{EFF} is the impedence profile of the PCB design and includes all PDN-related design parasitics, including:

- VRM R and L
- PCB spreading R and L
- Plane R and C
- Decoupling capacitors
- BGA_via R and L

1 These settings will be updated in a future release of this document.

$F_{EFFECTIVE}$ defines the effective frequency of on-board decoupling capacitors.

Refer to *Troubleshooting Z_{EFF}* if the Z_{EFF} is too high or the number of capacitors for decoupling becomes too high.

Note: $F_{EFFECTIVE}$ may not be enough when the Intel FPGA device shares a power rail with another device. The noise generated from other devices propagates along the PDN and affects FPGA device performance. The frequency of the noise is determined by the transfer impedance between the noise source and the FPGA device, and can be higher than $F_{EFFECTIVE}$. Reducing PDN parasitic inductance and increasing the isolation between the FPGA device and noise source reduces this risk. You must perform a transfer impedance analysis to clearly identify any noise interference risk.

Related Links

- Troubleshooting ZEFF on page 31
- For more information about the PDN decoupling methodology behind the PDN design tool, refer to the *Power Delivery Network Design Using Altera PDN Design Tools* online course.

1.2.2 Major Tabs of the PDN Tool 2.0

The tabs at the bottom of the PDN tool 2.0 application help you calculate your impedance profile.

Table 3. PDN Tool 2.0 Tabs

Tab	Description
Release_Notes	Provides the legal disclaimers, the revision history of the tool, and the user agreement.
Introduction	Displays the schematic representation of the circuit that is modeled as part of the PDN tool 2.0. It also provides the following related information: • quick start instructions • recommended settings for some power rails • a brief description of decoupling design procedures under different power supply connection schemes
System_Decap	The principal tab that allows you to decouple your system. It displays by default when you launch the application. This tab provides an interface to enter your power sharing scheme for a selected FPGA device and derive the decoupling based on the input.
Stackup	Provides an interface to enter your stackup information into the PDN tool.
Library	Points to various libraries (capacitor, dielectric materials, and so on) that are called by other tabs. You can change the default values listed as part of these libraries.
BGA_Via	Provides an interface to calculate the BGA mounting inductance based on design-specific via parameters and the number of vias.
Plane_Cap	Provides an interface to calculate the plane capacitance based on design-specific parameters.
Cap_Mount	Provides an interface to input design-specific parameters for calculating the capacitor mounting inductance for two different capacitor orientations (Via on Side [VOS] and Via on End [VOE]).
X2Y_Mount	Provides an interface to input design-specific parameters for calculating the capacitor mounting inductance for X2Y type capacitors.
Enlarged_Graph	Provides an enlarged view of the Z-profile shown in the **System_Decap** tab.

1.2.2.1 System_Decap

You can determine the decoupling of selected FPGA devices based on the power sharing scheme entered in the **System_Decap** tab.

The **System_Decap** tab is divided into the following sections:

- Device selection
- Power rail data and configuration
- VRM Data
- Rail group summary
- VRM impedance
- BGA Via
- Plane
- Spreading
- $F_{EFFECTIVE}$
- Decoupling selection
- Result summary

1.2.2.1.1 Device Selection Section

1. Select the **Family/Device** using the drop-down list.

   In the 20-nm Pro version of the PDN tool, choose Stratix 10 or Arria 10 devices. In the 20 nm Standard version of the tool, choose MAX 10 devices. In the 28 nm PDN tool, choose all other devices.

2. Select your device and the package type from the **Available Devices** drop-down list.
3. Select your desired power rail configuration from the **Power Rail Configuration** drop-down list.

   The **Power Rail Configuration** list includes custom and pre-defined configurations. When you select a pre-defined configuration, the tool sets the suggested power rail grouping automatically.

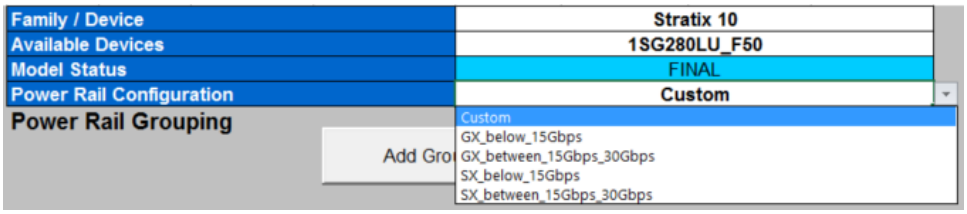
The drop-down selections are based on examples from the pin connection guidelines for the device. Select the one that most closely matches your design, and use it as a basis for entering your design data. Refer to the pin connection guidelines for your device.

The tool updates the list of power rails and the contents in the power rail configuration sections based on your selections.

Figure 4. Device Selection

Family / Device	Stratix 10
Available Devices	1SG280LU_F50
Model Status	FINAL
Power Rail Configuration	Custom

Figure 5. Power Rail Configuration Selection



Related Links

- Stratix 10 GX and SX Device Family Pin Connection Guidelines
- *Arria 10 GX, GT, and SX Device Family Pin Connection Guidelines*
- *MAX 10 Device Family Pin Connection Guidelines*
- *Stratix V E, GS, and GX Device Family Pin Connection Guidelines*
- *Stratix V GT Device Family Pin Connection Guidelines*
- *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*
- *Arria II Device Family Pin Connection Guidelines*
- *Cyclone V Device Family Pin Connection Guidelines*
- *Cyclone IV Device Family Pin Connection Guidelines*

1.2.2.1.2 Power Rail Data and Configuration Section

This section of the application is divided into two areas. Area 1 is for the device power rail information, and Area 2 is for the power rail configuration.

1. Enter the power supply voltage in the **Voltage** column for each power rail listed in Area 1 by selecting a value from the pull-down menu, or by manually entering your own value.

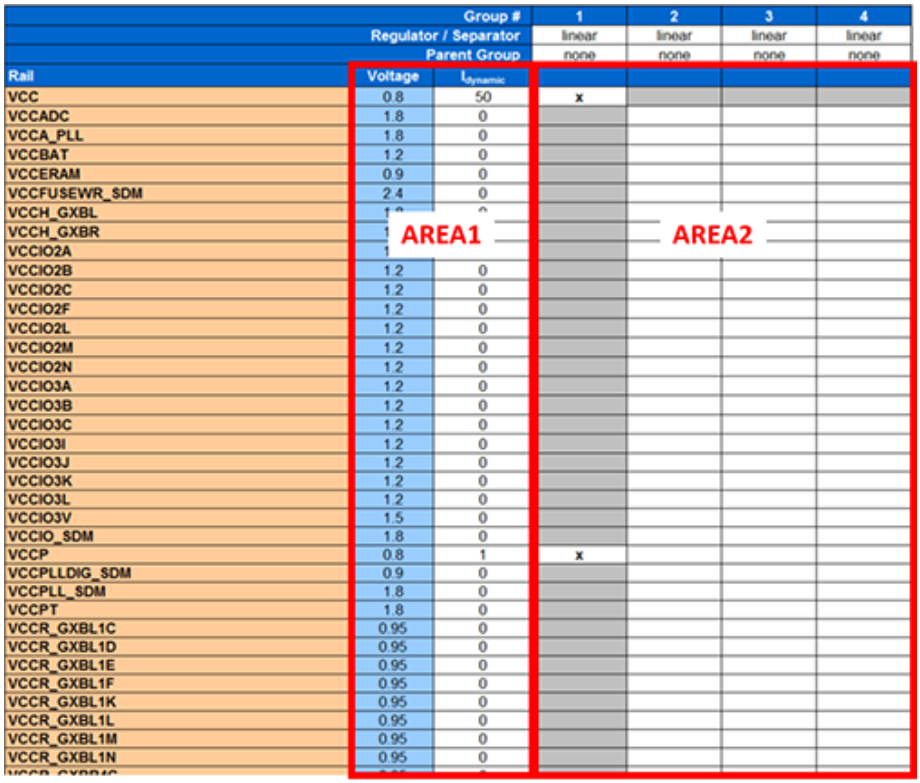
   Note: You must enter the total dynamic current consumption of related power rails before you can use the system decoupling function.

   You can optionally adjust the recommended number up or down slightly based on knowledge of the intended application.

2. Enter the current consumption in the **I dynamic** column for each power rail. The earliest data from the *PowerPlay Early Power Estimator (EPE)* can provide good values for the current entries. The EPE delivers bulk data for the transceiver channels. Each bank of transceiver channels should be assigned the total EPE value divided by the number of banks. Later in the design cycle, the Quartus Prime Power Play Power Analyzer (PPPA) can derive much better data for each bank rail.
3. Setup your device power sharing scheme in Area 2.

Figure 6. Power Rail Data and Power Sharing Scheme Section

This configuration is an example of how this section of the spreadsheet should look. Every design will vary depending on the device chosen and the power rail configuration selected.



	Group #	1	2	3	4
	Regulator / Separator	linear	linear	linear	linear
	Parent Group	none	none	none	none
Rail	Voltage	$I_{dynamic}$				
VCC	0.8	50	x			
VCCADC	1.8	0				
VCCA_PLL	1.8	0				
VCCBAT	1.2	0				
VCCERAM	0.9	0				
VCCFUSEWR_SDM	2.4	0				
VCCH_GXBL						
VCCH_GXBR						
VCCIO2A						
VCCIO2B	1.2	0				
VCCIO2C	1.2	0				
VCCIO2F	1.2	0				
VCCIO2L	1.2	0				
VCCIO2M	1.2	0				
VCCIO2N	1.2	0				
VCCIO3A	1.2	0				
VCCIO3B	1.2	0				
VCCIO3C	1.2	0				
VCCIO3I	1.2	0				
VCCIO3J	1.2	0				
VCCIO3K	1.2	0				
VCCIO3L	1.2	0				
VCCIO3V	1.5	0				
VCCIO_SDM	1.8	0				
VCCP	0.8	1	x			
VCCPLLDIG_SDM	0.9	0				
VCCPLL_SDM	1.8	0				
VCCPT	1.8	0				
VCCR_GXBL1C	0.95	0				
VCCR_GXBL1D	0.95	0				
VCCR_GXBL1E	0.95	0				
VCCR_GXBL1F	0.95	0				
VCCR_GXBL1K	0.95	0				
VCCR_GXBL1L	0.95	0				
VCCR_GXBL1M	0.95	0				
VCCR_GXBL1N	0.95	0				

The current usage for each rail should be entered in the **I dynamic** column in Area 1. Note that, for the VCC rail, only the dynamic current usage should be entered from the Early Power Estimator.

Each column in Area 2 represents a power group in your system. Add or remove a power group using the **Add Group** or **Remove Group** buttons. The first row of each group is the **Regulator/Separator** type. Set the source type for the power group and available options from the pull-down list as **switcher**, **linear**, or **filter**.

The second row is the **Parent Group** type. The available options for this row are **None** and the number representing all listed power groups. Input your power sharing hierarchy in this column, and set the power rail connection using the remaining rows.

Note: The PDN tool 2.0 defines the power rail configuration using the **Parent/ Child** power group. A power group is a child power group if it attaches to another power group at its input. The other power group is the parent group in this case. A parent group can have multiple child groups. A parent power group number is required for the child group. The parent group number of a parent power group is assigned to **None** because the group has no parent group.

The available options are:

- *blank* — Device rail does not connect to the power group.
- **x** — Device rail connects to the power group.
- **x/related**— Device rail connects to the group, and its activity is related to other rails that connect to the same group. You must select **x/related** if that VCCIO/VCCPT power rail is related to other rails within the same power rail group.

Note: Two I/O rails are related if their output activities are synchronous. For example, when two VCCIO rails are assigned to the same memory interface. The maximum current will usually be reached at the same time for these related rails. As a result, the total current of related rails equals the sum of the current of all shared rails. The total current of unrelated rails is calculated using the root-sum-square (RSS) method.

The PDN tool 2.0 sets the default power rail sharing configuration based on the selected Intel-recommended power rail configuration listed above. Make changes to better match your design.

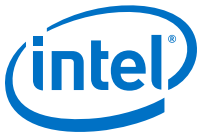
Note: In the rail connection matrix, you can change the voltage of a rail without disconnecting it from a regulator group. However, all other rails connected to the same group **must** be able to change to the new voltage.

Figure 7. Changing Voltage for All Rails in a Group

		Group #	1	2	3	4
		Regulator / Separator	linear	linear	linear	linear
		Parent Group	none	none	none	none
Rail	Voltage	$I_{dynamic}$				
VCC	0.8	0				
VCCADC	1.8	0				
VCCA_PLL	1.8	0				
VCCBAT	1.2	0				
VCCERAM	1.2	0				
VCCFUSEWR_SDM	1.5	0				
VCCH_GXBL	1.8	0				
VCCH_GXBR	1.8	0				
VCCIO2A	1.2	0				
VCCIO2B	1.2	0				
VCCIO2C	1.2	0				
VCCIO2F	1.2	0				
VCCIO2L	1.2	0				
VCCIO2M	1.2	0				
VCCIO2N	1.2	0				
VCCIO3A	1.2	0				
VCCIO3B	1.2	0				
VCCIO3C	1.2	0				
VCCIO3I	1.2	0				
VCCIO3J	1.2	0				
VCCIO3K	1.2	0				
VCCIO3L	1.2	0				
VCCIO3V	1.5	0				
VCCIO_SDM	1.8	0				
VCCP	0.8	0				
VCCPLLDIG_SDM	0.9	0				
VCCPLL_SDM	1.8	0				
VCCPT	1.8	0				
VCCR_GXBL1C	0.95	0				
VCCR_GXBL1D	0.95	0				
VCCR_GXBL1E	0.95	0				
VCCR_GXBL1F	0.95	0				
VCCR_GXBL1K	0.95	0				
VCCR_GXBL1L	0.95	0				
VCCR_GXBL1M	0.95	0				
VCCR_GXBL1N	0.95	0				

Related Links

PowerPlay Early Power Estimator (EPE)



1.2.2.1.3 VRM Data Section

Enter the voltage regulator module (VRM) parameters for **DC supply voltage**, **Switcher VRM Efficiency**, and **Switcher VRM Input Current**.

Note: If you are using a VRM with a sense line, the system compensates for the IR drop automatically.

1.2.2.1.4 Rail Group Summary Section

In this section, you can find a list of the following calculated key parameters of all power groups:

- Voltage
- Total Current
- Dynamic Current Change
- Noise Tolerance
- Core Clock Frequency
- Current Ramp Up Period
- Z_{TARGET}

These options allow you to customize how the data is collected or analyzed.

The **Dynamic Current Change** parameter has a pull-down menu with the following options:

- Calculate
- Override

Dynamic current change percentage requires a lot of diligence. The EPE and PPPA both deliver values for current usage that include:

- the maximum static current (does not vary)
- the maximum current usage by the active elements

This calculation yields both a very high total current and a fairly high dynamic current usage. Calculations for a value to insert into the **Dynamic Current Change** field could yield a value much lower than the auto-populated value, which represents a safe engineering value.

The **Noise Tolerance** parameter has a pull-down menu with the following options:

- Calculate
- Override

Some PDN tool variants allow you to add data for the **Core Clock Frequency** and **Current Ramp Up Period** parameters using the pull-down menus. These values tell the tool how to calculate the current ramp up period for transient events, sometimes reducing transient current changes. The values relate to how fast the clock for the section is running, and the length of the data pipeline. Given a transient change in the input data, there are clock cycles in the pipeline for the algorithm to deliver the results. If the input data change activates a broad yet short pipeline, the transient is abrupt. This results in a large current change for the number of logic elements being used. If the pipeline is narrow and long, the overall change in current usage is proportionately smaller.

You can set the **Core Clock Frequency** parameter to a **High**, **Medium**, **Low**, or **Custom** set of input frequencies. The **Custom** option allows you to enter a specific input frequency.

The **Current Ramp Up Period** parameter allows you to specify the number of clock cycles consumed by the pipeline. You can select a **Long**, **Medium**, **Short**, or **Custom** setting.

Core Clock Frequency and **Current Ramp Up Period** options are highly dependent upon the core utilization setup in Quartus Prime. Thus, options in the PDN tool can be used as a reference.

1.2.2.1.5 VRM Impedance Section

Enter the VRM impedance values for the regulators. Use the pull-down menu to enter data for **VRM Resistance** and **VRM Inductance**.

There are three ways to change the voltage regulator module (VRM) parameters. Depending on what you select in the **VRM Impedence** pull-down menu, you can:

- Select **Custom** and set your desired Rvrm and Lvrm values.
- Select **Library** and get the suggested typical Rvrm and Lvrm values. This depends on the type of regulator (for example, switching, linear, or filter) you have selected.
- Select **Ignore** and Rvrm and Lvrm will not be considered as design parameters.
- For switching regulators, you can choose a specific Enpirion® VRM (based on ordering code) directly in the pull-down menu.

The PDN tool can help you select the appropriate Enpirion VRM module to use for each power supply in your system.

1.2.2.1.6 BGA Via Section

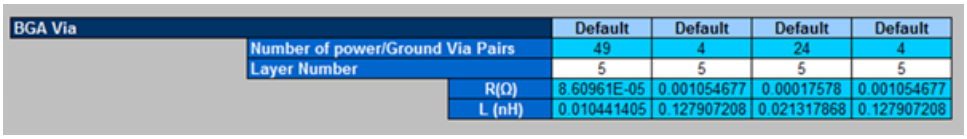
The **BGA Via** table shows the L and R values per via. You can set the tool to **Calculate**, **Custom**, **Default**, or **Ignore**. For a fully customized workflow in which each rail group can have different settings:

1. Select the **System_Decap** tab in the PDN tool 2.0.
2. Set the total effective R and L values in the **BGA Via** section to match your system.

If you set the **BGA Via** table to **Calculate** or **Ignore**, the **System_Decap** tab to uses the same global settings for all rail groups.

If you set the **BGA Via** table to **Default**, the PDN tool calculates the R and L values similarly to the **Calculate** option, however, the tool also calculates the number of power/ground via pairs based on the rails connected to the regulator group. You can input the layer number in the tool. The layer number should match the target layer in **Full Stackup**. Then, BGA via R and L will be calculated corresponding to the layer number.

Figure 8. Setting the Layer Number



BGA Via		Default	Default	Default	Default
Number of power/Ground Via Pairs		49	4	24	4
Layer Number		5	5	5	5
	R(Ω)	8.60961E-05	0.001054677	0.00017578	0.001054677
	L (nH)	0.010441405	0.127907208	0.021317868	0.127907208

1.2.2.1.7 Plane Section

In the **Plane** table, you can set the tool to **Calculate**, **Custom**, or **Ignore**. For a fully customized workflow in which each rail group can have different settings:

1. Select the **Plane_Cap** tab in the PDN tool 2.0.
2. Set the parameters to match your system, and notice that the **Total planar capacitance** and **Total sheet resistance** values are updated automatically.
3. In the **System_Decap** tab, select the **Custom** option for each group where a custom plane is required.
4. Enter the calculated **Ctotal** and **Rtotal** values into the **Plane** section of the **System_Decap** tab.

Setting the **Plane** table to **Calculate** or **Ignore** causes the **System_Decap** tab to use the same global settings for all rail groups.

1.2.2.1.8 Spreading Section

In the **Spreading** table, you can set the tool to one of the following options:

- **Ignore**
- **Low**
- **Medium**
- **High**
- **Custom**

For a fully customized workflow in which each rail group can have different settings:

1. Select the **Library** tab in the PDN tool 2.0.
2. Set the parameters in the **Spreading R and L** table to match your system.
3. Examine the range of spreading R and L values to determine if you need a custom R and L. If a custom R and L is warranted, select **Custom** in the **System_Decap** tab and set the R and L values directly.

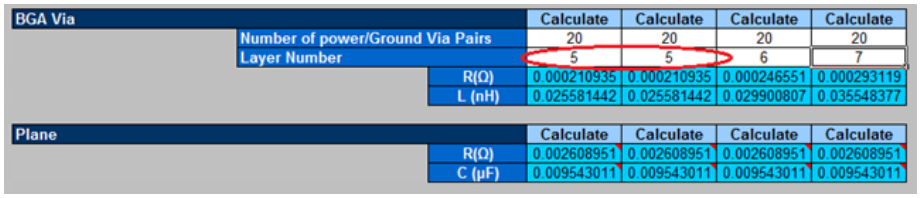
Setting the **Spreading** table to **Low**, **Medium**, **High**, or **Ignore** causes the **System_Decap** tab to use the same global settings for all rail groups.

1.2.2.1.9 Implementing Split Planes

Each group of power rails shares the same regulator. Therefore, separate power rail groups have separate regulators. However, they might share the same power plane layer (but separate power islands with different dimensions). Alternatively, each power rail group can be located on a different power plane layer.

1. If the regulator groups share the same power plane, select the same **Layer Number** under **BGA Via** in the **System-Decap** tab.

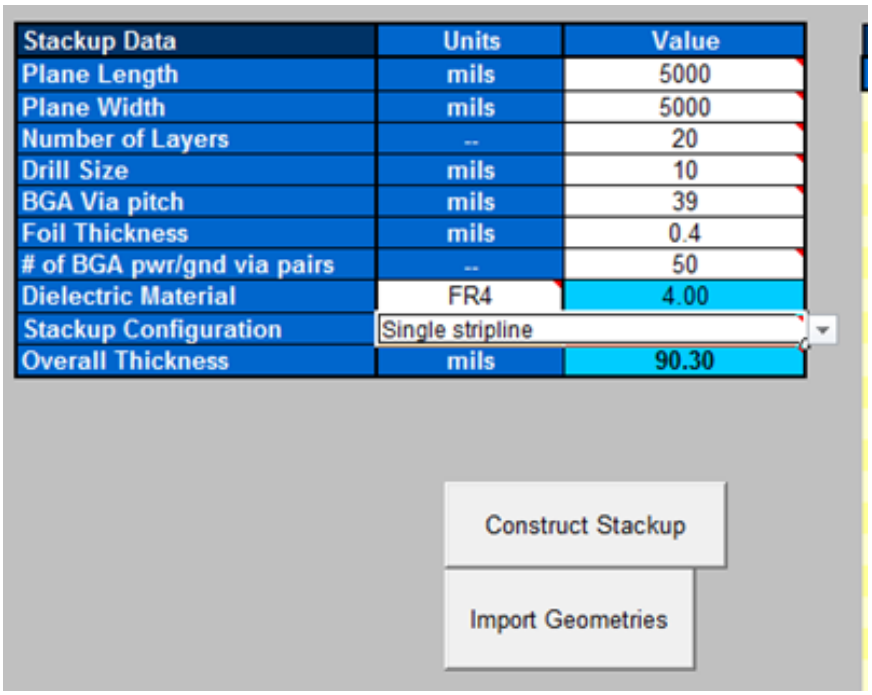
Figure 9. Set the Layer Number



BGA Via		Calculate	Calculate	Calculate	Calculate
	Number of power/Ground Via Pairs	20	20	20	20
	Layer Number	5	5	6	7
	R(Ω)	0.000210935	0.000210935	0.000246551	0.000293119
	L (nH)	0.025581442	0.025581442	0.029900807	0.035548377
Plane		Calculate	Calculate	Calculate	Calculate
	R(Ω)	0.002608951	0.002608951	0.002608951	0.002608951
	C (µF)	0.009543011	0.009543011	0.009543011	0.009543011

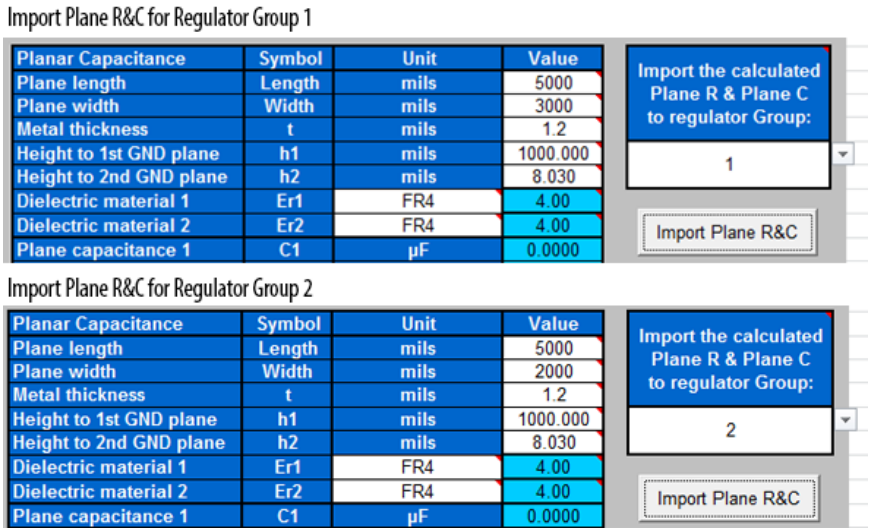
2. Perform these steps in the **Stackup** tab:
   a. Complete the **Stackup Data** table.
   b. Click **Import Geometries**.

Figure 10. Complete the Stackup Data Table



3. Perform these steps in the **Plane_Cap** tab:
   a. Specify the dimensions of the area allocated to each regulator group.
   b. Change the import target from **All** to the group ID.
   c. Click **Import Plane R&C**.

Figure 11. Import the Plane R&C



1.2.2.1.10 $F_{EFFECTIVE}$ Section

You can set **Feffective** to **Calculate** or **Override.** Select the **Calculate** option to use the Intel-recommended cut off frequency based on package and die parasitics.

1.2.2.1.11 Decoupling Section

You can set **Decoupling** to **Manual** or **Auto**. If you select the **Auto** option, any change you make to the system is automatically reflected in the decoupling solution. You can also view the impedance chart per rail group or VRM.

Selecting the **Manual** option allows you to:

- Lock in calculated decoupling solutions from being further optimized by any changes made to the **System_Decap** tab.
- Add or remove the number and type of decoupling capacitors in the **Results Summary** section. You can see its immediate impact on the impedance profile curve.

1.2.2.1.12 Results Summary Section

You can find the list of the number and type of capacitors used for each group, and the summary of all the capacitors used. The values in each column indicate the number of capacitors needed of each value for each rail.

The results section may show a very large number of capacitors required to decouple some power rails. Changes in various worksheets that supply data to this worksheet will have a substantial effect on the capacitors required.

Figure 12. Results Summary Section of the System_Decap Tab

1.2.2.1.13 Recommended Flow for Deriving Decoupling for an FPGA System using the System_Decap Tab

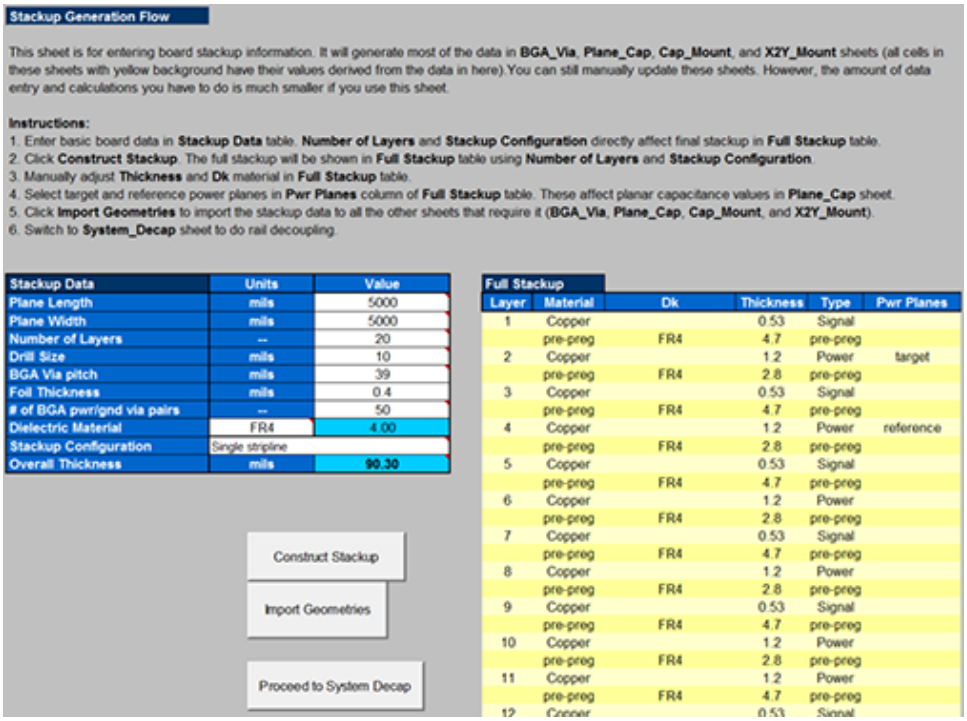
To use the **System_Decap** tab, perform the following steps:

1. Select the appropriate device family or device.
2. Set up the stack up information in the **Stackup** tab.
3. Select the decoupling scheme.
   The tool updates the power rail connection configuration to the scheme recommended in the Pin Connection Guidelines.
4. Ensure that the following default parameters match your system, and make the necessary changes such as:
   - power rail configuration
   - relativity of power rails within the same power group
   - power group layer
   - number of power/ground Via pairs
   - DC voltage supply for VRM module
   - decoupling cap location
5. Enter the projected current consumption of each power rail.
   If you applied the **Custom** setting, refer to BGA Via Section on page 14, Plane Section on page 15, or Spreading Section on page 15 to enter your values.

1.2.2.2 Stackup

Enter the PCB stackup information of your design in the **Stackup** tab. This tab updates related data in the **BGA_Via**, **Plane_Cap**, **Cap_Mount** and the **X2Y_Mount** tabs. The stackup information in this tab is also used for the **System_Decap** tab. Follow the instructions provided at the beginning of the tab to fill in the content for this tab.

Figure 13. Stackup Tab



1.2.2.2.1 Stackup Data

The **Stackup Data** section is where you enter board dimension data and other parameters, such as board stackup settings, power via, and dielectric material.

1.2.2.2.2 Full Stackup

This section lists the complete stackup of your board. You can modify content in the section to better match your board design. The last column in the section is the **PWR plane** types. In a single rail analysis case, assign the layer where the power rail is located as **target**, and the ground layer that the power rail refers to as **reference**.

Table 4. Full Stackup Buttons

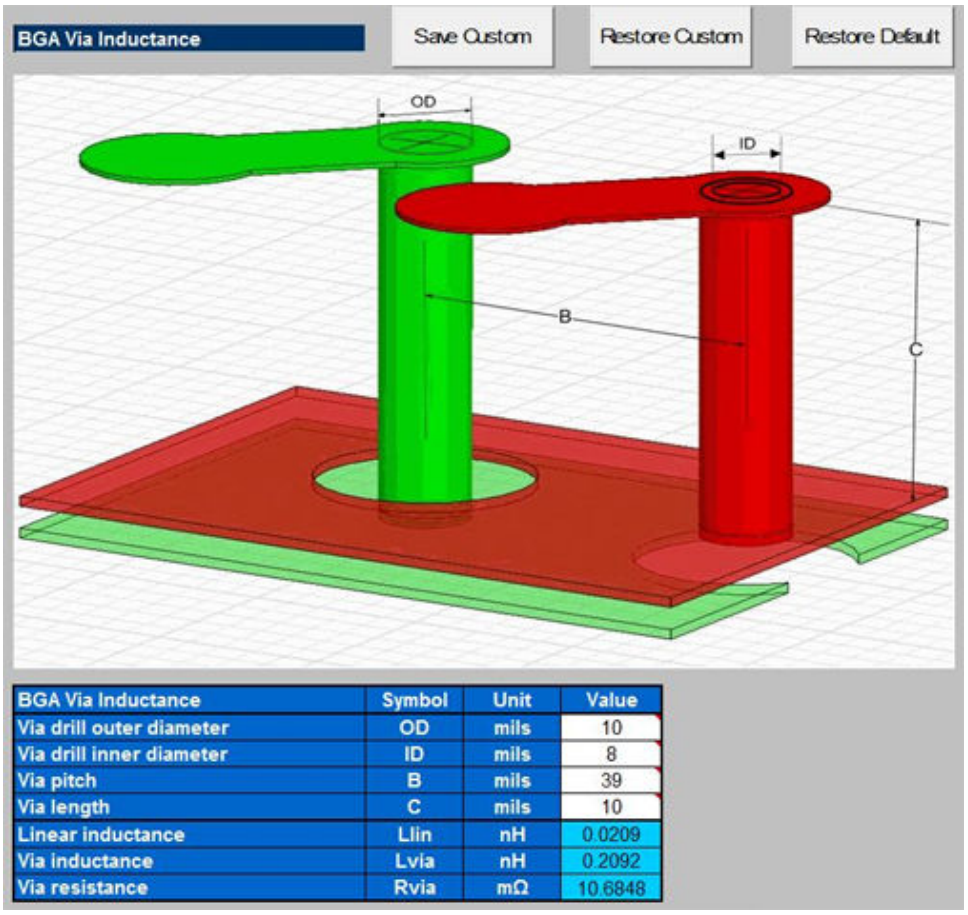
Button Label	Description
Construct Stackup	Populates the **Full Stackup** section to the number of layers defined in the **Stackup Data** section using the blocks listed in the **Stackup Stub** section.
Import Geometries	Updates geometry parameters in the **BGA_Via**, **Plane_Cap**, **Cap_Mount**, and **X2Y_Mount** tabs using your input from the **Stackup Data** section. The tool also checks that the **PWR Planes** column in the **Full Stackup** section has only one target layer, and provides a warning for this error.
Proceed to System Decap	Opens the **System_Decap** tab.

1.2.2.3 BGA_Via

The **BGA Via** tab calculates the vertical via loop inductance under the **BGA pin** field.

Figure 14. BGA_Via Tab

The values in the **Unit** column indicate a unit value per one pair.



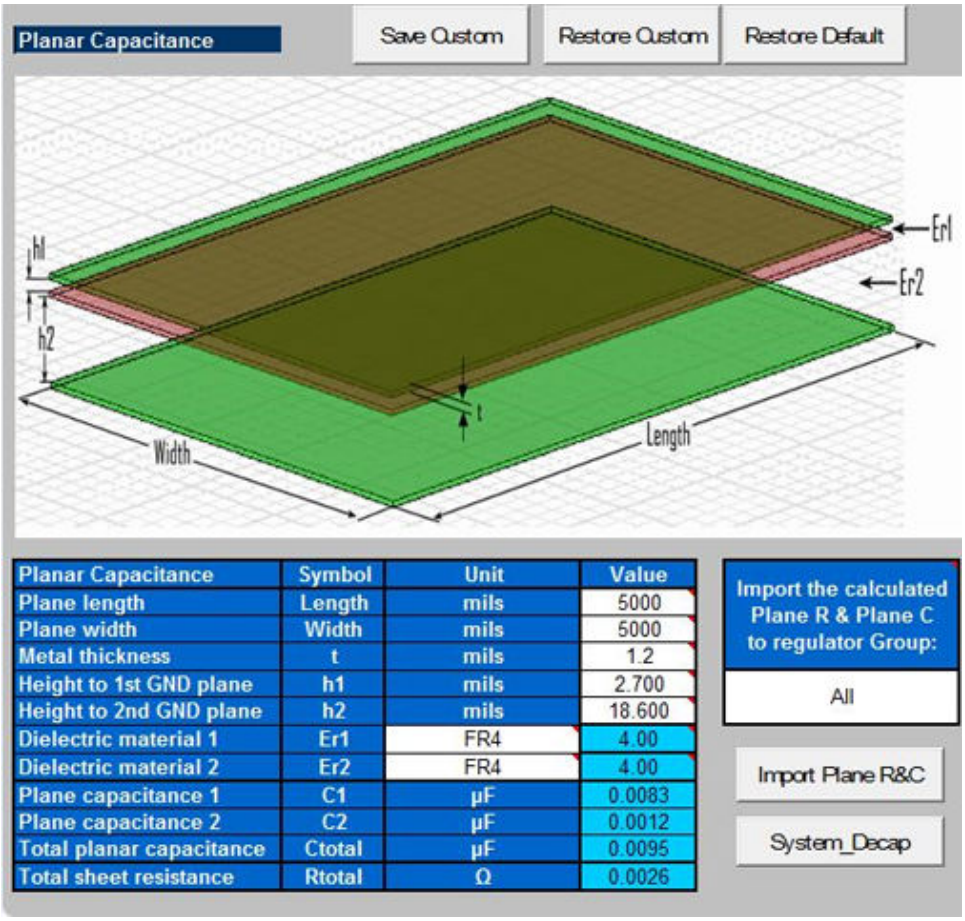
BGA Via Inductance	Symbol	Unit	Value
Via drill outer diameter	OD	mils	10
Via drill inner diameter	ID	mils	8
Via pitch	B	mils	39
Via length	C	mils	10
Linear inductance	Llin	nH	0.0209
Via inductance	Lvia	nH	0.2092
Via resistance	Rvia	mΩ	10.6848

Enter the layout-specific information such as via drill diameters, via length, via pitch, and the number of power/ground via pairs under the BGA in the **BGA Via Inductance** table. The tool calculates the effective via loop inductance and resistance value. You can save the change made to the tab, restore the changes, or restore the tab back to the default settings.

1.2.2.4 Plane_Cap

The **Plane Cap** tab calculates the distributed plane capacitance in microfarads (µF) that is developed between the power/ground planes based on the parallel plate capacitor equation.

Figure 15. Plane_Cap Tab



Planar Capacitance	Symbol	Unit	Value
Plane length	Length	mils	5000
Plane width	Width	mils	5000
Metal thickness	t	mils	1.2
Height to 1st GND plane	h1	mils	2.700
Height to 2nd GND plane	h2	mils	18.600
Dielectric material 1	Er1	FR4	4.00
Dielectric material 2	Er2	FR4	4.00
Plane capacitance 1	C1	µF	0.0083
Plane capacitance 2	C2	µF	0.0012
Total planar capacitance	Ctotal	µF	0.0095
Total sheet resistance	Rtotal	Ω	0.0026

Enter the design specific information such as plane dimensions, plane configuration and the dielectric material used in the **Planar Capacitance** table. The tool calculates a plane capacitance value. You can save custom values, restore custom values, or restore the default settings.

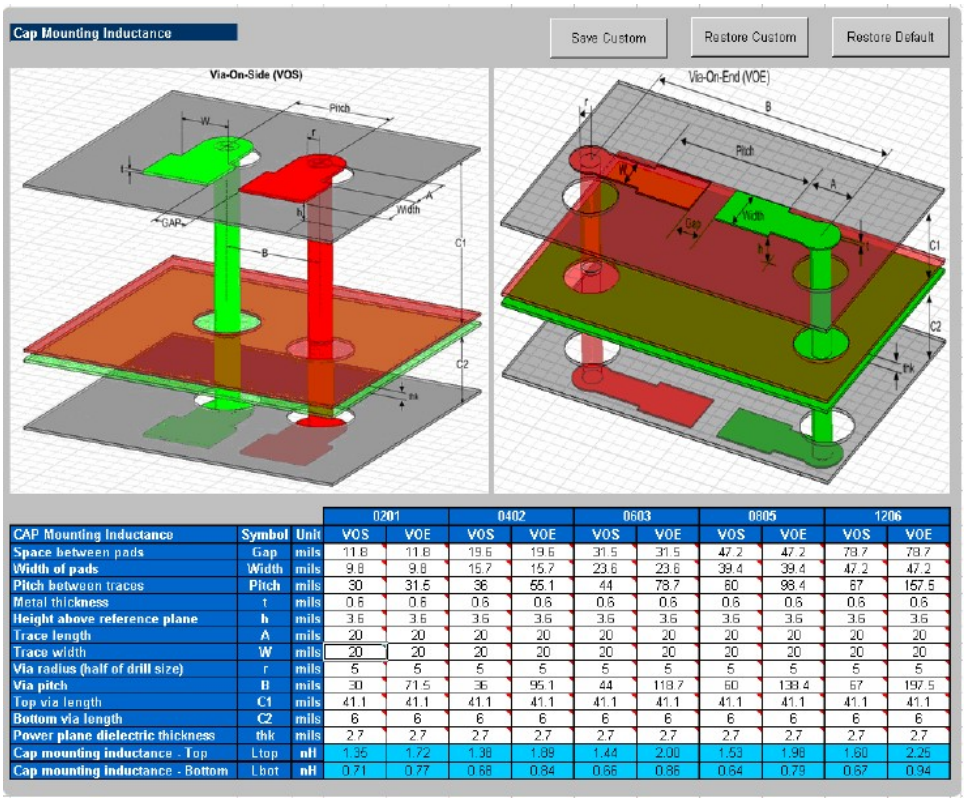
The **Import Plane R&C** button inserts the data for the planar capacitance into the regulator group data.

1.2.2.5 Cap_Mount

The **Cap Mount** tab calculates the capacitor mounting inductance seen by the decoupling capacitor.

Note: Power rails on different layers have different mounting inductances. For the best results, run the PDN separately for each layer set.

Figure 16. Cap Mount Tab



			0201		0402		0603		0805		1206	
CAP Mounting Inductance	Symbol	Unit	VOS	VOE	VOS	VOE	VOS	VOE	VOS	VOE	VOS	VOE
Space between pads	Gap	mils	11.8	11.8	19.6	19.6	31.5	31.5	47.2	47.2	78.7	78.7
Width of pads	Width	mils	9.8	9.8	15.7	15.7	23.6	23.6	39.4	39.4	47.2	47.2
Pitch between traces	Pitch	mils	30	31.5	36	55.1	44	78.7	60	98.4	67	157.5
Metal thickness	t	mils	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
Height above reference plane	h	mils	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6	3.6
Trace length	A	mils	20	20	20	20	20	20	20	20	20	20
Trace width	W	mils	20	20	20	20	20	20	20	20	20	20
Via radius (half of drill size)	r	mils	5	5	5	5	5	5	5	5	5	5
Via pitch	B	mils	30	71.5	36	95.1	44	118.7	60	138.4	67	197.5
Top via length	C1	mils	41.1	41.1	41.1	41.1	41.1	41.1	41.1	41.1	41.1	41.1
Bottom via length	C2	mils	6	6	6	6	6	6	6	6	6	6
Power plane dielectric thickness	thk	mils	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7	2.7
Cap mounting inductance - Top	Ltop	nH	1.35	1.72	1.38	1.89	1.44	2.00	1.53	1.98	1.60	2.25
Cap mounting inductance - Bottom	Lbot	nH	0.71	0.77	0.68	0.84	0.66	0.86	0.64	0.79	0.67	0.94

The capacitor mounting calculation is based on the assumption that the decoupling capacitor is a two-terminal device. The capacitor mounting calculation is applicable to any two-terminal capacitor with the following footprints: 0201, 0402, 0603, 0805, and 1206. Enter all the information relevant to your layout, and the tool provides a mounting inductance for a capacitor mounted on either the top or bottom layer of the board. Depending on the layout, you can choose between VOE (Via on End) or VOS (Via on Side) to achieve an accurate capacitor mounting inductance value. Generally, VOS can have lower mounting inductance due to a smaller via pitch. Also, X2Y cap can be considered as a solution for a space-limited design.

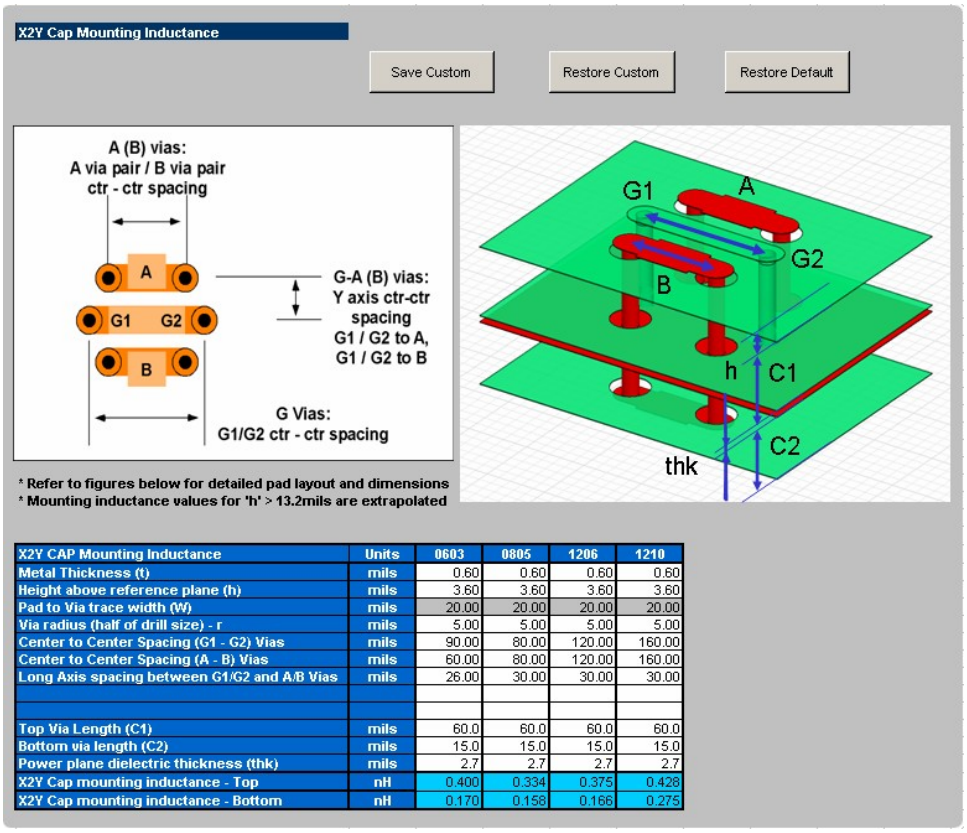
If you plan to use a footprint capacitor other than a regular two-terminal capacitor or X2Y capacitor for decoupling, you can skip the **Cap Mount** tab. In this case, you can directly enter the capacitor parasitics and capacitor mounting inductance in the **Library** tab (under the **Custom** field in the **Decoupling Cap** section of the library). As with the other tabs, you can save the changes made to the tab, restore the changes, or restore the tab back to the default settings.

You must pay special attention to the via lengths for the capacitors. Via inductance comprises a substantial portion of the PDN impedance.

1.2.2.6 X2Y_Mount

The **X2Y Mount** tab calculates the capacitor mounting inductance seen by the X2Y decoupling capacitor.

Figure 17. X2Y_Mount Tab



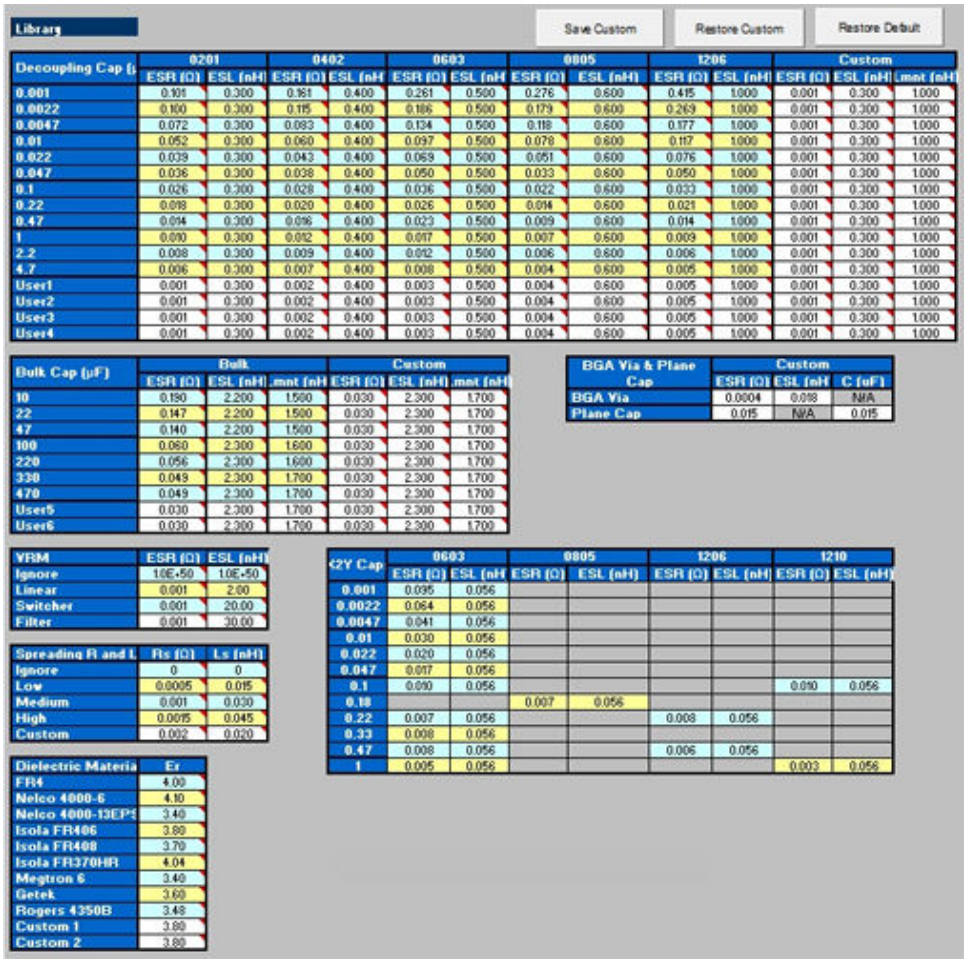
X2Y CAP Mounting Inductance	Units	0603	0805	1206	1210
Metal Thickness (t)	mils	0.60	0.60	0.60	0.60
Height above reference plane (h)	mils	3.60	3.60	3.60	3.60
Pad to Via trace width (W)	mils	20.00	20.00	20.00	20.00
Via radius (half of drill size) - r	mils	5.00	5.00	5.00	5.00
Center to Center Spacing (G1 - G2) Vias	mils	90.00	80.00	120.00	160.00
Center to Center Spacing (A - B) Vias	mils	60.00	80.00	120.00	160.00
Long Axis spacing between G1/G2 and A/B Vias	mils	26.00	30.00	30.00	30.00
Top Via Length (C1)	mils	60.0	60.0	60.0	60.0
Bottom via length (C2)	mils	15.0	15.0	15.0	15.0
Power plane dielectric thickness (thk)	mils	2.7	2.7	2.7	2.7
X2Y Cap mounting inductance - Top	nH	0.400	0.334	0.375	0.428
X2Y Cap mounting inductance - Bottom	nH	0.170	0.158	0.166	0.275

Enter all the information relevant to your layout in the **X2Y CAP Mounting Inductance** table. The tool then provides a mounting inductance for an X2Y capacitor mounted on either the top or bottom layer of the board. You can save the changes made to the tab, restore the changes, or restore the tab back to the default settings.

1.2.2.7 Library

The **Library** tab stores all the device parameters that are referred to in the other tabs.

Figure 18. Library Tab



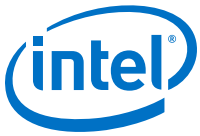
You can change each of the default values listed in the respective sections to meet the specific needs of your design.

1.2.2.7.1 Two-Terminal Decoupling Capacitors

The decoupling capacitors section contains the default ESR and ESL values for the various two-terminal capacitors in the following footprints:

- 0201
- 0402
- 0603
- 0805
- 1206

You also have the option to either modify the default values or enter your own commonly used custom values in the **Custom** field. If you are using a capacitor with a footprint that is not available in the tool, you must use the **Custom** field to enter the capacitor parasitics and the corresponding mounting inductance.



The decoupling capacitors section also provides the option for the user defined capacitors (such as User1 through User4). You can define the ESR and ESL parasitics for the various footprints and enter the corresponding capacitor value in the **System_Decap** tab. Choose the corresponding footprint when defining the capacitor values.

1.2.2.7.2 Bulk Capacitors

The bulk capacitors section contains the commonly used capacitor values for decoupling the power supply at mid and low frequencies. You can change the default values to reflect the parameters specific to the design.

1.2.2.7.3 X2Y Decoupling Capacitors

The X2Y decoupling capacitors section contains the default ESR and ESL values for the various X2Y capacitors in the 0603, 0805, 1206, and 1210 footprints. You also can replace the default ESR and ESL values with your own commonly used custom values.

1.2.2.7.4 BGA Via and Plane Capacitance

This section allows you to directly enter the values for effective via loop inductance under the BGA and plane capacitance during the pre-layout phase when no design-specific information is available.

If you have access to design-specific information, you can ignore this section and enter the design-specific information in the **Plane Cap** and **BGA Via** tabs that calculate the plane capacitance and the BGA via parasitics, respectively.

1.2.2.7.5 VRM Library

The VRM section lists the default values for both the linear and switcher regulators. In the **Custom** field, you can change the VRM parasitics listed under the linear/switcher rows or add the custom parasitics for the VRM relevant to the design.

1.2.2.7.6 Spreading R and L Parasitics

This library provides various options for the default effective spreading inductance values that the decoupling capacitors see with respect to the FPGA. These values are based on the quality of the PDN design. You can choose a **Low** value of effective spreading inductance if you have optimally designed your PDN Network. Optimum PDN design involves implementing the following design rules:

- PCB stackup that provides a wide solid power/ground sandwich for a given supply with a thin dielectric between the planes. This minimizes the current loop, which reduces the spreading inductance. The thickness of the dielectric material between the power/ground pair directly influences the amount of spreading/loop inductance that a decoupling cap can see with respect to the FPGA.
- Placing the capacitors closer to the FPGA from an electrical standpoint.
- Minimizing via perforations in the power/ground sandwich in the current path from the decoupling caps to the FPGA device.

Due to layout and design constraints, the PDN design may not be optimal. In this case, you can choose either a **Medium** or **High** value of spreading R and L. You can also change the default values or use the **Custom** field listed in the library specific to the design.

1.2.2.7.7 Dielectric Material Library

This library lists the dielectric constant values for the various commonly used dielectric materials. These values are used in the plane capacitance calculations listed under the **Plane_Cap** tab. You can change the values listed in this section.

If you change the default values listed in the various sections in the **Library** tab, you can save the changes by clicking **Save Custom**. You can restore the default library by clicking **Restore Default** located at the top right-hand corner of the **Library** page. You can also restore the saved custom library by clicking **Restore Custom**.

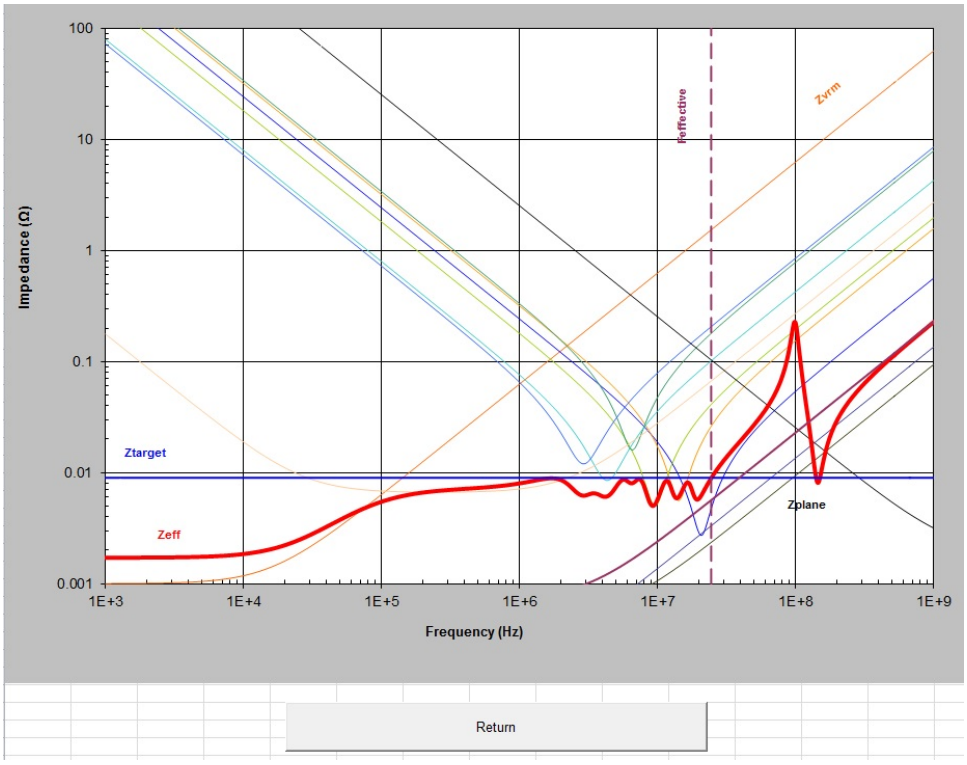
1.2.2.7.8 User Set $F_{EFFECTIVE}$

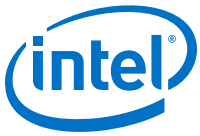
You must decouple to a $F_{EFFECTIVE}$ higher than what is calculated for the power rails of some device families. In this case, you must set the $F_{EFFECTIVE}$ option to **Override** in the **System_Decap** tab. The PDN tool 2.0 then uses the $F_{EFFECTIVE}$ value entered here.

1.2.2.8 Enlarged_Graph

In the **Enlarged_Graph** tab, you can view the enlarged Z-profile plot. The PDN tool 2.0 switches to this tab when you click on the Z-profile plot in the **System_Decap** tab. You can go back to the **System_Decap** tab when you click the **Return** button.

Figure 19. Enlarged_Graph Tab





1.2.3 Design PCB Decoupling Using the PDN Tool 2.0

PCB decoupling keeps the PDN Z_{EFF} smaller than Z_{TARGET} with the properly chosen PCB capacitor combination up to the frequency where the capacitance on the package and die take over the PDN decoupling. This procedure uses the PDN tool 2.0 in different power rail configurations and provides design examples using the Stratix 10 device PDN tool.

1.2.3.1 Pre-Layout Instructions

The PDN tool 2.0 provides an accurate estimate of the number and types of capacitors needed to design a robust power delivery network, regardless of where you are in the design phase. However, the accuracy of the results depends highly on the user inputs for the various parameters.

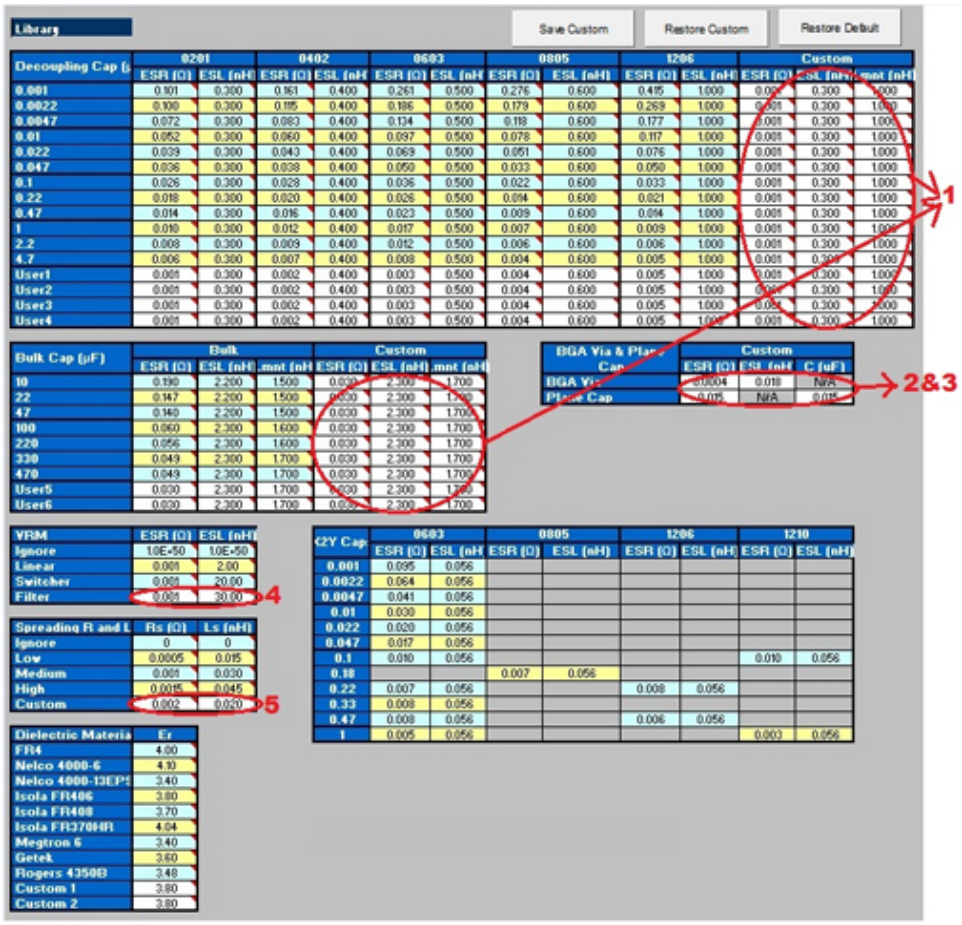
If you have finalized the board stackup and have access to board database and layout information, you can proceed through the tabs and enter the required information to arrive at an accurate decoupling scheme.

In the pre-layout phase of the design cycle when you do not have specific information about the board stack-up and board layout, you can follow these instructions to explore the solution space when finalizing key design parameters such as stackup, plane size, capacitor count, capacitor orientation, and so on.

In the pre-layout phase, ignore the **Plane Cap** and **Cap Mount** tabs and go directly to the **Library** tab when you do not have the layout information. If available, enter the values shown below in the **Library** tab. To use the default values, go directly to the **System_Decap** tab to begin the analysis.

Figure 20. Library Tab Fields

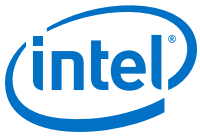
The callouts correspond to the fields in which you must enter values.



1. Enter the ESR, ESL, and Lmnt values for the capacitors listed in the **Custom** field.
2. Enter the effective BGA via parasitics for the power supply being decoupled in the **BGA Via & Plane Cap** field..
3. Enter the plane capacitance seen by the power/ground plane pair on the board for the power supply in the **BGA Via & Plane Cap** field.
4. Enter the VRM parasitics, if available, in the **Custom** row of the **VRM** field.
5. Enter the effective spreading inductance seen by the decoupling capacitors in the **Custom** row of the **Spreading R and L** field.

1.2.3.2 Deriving Decoupling in a Single-Rail Scenario

A power supply connects to only one power rail on the FPGA device in a single-rail scenario. The PDN noise is created by the dynamic current change of the single rail. You determine Z_{TARGET} and $F_{EFFECTIVE}$ based on the parameters related to the selected rail only.



The PDN tool 2.0 provides two ways to derive a decoupling network. You can set up the tool with the information needed and let the tool derive the PDN decoupling for your system. You can also manually enter the information and derive decoupling. To derive the desired capacitor combination:

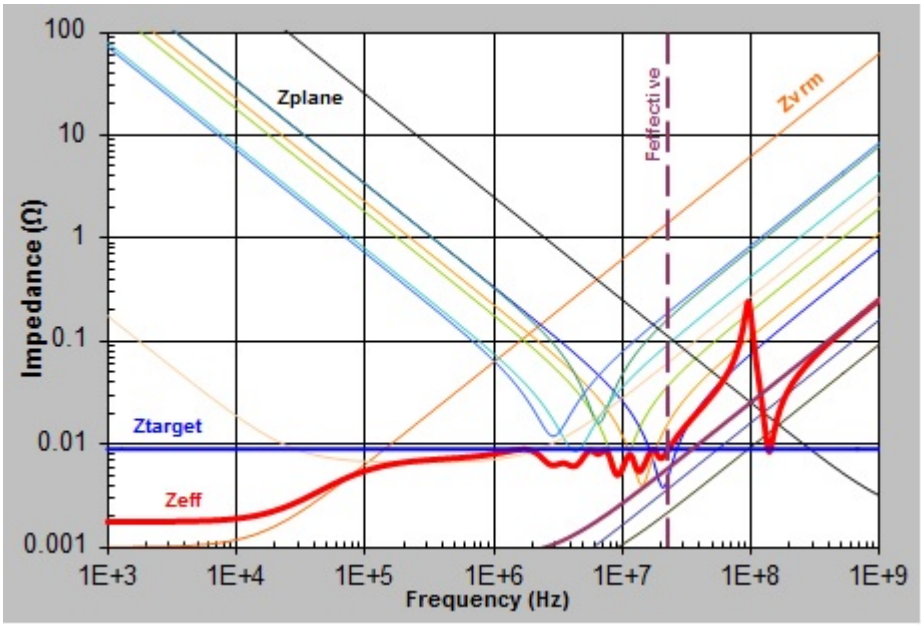
1. Select the device/power rail to work with.
2. Select the parameter settings for the PDN components.
3. Enter the electric parameters to set Z_{TARGET} and $F_{EFFECTIVE}$.
   You need to have a good estimate of the parameters entered to derive the proper decoupling guidelines (Z_{TARGET} and $F_{EFFECTIVE}$). Although you need to determine those guidelines based on the worst-case scenario, pessimistic settings result in hard-to-achieve guidelines and over design of your PCB decoupling.
4. Derive the PCB decoupling scheme.

   You must adjust the number and value of the PCB capacitors in the **Decoupling Capacitor (Mid/High Frequency)** and **Decoupling Capacitor (Bulk)** fields to keep the plotted Z_{EFF} below Z_{TARGET} until $F_{EFFECTIVE}$. You can derive the decoupling for the selected power rail manually. You can also select the **Auto Decouple** button and let the PDN tool 2.0 automatically determine a decoupling solution. If you are not able to find a capacitor combination that meets your design goal, you can try to change the parameters at 2 on page 29. For example, you can reduce the BGA via inductance used in the **Calculate** option by reducing the BGA via length in the **BGA_VIA** tab and using the **low** option for plane spreading. These changes reduce parasitic inductance and make it easier to achieve your decoupling goal. To achieve the low spreading setting, you must place the mid to high frequency PCB capacitors close to the FPGA device. You also must minimize the dielectric thickness between the power and ground plane. Refer to *Troubleshooting Z_{EFF}* if the Z_{EFF} is too high or the number of capacitors for decoupling becomes too high.

If you are not able to meet the Z_{TARGET} requirement with the changes above, the PDN in your design may have reached its physical limitation under the electrical parameters you entered for Z_{TARGET} and $F_{EFFECTIVE}$. You should re-examine these parameters to check if they are overly pessimistic.

Figure 21. Enlarged Plot of Z_{EFF}

This sample impedence plot is for a 1SG280LU_F50 VCC power rail. Assume that the minimum voltage supply is 0.8 V, $I_{dynamic}$ is 50 A, dynamic current change is 30% of $I_{dynamic}$, and the maximum allowable die noise tolerance is 5% of supply voltage. The VCC rail has 169 power BGA vias. The length of BGA via is assumed to be 20 mil.



The PDN tool 2.0 calculated that Z_{TARGET} is 0.0027 Ω and $F_{EFFECTIVE}$ is 13.58 MHz. The figure above shows one of the capacitor combinations that you can select to meet the design goal. As shown in the plot, Z_{EFF} remains under Z_{TARGET} up to $F_{EFFECTIVE}$. There are many combinations, but the ideal solution is to minimize the quantity and the type of capacitors needed to achieve a flat impedance profile below the Z_{TARGET}.

Related Links

Troubleshooting ZEFF on page 31

1.2.3.3 Deriving Decoupling in the Power-Sharing Scenarios

It is a common practice that several power rails in the FPGA device share the same power supply. For example, you can connect VCCPT, VCCA_PLL, and VCCA_FPLL rails that require the same supply voltage to the same PCB power plane. This can be required by the design, such as in the memory interface case. This can also come from the need to reduce bill of materials (BOM) cost. You can use the **System_Decap** tab to facilitate the decoupling design for the power sharing scenarios.

When deriving decoupling capacitors for multiple FPGAs sharing the same power plane, each FPGA should be analyzed separately using the PDN tool 2.0. For each FPGA design, combine the required power rails as described above and analyze the decoupling scheme as if the FPGA was the only device on the power rail, taking note of how the current is divided across the devices.

High frequency decoupling capacitors are meant to provide the current needed for AC transitions, and must be placed in a close proximity to the FPGA power pins. Thus, the PDN tool 2.0 should be used to derive the required decoupling capacitors for the unique power requirements for each FPGA on the board.

The power regulators must be able to supply the total combined current requirements for each load on the supply, but the decoupling capacitor selections should be analyzed on a single FPGA basis.

1.2.4 Troubleshooting Z_{EFF}

When the decoupling mode is set to **Auto**, this may result in a Z_{EFF} value that is too high. This can happen when the PCB parameters you entered result in an inefficient PDN, and the current to be decoupled by the PCB are unrealistically high.

With difficult PCB and current parameters, auto decoupling continues to add decoupling capacitors until it determines they have little effect. This results in hundreds of capacitors. You can achieve decoupling schemes with similar performance manually using far fewer capacitors.

1.2.4.1 Strategies for Correcting a High Z_{EFF}

As well as decoupling manually, you can reduce the decoupling burden by accurately estimating your current requirements and making your PCB more efficient. You may be able to achieve reduced PCB current requirements in the following ways:

- Estimating realistic current requirements in the PowerPlay Early Power Estimator (EPE).
- Entering realistic toggle rate figures for the logic in the EPE. Unrealistically high toggle rates dramatically increases dynamic current requirements.
- Entering realistic logic requirements in the EPE.
- Entering realistic clock frequencies in the EPE.
- Using the Quartus Prime software (PowerPlay Power Analyzer) PPPA and **.vcd** simulation entry for accurate current requirement estimation.
- Considering Root Sum Squared (RSS) averaging for shared power supply rails. Refer to the **Introduction** tab of the PDN tool for more information on this method.

You can make the PCB more efficient in the following ways:

- Increasing inter-plane capacitance of your Power (PWR) and Ground (GND) plane pair by reducing their dielectric thickness.
- Increasing inter-plane capacitance of your PWR and GND plane pair by increasing their surface area.
- Reducing loop inductance from the PWR and GND plane pair to the FPGA. You can do this by moving them closer to the surface of the PCB where the FPGA is mounted.
- Reducing loop inductance from the high frequency decoupling capacitors to the PWR and GND plane pair. You can do this by placing them on the surface of the PCB that is closest to the planes.
- Using Via On Side (VOS) instead of Via On End (VOE) capacitor mounting topologies to help at high frequencies.

- Using ultra-low Effective Series Inductance (ESL) mounting capacitors to help at high frequencies, for example, X2Y package style.
- Using ultra-low Effective Series Resistance (ESR) bulk capacitors to help at low frequencies.
- Considering larger vias with less ESL.

Realistic tool entry can make decoupling easier to achieve. The following factors affect the calculation of Z_{TARGET}:

- An increase in dynamic current reduces Z_{TARGET} and makes decoupling difficult to achieve. See the guidelines above.
- Enter realistic noise or ripple figures into the PDN tool. Use the noise figure listed in the device and rail specific table in the **Introduction** tab of the PDN Tool. Unrealistic ripple requirements reduce Z_{TARGET} and make decoupling difficult.
- Enter realistic transient % figures into the PDN tool. Use the transient % figure listed in the device and rail specific table in the **Introduction** tab of the PDN Tool. Unrealistic transient % requirements reduce Z_{TARGET} and make decoupling difficult.

The PDN Tool 2.0 includes the following new pessimism removal features to make decoupling the large core current manageable:

- Core clock frequency
- Current ramp up period

Note: These features are available only for the core rail.

1.3 Document Revision History

Date	Version	Changes
December 2016	2016.12.09	Made the following changes: • Added Stratix 10 device information globally. • Changed "Die Noise Tolerance" to "Noise Tolerance" globally. • Changed the "Settings for the Stratix 10 Device Power Rails" table to display the Stratix 10 specifications. • Changed the "Device Selection" figure to show Stratix 10 selections. • Changed the "Power Rail Configuration Scheme" figure to show Stratix 10 configurations. • Added a cross-reference to the *Stratix 10 GX and SX Device Family Pin Connection Guidelines* to the "Device Selection Section" topic. • Changed "Imax" to "Idynamic" in the "Power Rail Data and Configuration Section" topic. • Changed the "Power Rail Data and Power Sharing Scheme Section" figure to show Stratix 10 configurations. • Changed " root-mean-square" to " root-sum-square" in the "Power Rail Data and Configuration Section" topic. • Changed the "Changing Voltage for All Rails in a Group" figure to show Stratix 10 voltages. • Changed the note in the "VRM Data Section" topic. • Updated the options for the **Current Ramp Up Period** in the "Rail Group Summary Section" topic. • Changed the "Stackup Tab" figure to show Stratix 10 stackup information. • Removed the "Stackup Stub" section. • Changed the description of the "Enlarged Plot of Z_{EFF}" figure.

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Date	Version	Changes
		• Changed the PDN Tool 2.0 calculations in the "Deriving Decoupling in a Single-Rail Scenario" section. • Removed the following pessimism removal features from the "Strategies for Correcting a High Z_{EFF}" section: — Dynamic current change — Die noise tolerance • Added definition of Z_{EFF} to the "$F_{EFFECTIVE}$" section. • Added the **Ignore** option in the "VRM Impedance Section" section.
October 2016	2016.10.31	• Clarified the **Family/Device**, **Available Devices**, and **Power Rail Configuration** entry description. • Documented a new option to change a rail's voltage without disconnecting it from the regulator group. • Clarified the PDN tool's treatment of VRMs with sense lines. • Documented the **Default** option in the **BGA Via** table. • Described how to implement split planes.
June 2016	2016.06.15	Made the following changes: • Changed the description of how $F_{EFFECTIVE}$ is calculated in the "$F_{EFFECTIVE}$" section.
November 2015	2015.11.02	Made the following changes: • Changed the description in the "Overview" section. • Clarified the note in the "Z_{TARGET}" section. • Clarified the description in the "$F_{EFFECTIVE}$" section. • Changed the "Device Selection" figure. • Changed the "Power Rail Data and Power Sharing Scheme Section" figure. • Added a description for current usage of Imax in the "Power Rail Data and Configuration Section" section. • Added description to the "Results Summary Section" section. • Changed the "Results Summary Section of the System_Decap Tab" figure. • Changed the "BGA_Via Tab" figure. • Changed the "Plane_Cap Tab" figure. • Added description for the Import Plane R&C button in the "Plane_Cap" section. • Added description to the "Cap_Mount" section. • Changed the "Library Tab" figure. • Changed the "Library Tab Fields" figure. • Added list of pessimism removal features in the "Strategies for Correcting a High Z_{EFF}" section.
July 2015	2015.07.06	Made the following changes: • Changed the voltage for VCCH_GXB in the "Settings for the Arria 10 Device Power Rails" table.
March 2015	2015.03.06	Made the following changes: • Added MAX 10 to the list of supported devices in the *Overview* section. • Changed the "Device Selection" figure. • Clarified options for entering power supply voltage in the *Power Rail Data and Configuration Section* section. • Changed the "Power Rail Data and Power Sharing Scheme Section" figure.

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Date	Version	Changes
		• Added new parameters and descriptions to the *Rail Group Summary Section* section. • Added a note to the *Cap_Mount* section. • Added the *Troubleshooting* Z_{EFF} and *Strategies for Correcting High* Z_{EFF} sections.
September 2014	2014.09.29	• Added notes to the "PDN Topology Modeled as Part of the Tool" figure. • Added detailed explanation of the options availabe in the VRM Impedence pull-down menu in the "VRM Impedence Section."
September 2014	2014.09.12	Initial release.