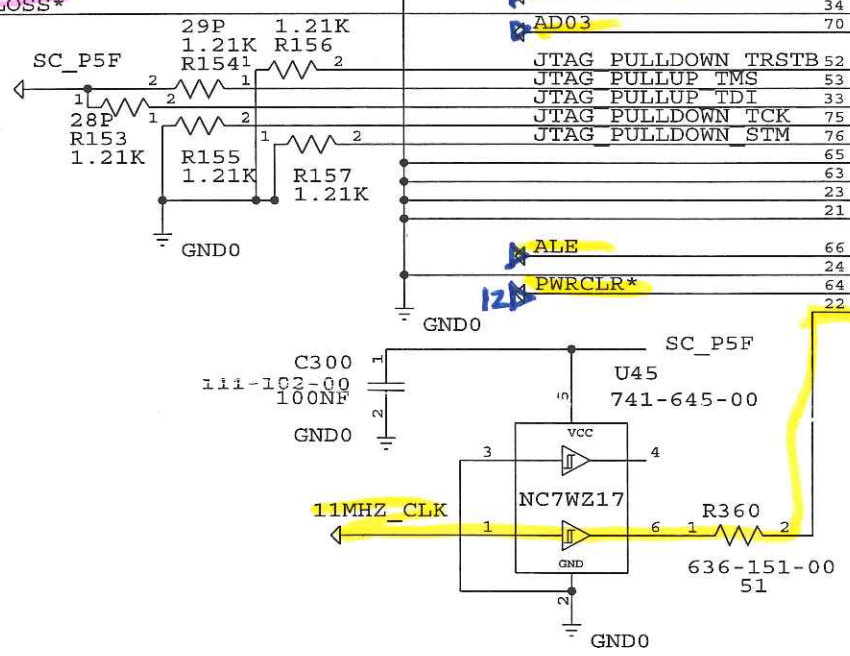
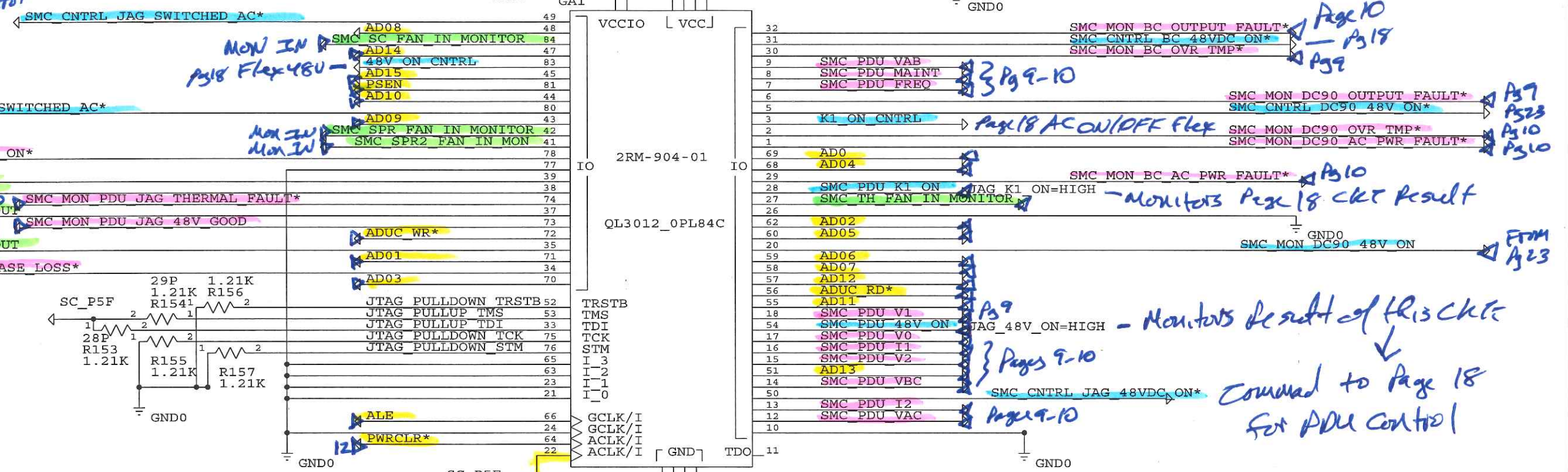
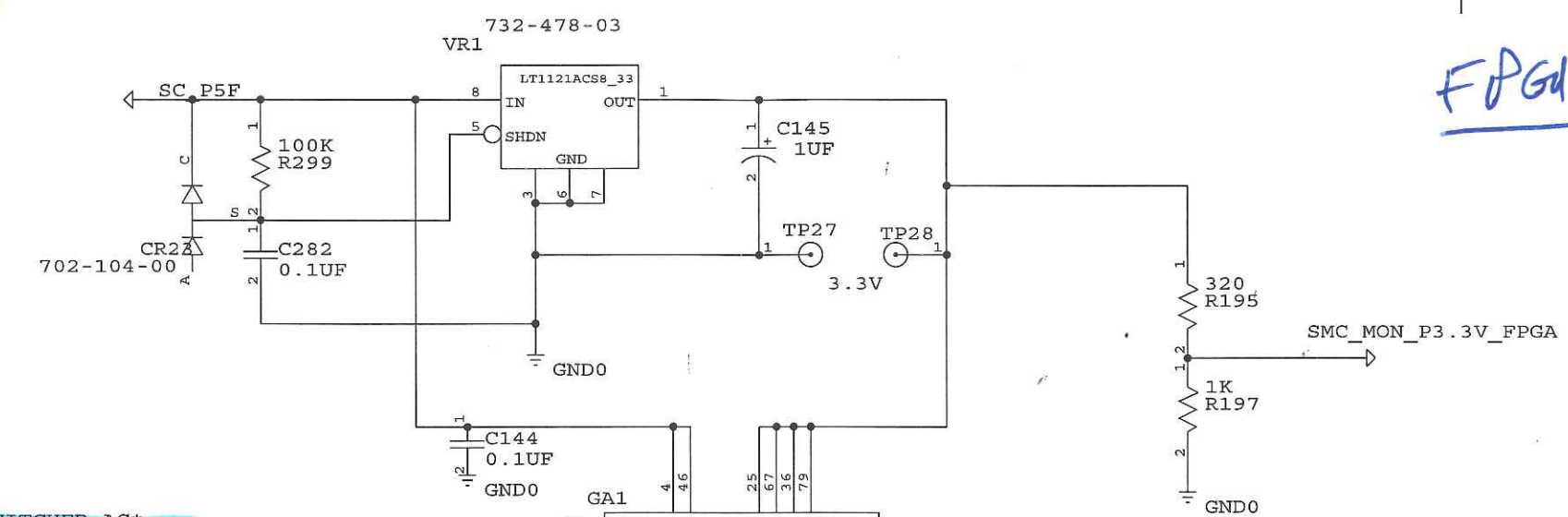


Addresses: To/From Rider Card

REVISIONS
SEE SHEET 1

FPGA = PDU & Fan Monitors

Page 18 - Pdu Control
Page 18 - AC Control
Page 18 - SMC MON BC AC ON*
Page 18 - SMC MON BC FAN1 STATE
Page 18 - SMC MON BC FAN0 STATE
Page 18 - SMC MON BC FAN1 TACH OUT
Page 18 - SMC MON BC FAN0 TACH OUT
Page 18 - SMC MON BC PHASE LOSS*



HARDWARE: OPEN: #01 + #03 357-290-00

Monitors result of this ckt
↓
Command to Page 18
for PDU control

FPGA

DRAWING
LA975
LAST_MODIFIED=Tue Sep 24 04:46:44 2013

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ENGINEER: ROBERT BROADBENT		SHEET 13 OF 26	