



EVB-LAN9692-LM

Hardware User's Guide

Microchip Information

Trademarks

The "Microchip" name and logo, the "M" logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries ("Microchip Trademarks"). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legalinformation/microchip-trademarks>.

ISBN: 979-8-3371-0914-5

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Table of Contents

Preface	6
Chapter 1. Overview	
1.1 Introduction	10
1.2 Audience	10
1.3 References	10
1.3.1 Microchip Documents	10
1.3.2 IEEE Standards	10
1.3.3 (Optical) Module Standards	10
1.4 Acronyms and Definitions	11
Chapter 2. EVB-LAN9692-LM Reference Board	
2.1 Introduction	13
2.2 Board Features	13
2.3 Board Design	13
2.4 CPU Subsystem	14
2.4.1 Embedded CPU Subsystem	14
2.4.2 External CPU Connectors	14
2.5 Management	14
2.6 Copper PHYs	14
2.7 Timing and Synchronization	14
2.7.1 SyncE	14
2.7.2 PTP/IEEE1588v2/802.1AS-2020	14
2.8 Power Usage	15
Chapter 3. Management Software	
3.1 Introduction	16
3.2 Software Features	16
3.2.1 Networking Features	16
3.2.2 Management	17
3.3 Firmware Update using TF-A	17
3.4 VelocityDRIVE™ SP Logfile	20
3.5 Using Firmware Update to Upload PCIe Driver	23
Chapter 4. LED Indicators and Board Connector	
4.1 Front Layout	25
4.1.1 T1 PHYs and Port Status LEDs	25
4.1.2 SFP+ Slots	25
4.2 Rear-side Layout	26
4.2.1 Power Switch and LEDs	26
4.2.2 Power Jack	26
4.2.3 PCIe 2.0 – OCuLink Connector	26
4.2.4 SMA Connectors Used for 1PPS Input and Output	26

4.2.5 Management Port and Status LED	26
4.2.6 USB 2.0 Type-C Serial Port	27
4.2.7 Reset Button	27
4.2.8 Board Status and Reset LEDs	27
4.3 Additional On-board Connectors	27
4.3.1 Expansion Header	27
4.3.2 ARM CPU JTAG Connector	28
4.3.3 QSPI Flash Program Header, 1.8V	28
4.3.4 On-die Temperature Sensor Header	28
4.4 Boot Mode and Reference Clock	28

Chapter 5. Detailed Hardware Description

5.1 Block Diagram	29
5.2 VCore-IV CPU Subsystem	30
5.2.1 VCore Configuration Strapping	30
5.2.2 Clock Source Configuration Strapping	30
5.2.3 eMMC NAND Flash	30
5.2.4 QSPI NOR Flash	31
5.2.5 QSPI Flash Programming	31
5.2.6 ARM CPU JTAG Header	32
5.2.7 FLEXCOM Usage	33
5.2.7.1 FLEXCOM0 UART for TF-A Monitor and trace output	33
5.2.7.2 FLEXCOM1 I ² C Interface	34
5.2.8 Serial GPIO Controller	34
5.2.9 MII-Management Controllers	36
5.2.9.1 PHY Shared Interrupts Pins on GPIO	36
5.2.10 LAN9692 GPIO Usage	37
5.3 Switch Core	38
5.3.1 Network Ports	38
5.3.2 LAN8840 Copper PHY	39
5.3.2.1 Media Side Interface	39
5.3.2.2 Integrated Magnetics – ICM	39
5.3.2.3 Port LEDs	39
5.3.2.4 PHY GPIO Usage	40
5.3.3 LAN8870 Copper PHY	40
5.3.3.1 Media Side Interface - EMC-ESD Network	40
5.3.3.2 TC10 - Low-Power Remote Sleep and Wake-Up Support	41
5.3.3.3 Port LEDs	42
5.3.3.4 PHY GPIO Mapping and Strapping	43
5.3.4 SFP+, SFI Interfaces	43
5.3.5 PCIe 2.0 End-point	43
5.4 Reference Clocks, Synchronization, and PTP	44
5.4.1 Switch and CuPHY Reference Clocks	44
5.4.2 PTP Engines	45
5.4.3 SMA Connectors	45
5.5 Reset Circuitry	46
5.6 Expansion Header	46
5.7 Power Distribution	47
5.7.1 DC/DC Converters	47
5.7.2 Power Supply Sequencing	48

5.7.3 Power Supply, Test Points and LEDs	49
Chapter 6. Environmental Requirements	
6.1 Storage and Operating Conditions	50
Appendix A. PCB Layout	
A.1 Dimension	52
A.2 PCB Layers	52
A.2.1 Layer 1 – Top Layer	53
A.2.2 Layer 2 – Ground Layer	54
A.2.3 Layer 3 – Combined Power and Ground Layer	55
A.2.4 Layer 4 – Bottom Layer	56
A.3 PCB Layer Stack-up	57
A.3.1 PCB Trace Widths, Clearance, and Impedance	57

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXA”, where “XXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9692-LM Hardware User’s Guide. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [Warranty Registration](#)
- [The Microchip Website](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

The manual layout is as follows:

- [Chapter 1. “Overview”](#) – This chapter provides an overview of the additional documentation needed.
- [Chapter 2. “EVB-LAN9692-LM Reference Board”](#) – This chapter provides a brief overview of the EVB-LAN9692 and its main features.
- [Chapter 3. “Management Software”](#) – This chapter provides information on the software management of the EVB-LAN9692-LM.
- [Chapter 4. “LED Indicators and Board Connector”](#) – This chapter is a short walk-through on identifying board connectors and LEDs.
- [Chapter 5. “Detailed Hardware Description”](#) – This chapter describes the hardware details of the EVB-LAN9692-LM.
- [Chapter 6. “Environmental Requirements”](#) – This chapter describes the environmental requirements.
- [Appendix A. “PCB Layout”](#) – This section shows the different PCB layers, especially the routing to the DDR RAM.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB® IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<i>File>Save</i>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending the Warranty Registration Card entitles users to receive new product updates. Interim software releases are available at the Microchip website.

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

DEVELOPMENT SYSTEMS CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip website at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLAB C compilers; all MPLAB assemblers (including MPASM assembler); all MPLAB linkers (including MPLINK object linker); and all MPLAB librarians (including MPLIB object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:

<http://www.microchip.com/support>

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003848B (04-10-25)	Cover	VelocityDRIVE™ logo added
	Section 3.1 “Introduction”	Added a note encouraging customers to review each software release for new features in the ‘Release Note’ section of the Microchip Velocity DriveSP Documentation.
DS50003848A (03-06-25)	All	Initial release

Chapter 1. Overview

1.1 INTRODUCTION

This document describes the design of the EVB-LAN9692-LM reference board, demonstrating the Automotive TSN Ethernet Switch architecture. The LAN9692 has a total bridging bandwidth of 66 Gbit/s.

Regarding basic board design, the LAN9692 and other derivatives, such as the LAN9691 and LAN9693 are all very similar devices. They use the same BGA package, pin layout, number of SerDes macros and types, and incorporate the VCore-IV CPU subsystem and associated interfaces. The main difference is the maximum bridging bandwidth supported.

1.2 AUDIENCE

This document is developed primarily for hardware and software engineers who want to get an overview of designing products based on the LAN9692 or its derivatives.

1.3 REFERENCES

1.3.1 Microchip Documents

Concepts and materials available in the following references may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *EVB-LAN9692-LM Reference Schematic Design (Schematic)*
- *LAN9691/LAN9692/LAN9693 Data Sheet (DS00005047)*
- *LAN8840 Data Sheet (DS00004727)*
- *LAN8870/LAN8871/LAN8872 Data Sheet (DS00004828)*
- *ENT-AN1187 Using the Serial GPIO/LED Controller*

1.3.2 IEEE Standards

- IEEE802.1D, Media Access Control Bridges
- IEEE802.1Q, Virtual Bridged Local Area Networks
- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification
- IEEE1588-2019, Precision Clock Synchronization Protocol

1.3.3 (Optical) Module Standards

- SFP+ MSA, [ftp://ftp.seagate.com/sff/SFF-8431.PDF](http://ftp.seagate.com/sff/SFF-8431.PDF)

1.4 ACRONYMS AND DEFINITIONS

TABLE 1-1: ACRONYMS AND DEFINITIONS

Term	Definition
AMS	Automatic Media-Sense
CLI	Command Line Interface
EMI	Electromagnetic Interference (emissions)
GUI	Graphical User Interface
ICM	RJ45 connector with Integrated Magnetics
JTAG	Joint Test Access Group (IEEE1149)
LVDS	Low-Voltage Differential Signaling
LVTTL	Low-Voltage TTL
NPI	Node Processor Interface
PCS	Physical Coding Sublayer
PHY	Physical layer device
PTP	Precision Time Protocol (IEEE1588)
SFP	Small Form-factor Pluggable transceiver
SFP+	Small Form-factor Pluggable transceiver for 10 Gbps
SI	Serial Interface (SPI)
SME	Small/Medium Enterprise
SSM	Synchronization Status Message
Sync-E	Synchronous Ethernet (ITU-T G.8262/Y.1362)
TF-A	Trusted Firmware for ARM
TWI	Two-Wire Interface

NOTES:

Chapter 2. EVB-LAN9692-LM Reference Board

2.1 INTRODUCTION

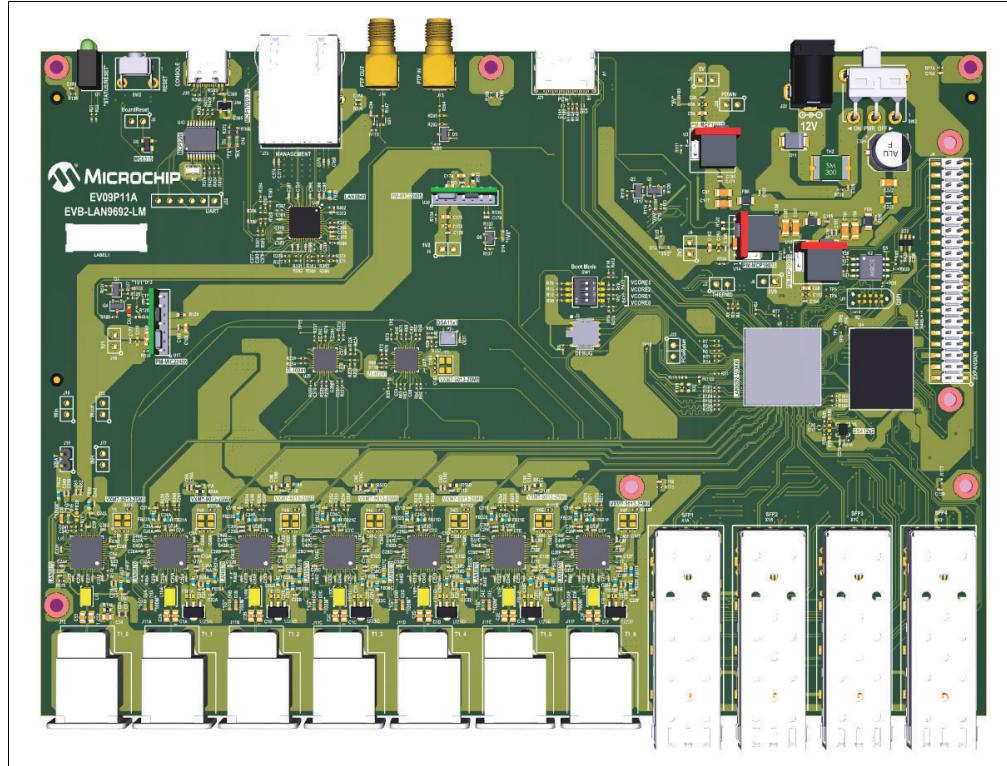
This chapter provides an overview of the EVB-LAN9692-LM reference board features, software and hardware. Refer to [Figure 5-1](#) for details on the board block diagram.

2.2 BOARD FEATURES

- One LAN9692 Automotive TSN Switch
- Four SFP+ module slots directly connected to LAN9692
- Seven MATEnet front ports using LAN8870 supporting 100/1000Base-T1
- Management port using LAN8840 supporting 10/1000Base-T and 100Base-Tx
- Serial UART port (USB-C) for local management and software debugging
- Two SMA connectors for 1PPS input and output clocks
- JTAG/Debug pin header
- Option for external CPU control via PCIe 2.0 OCuLink connector or SPI client
- Expansion pin header – partially Raspberry Pi compatible regarding Power, UART and I²C
- Standard 12V DC powered input Jack (5.5mm/2.5mm center pin)

2.3 BOARD DESIGN

FIGURE 2-1: EVB-LAN9692-LM REFERENCE BOARD



2.4 CPU SUBSYSTEM

2.4.1 Embedded CPU Subsystem

By default, LAN9692 is managed through its embedded CPU subsystem.

- Embedded ARM Cortex-A53 single core 64-bit processor operating at 1 GHz
- Internal 2 MByte ECC SRAM memory
- 8MB QSPI NOR
- 4 GB eMMC NAND (the eMMC is not supported by the SW)
- Some GPIOs are implemented through the CPU subsystem serial GPIO engine for control signals to the four SFP+ slots and for LED control

2.4.2 External CPU Connectors

An external host CPU system can optionally control the LAN9692 Switch through:

- PCIe 2.0 cable connector (OCuLink)
- SPI client located in the Expansion header (or the QSPI Programming header)

The SPI client is set up through a specific boot mode. The PCIe end-point can either be set up through the SPI client or from a QSPI boot NOR Flash device.

2.5 MANAGEMENT

The embedded CPU subsystem is intended to boot and run a Lightly Managed Switch Application called VelocityDRIVE™ SP. Using this application, the Switch can be managed through the machine interface CORECONF/YANG. A graphical UI called VelocityDRIVE CT is available for manual configuration and management.

The embedded CPU firmware includes a Secure Boot Manager, from where the reference board can be brought up through a browser-based Firmware Update utility program called FWU.html. Hereby the NOR and eMMC Flashes can be (pre)programmed with the Lightly Managed application.

The Firmware Update utility uses the Switch serial UART interface located on Flex-com0, which is provided through the USB-C connector.

2.6 COPPER PHYS

The Ethernet copper ports are composed of the following single PHY's. Both PHYs supports Frame pre-emption and PHY time-stamping.

- LAN8870, 100Base-T1/1000Base-T1
- LAN8840, 10Base-T/100Base-Tx/1000Base-Tx

2.7 TIMING AND SYNCHRONIZATION

2.7.1 SyncE

The EVB-LAN9692-LM reference board does not support SyncE.

2.7.2 PTP/IEEE1588v2/802.1AS-2020

Precision Time Protocol (PTP) interfacing is available through all Ethernet ports with high accuracy timestamping in either the CuPHY or Switch, and through input and output of 1PPS SMA connectors.

The LAN9692 can be configured as boundary clock or transparent clock. LAN9692 can support both one-step and two-step operations. Likewise, multiple time domains are also supported.

2.8 POWER USAGE

The reference board is powered through a standard 12V DC barrel jack. A two-position switch is used for ON/OFF operation.

Table 2-1 shows the DC/DC power supplies being used on the board.

TABLE 2-1: DC/DC POWER SUPPLIES USAGE

Source	DC/DC Converter	Supply Used By
12V	0.9V up to 6.7A	LAN9692 Switch core and 10G SerDes I/O
	3.3V up to 3.5A	LAN8870/LAN8840, eMMC, USB, DC/DC and SFP+
	5V up to 1.2A	DC/DC converters (and Expansion header)
5V	1.1V up to 3.0A	LAN8870/LAN8840 PHY core and analog low
	1.8V up to 1.2A	LAN9692: VDDIO, VDDH, VDDPLLDDR LAN8870: VDDIO
3.3V	6x 2.5V up to 20 mA	LAN8870: VP_H, SGMII supply (Local LDO)

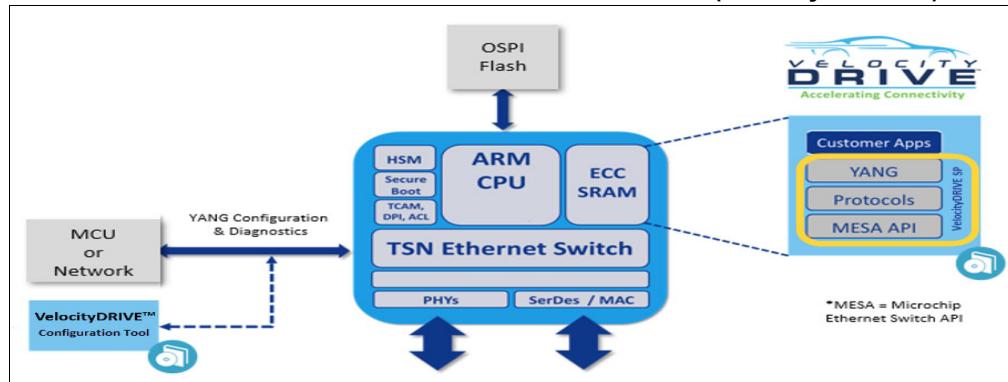
The expansion header can supply both 3.3V up to 2A and 5V up to 2A power.

Chapter 3. Management Software

3.1 INTRODUCTION

The EVB-LAN9692-LM reference board is locally running a Lightly Managed Switch application called VelocityDRIVE SP. It is a software framework designed to run on CPU/memory-constrained systems and is built on top of the MESA API. It is intended for automotive and industrial applications. See [Figure 3-1](#).

FIGURE 3-1: EMBEDDED SOFTWARE SOLUTION (VelocityDRIVE™)



The Lightly Managed application offers a CORECONF/YANG based management interface, which implements selected leaves from standardized YANG models and Microchip defined YANGs. The application is managed remotely by a Linux-based graphical UI called VelocityDRIVE CT. Refer to the VelocityDRIVE CT release notes for a list of supported YANG attributes.

The offered SW stack can be customized to other board variants. Most common board changes can be accommodated using the Device Tree hardware configuration mechanisms. The effort depends on how much a given design differs from the already supported reference boards.

Customers are encouraged to review each software release for new features in the ‘Release Note’ section of:

<https://microchip-ung.github.io/velocitydrivesp-documentation/>

3.2 SOFTWARE FEATURES

3.2.1 Networking Features

- 802.1AS-Relay with MAC-based timestamping
- Link Aggregation and LACP
- Port settings, status and statistics
- 802.1Q Mac-table and VLAN support
- QoS queue classification
- Credit based shaping
- Port Mirroring
- LLDP (Link Layer Discovery Protocol)

- TAS (Time Aware Shaper)
- PSFP (Per Stream Filtering and Policing)

3.2.2 Management

- Serial/UART based management via MUP1 (Microchip UART Protocol 1)
- In-band IPv4 based host interface
- CoAP Server
- Firmware update
- YANG/CORECONF status, configuration and RPC support
- CORECONF data-stores: start-up config and running-config
- DTLS for CoAP over IP
- DHCPv4 Client support

3.3 FIRMWARE UPDATE USING TF-A

A browser-based update utility called fwu.html allows a simple approach for recovering or updating the firmware image on the EVB-LAN9692-LM. Complete the following steps for a firmware update:

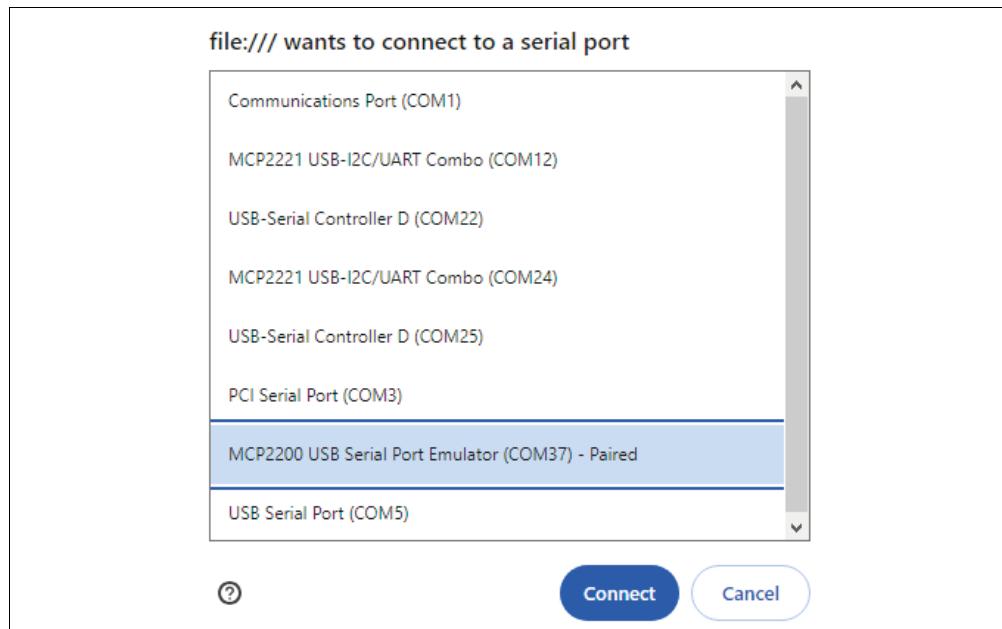
1. The board can be connected directly to the USB port of a PC using a standard USB-A to USB-C cable to access the built-in Secure boot manager. The USB driver software (Windows, Mac, Linux) is found at <https://www.microchip.com/wwwproducts/en/MCP2200>.
2. When connected through the USB connector, the PC detects the on-board USB device, which includes giving the connection a COMx port number. From here, the port behaves like a standard serial port.
3. To have the fwu.html communicating with LAN9692, the reference board SW1 boot strapping must be set to '1010' for 115200 baud or '1011' for 921600 baud. See [Table 5-1](#). The built-in bootstrap manager, BL1 will enable the FLEXCOM0 UART interface (connected to the USB port) on the next boot-up.
4. To get the latest fwu.html file, go to <https://github.com/microchip-ung/arm-trusted-firmware> and click on the **Latest** button. Download fwu-lan969x_a0-release.html and lan969x_EV09P11A.img.
5. Make sure that the board USB port is not connected to a terminal server. If it is, then the HTML script will not work. A restart of the HTML script may be necessary.
6. Use either Chrome or MS Edge browser and have the browser setting, JavaScript, enabled. Simply run the fwu.html file inside the browser address field. See [Figure 3-3](#).

FIGURE 3-2: CONNECTING TO LAN9692 SECURE BOOT MANAGER



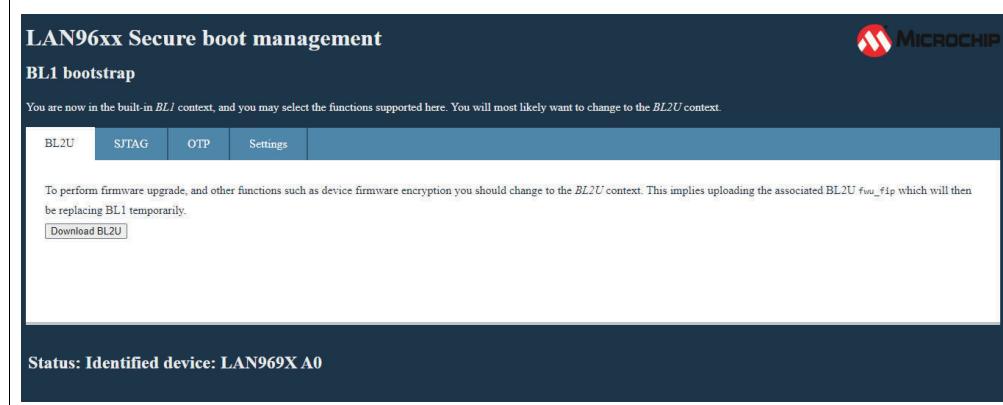
7. Click the **Connect device** button. The dialogue in [Figure 3-3](#) appears.
8. Select MCP2200 and click on **Connect**.

FIGURE 3-3: COM PORT SELECTION



9. [Figure 3-4](#) displays after clicking **Connect**. Click on **Download BL2U** to get the firmware update functions.

FIGURE 3-4: BL1 BOOTSTRAP PAGE



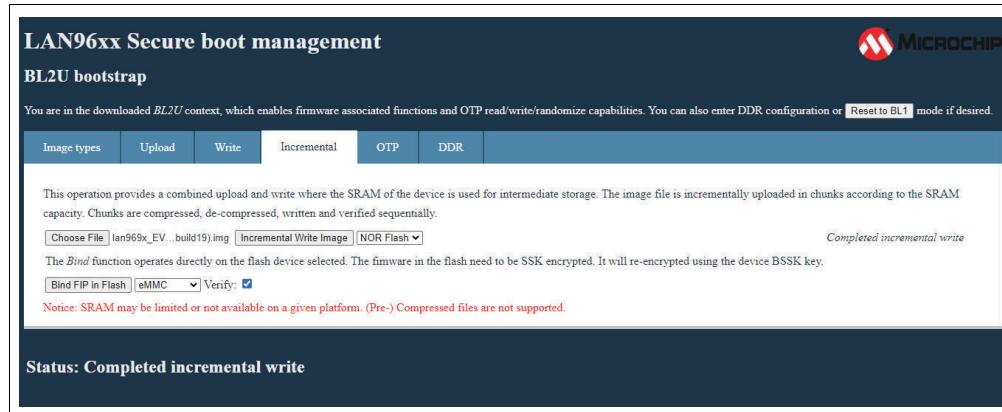
10. Within the BL2U monitor, click **Incremental** tab in order to load an image. See [Figure 3-5](#).

FIGURE 3-5: BL2U BOOTSTRAP PAGE



11. Click **Choose File** and select the previously collected file lan969x_EV09P11A.img.
12. Select **NOR Flash** as shown in [Figure 3-6](#) and then click **Incremental Write Image**. This will upload the file in small chunks to the internal SRAM and do a partial programming of the NOR Flash. The Flash programming will take about 30 seconds.

FIGURE 3-6: BL2U – INCREMENTAL FLASH PROGRAMMING



13. Once the NOR Flash programming is done, change SW1 DIP-switch back to '0001' and reset the board to bootup from the NOR Flash.
14. To release the COM port, F5 must be issued to update the browser page.

3.4 VelocityDRIVE™ SP LOGFILE

Now running a terminal program on a PC, which is connected to the board USB-C port, the below output will be shown:

```
NOTICE: Booting Trusted Firmware
NOTICE: BL1: v2.6(release):lan969x-a0-bl1-rc2
NOTICE: BL1: Built : 11:04:40, Feb 8 2023
INFO: BL1: RAM 0x2f0000 - 0x2ff000
INFO: Using crypto library 'LAN969X crypto core'
INFO: QSPI0 running at 25 Mhz
WARNING: Failed to access image id=28 (-2)
ERROR: No 'fip' partition found
WARNING: Failed to obtain reference to image id=0 (-22)
WARNING: Failed to obtain reference to image id=6 (-2)
NOTICE: Image(6) load error: -2
ERROR: No 'fip.bak' partition found
WARNING: Failed to obtain reference to image id=0 (-22)
WARNING: Failed to obtain reference to image id=6 (-2)
NOTICE: Image(6) load error: -2
NOTICE: Assuming FIP start at device origin
INFO: Loading image id=6 at address 0x2f4600
INFO: Image id=6 loaded: 0x2f4600 - 0x2f48ca
INFO: Authenticating image id=6 (sign)
NOTICE: ROTPK is not deployed on platform. Skipping ROTPK verification.
INFO: Authenticated image id=6 (sign) = 0
INFO: Authenticating image id=6 (ctr 1.3.6.1.4.1.4128.2100.1)
INFO: Authenticated image id=6 (ctr 1.3.6.1.4.1.4128.2100.1) = 0
INFO: Loading image id=31 at address 0x2f4600
INFO: Image id=31 loaded: 0x2f4600 - 0x2f4fba
INFO: Authenticating image id=31 (hash)
INFO: Authenticated image id=31 (hash) = 0
```

```
INFO:     BL1: Loading BL2
ERROR:    No 'fip' partition found
WARNING:   Failed to obtain reference to image id=0 (-22)
WARNING:   Failed to obtain reference to image id=30 (-2)
WARNING:   Failed to obtain reference to image id=0 (-22)
WARNING:   Failed to obtain reference to image id=1 (-2)
NOTICE:   Image(1) load error: -2
ERROR:    No 'fip.bak' partition found
WARNING:   Failed to obtain reference to image id=0 (-22)
WARNING:   Failed to obtain reference to image id=6 (-2)
NOTICE:   Image(6) load error: -2
NOTICE:   Assuming FIP start at device origin
INFO:    Loading image id=6 at address 0x100000
INFO:    Image id=6 loaded: 0x100000 - 0x1002ca
INFO:    Authenticating image id=6 (sign)
NOTICE:   ROTPK is not deployed on platform. Skipping ROTPK
verification.
INFO:    Authenticated image id=6 (sign) = 0
INFO:    Authenticating image id=6 (ctr 1.3.6.1.4.1.4128.2100.1)
INFO:    Authenticated image id=6 (ctr 1.3.6.1.4.1.4128.2100.1) = 0
WARNING:  Failed to obtain reference to image id=30 (-2)
INFO:    Loading image id=1 at address 0x100000
INFO:    Image id=1 loaded: 0x100000 - 0x116268
INFO:    Authenticating image id=1 (hash)
INFO:    Authenticated image id=1 (hash) = 0
NOTICE:   BL1: Booting BL2
INFO:    Entry point address = 0x100000
INFO:    SPSR = 0x3c5
INFO:    Running on platform build: 0x00000000
NOTICE:   BL2: lts-v2.8.8(release):v2.8.8-mchp0-1-g4906fc357
NOTICE:   BL2: Built : 13:42:39, Jan 15 2024
INFO:    Using crypto library 'LAN969X crypto core'
INFO:    BL2: Doing platform setup
INFO:    QSPIO running at 100 Mhz
INFO:    QSPI: Using 1-4-4 quad mode
WARNING:  Failed to access image id=28 (-2)
INFO:    Configuring TrustZone
NOTICE:   Try FIP at offset 00020000
INFO:    BL2: Loading image id 3
INFO:    Loading image id=7 at address 0x200000
INFO:    Image id=7 loaded: 0x200000 - 0x200283
NOTICE:   Image(7) load error: 2
NOTICE:   Try FIP at offset 000f0000
INFO:    Loading image id=7 at address 0x200000
INFO:    Image id=7 loaded: 0x200000 - 0x200283
INFO:    Authenticating image id=7 (sign)
NOTICE:   ROTPK is not deployed on platform. Skipping ROTPK
verification.
INFO:    Authenticated image id=7 (sign) = 0
INFO:    Authenticating image id=7 (ctr 1.3.6.1.4.1.4128.2100.1)
INFO:    Authenticated image id=7 (ctr 1.3.6.1.4.1.4128.2100.1) = 0
INFO:    Loading image id=9 at address 0x200000
INFO:    Image id=9 loaded: 0x200000 - 0x20021d
INFO:    Authenticating image id=9 (sign)
INFO:    Authenticated image id=9 (sign) = 0
INFO:    Authenticating image id=9 (ctr 1.3.6.1.4.1.4128.2100.1)
INFO:    Authenticated image id=9 (ctr 1.3.6.1.4.1.4128.2100.1) = 0
INFO:    Loading image id=13 at address 0x200000
INFO:    Image id=13 loaded: 0x200000 - 0x200243
INFO:    Authenticating image id=13 (sign)
```

```
INFO: Authenticated image id=13 (sign) = 0
INFO: Authenticating image id=13 (ctr 1.3.6.1.4.1.4128.2100.1)
INFO: Authenticated image id=13 (ctr 1.3.6.1.4.1.4128.2100.1) = 0
INFO: Loading image id=3 at address 0x200000
INFO: Image id=3 loaded: 0x200000 - 0x2101f0
INFO: Authenticating image id=3 (hash)
INFO: Authenticated image id=3 (hash) = 0
NOTICE: Try FIP at offset 00020000
INFO: BL2: Loading image id 5
INFO: Loading image id=11 at address 0x220000
INFO: Image id=11 loaded: 0x220000 - 0x22022e
NOTICE: Image(11) load error: 2
INFO: AUTH: Invalidate parent image: 7
NOTICE: Try FIP at offset 000f0000
INFO: Loading image id=7 at address 0x220000
INFO: Image id=7 loaded: 0x220000 - 0x220283
INFO: Authenticating image id=7 (sign)
NOTICE: ROTPK is not deployed on platform. Skipping ROTPK
verification.
INFO: Authenticated image id=7 (sign) = 0
INFO: Authenticating image id=7 (ctr 1.3.6.1.4.1.4128.2100.1)
INFO: Authenticated image id=7 (ctr 1.3.6.1.4.1.4128.2100.1) = 0
INFO: Loading image id=11 at address 0x220000
INFO: Image id=11 loaded: 0x220000 - 0x22022e
INFO: Authenticating image id=11 (sign)
INFO: Authenticated image id=11 (sign) = 0
INFO: Authenticating image id=11 (ctr 1.3.6.1.4.1.4128.2100.2)
INFO: Authenticated image id=11 (ctr 1.3.6.1.4.1.4128.2100.2) = 0
INFO: Loading image id=15 at address 0x220000
INFO: Image id=15 loaded: 0x220000 - 0x220254
INFO: Authenticating image id=15 (sign)
INFO: Authenticated image id=15 (sign) = 0
INFO: Authenticating image id=15 (ctr 1.3.6.1.4.1.4128.2100.2)
INFO: Authenticated image id=15 (ctr 1.3.6.1.4.1.4128.2100.2) = 0
INFO: Loading image id=5 at address 0x220000
INFO: Image id=5 loaded: 0x220000 - 0x2ec000
INFO: Authenticating image id=5 (hash)
INFO: Authenticated image id=5 (hash) = 0
NOTICE: BL1: Booting BL31
INFO: Entry point address = 0x200000
INFO: SPSR = 0x3cd
NOTICE: BL31: lts-v2.8.8(release):v2.8.8-mchp0-1-g4906fc357
NOTICE: BL31: Built : 13:42:43, Jan 15 2024
INFO: ARM GICv2 driver initialized
NOTICE: Direct boot of BL33 binary image
INFO: BL31: Initializing runtime services
INFO: BL31: Preparing for EL3 exit to normal world
INFO: Entry point address = 0x220000
INFO: SPSR = 0x3c5
INFO: NS Runtime initialization performed now
>Tmain: start scheduler
                <<0cca
>T
    <b76f
>TPhy@0 Part number:0x1c Rev:2<<3c7f
>T
    <b76f
>TPhy@1 Part number:0x1c Rev:2<<3b7f
>T
    <b76f
```

```
>TPhy@2 Part number:0x1c Rev:2<<3a7f
>T
<b76f
>TPhy@3 Part number:0x1c Rev:2<<397f
>T
<b76f
>TPhy@4 Part number:0x1c Rev:2<<387f
>T
<b76f
>TPhy@5 Part number:0x1c Rev:2<<377f
>T
<b76f
>TPhy@6 Part number:0x1c Rev:2<<367f
>T
<b76f
>TPhy@11 Part number:0x2289 Rev:0<790d
>T
<b76f
>ALMSTAX-DEV-29-06d233e1-240513160438 0 300 2
                                         <<6cfe
>Tport 1 up at 1G-Fdx<a68d
>T
<b76f
>Tport 2 up at 1G-Fdx<a68c
>T
<b76f
>Tport 3 up at 1G-Fdx<a68b
>T
<b76f
>Tport 4 up at 1G-Fdx<a68a
>T
<b76f
>Tport 11 up at 1G-Fdx<<8442
>T
<b76f
```

Note: In above output >T means trace and >A means announcement.

The Lightly Managed application uses a machine protocol and is intended to run with a MCHP software utility called VelocityDRIVE CT. Once the DEV-xxx comes up, the Switch application has finish setting up ports and is then running to serve port link changes or external commands.

3.5 USING FIRMWARE UPDATE TO UPLOAD PCIE DRIVER

The LAN9692 can be controlled externally by using it as a PCIe end-point. The SerDes macro and PCIe controller are, however, not per default setup.

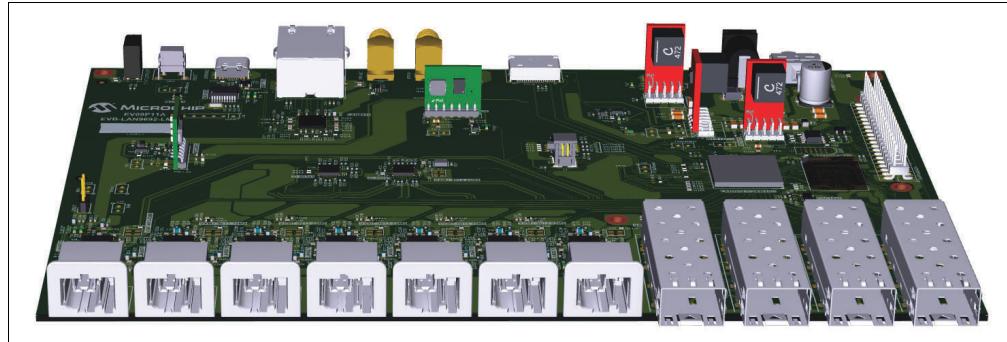
The Firmware update utility can be used to upload a special LAN969x_PCIE image to the NOR Flash. The image configures and enables the PCIe end-point interface. The bin file does not contain U-boot. The LAN969x_PCIE image is released along with the TFA software.

Chapter 4. LED Indicators and Board Connector

4.1 FRONT LAYOUT

Figure 4-1 shows the front layout of the EVB-LAN9692-LM reference board.

FIGURE 4-1: FRONT LAYOUT



4.1.1 T1 PHYs and Port Status LEDs

The reference board exposes 7x MATEnet connectors – one for each of the LAN8870 T1 PHYs.

The port status LEDs are located behind each connector and are automatically controlled by the T1 PHY itself. There is a 1G LED to indicate link/traffic (green solid/blinks) and a 100M LED to indicate 100M link/traffic (orange solid/blinks).

4.1.2 SFP+ Slots

The reference board has four SFP+ slots intended for 10G transceivers. Each slot is organized as a single module and connects directly to LAN9692 10G SerDes macro, S6-S9.

The SerDes macros supports a variety of interface standards such as SFI, 2500BASE-X, 1000Base-X and 100BASE-FX to optical SFP modules, as well as copper SFPs through either XFI, SGMII or 2.5G SGMII.

It is also possible to support 10GBase-KR, 5GBASE-KR, 2500Base-KX and 1000Base-KX by using DAC cabling.

Under each SFP slot a single bi-color LED (green/yellow) signals the current port status. The LED status indication is controlled through the Switch serial GPIO engine.

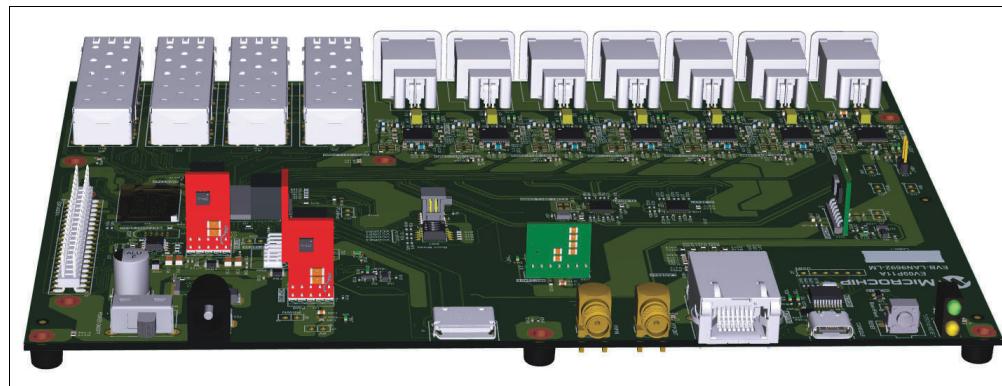
Likewise, the SFP MSA out-of-band control and monitoring of each SFP slot is also made through the Switch serial GPIO engine.

The SFP I²C required clock muxing is made by using an (external) 8-channel analog multiplexer. Three select pins are controlled through Switch GPIOs.

4.2 REAR-SIDE LAYOUT

[Figure 4-2](#) shows the rear-side layout of the EVB-LAN9692-LM Reference Board.

FIGURE 4-2: REAR-SIDE LAYOUT



4.2.1 Power Switch and LEDs

A slide switch is used for power ON/OFF.

A green LED indicates power-up and a red LED indicates that something is wrong on the power rails. Green LEDs are populated next to the individual DC/DC converters being used to generate the 5V, 3.3V, 1.8V, 1.1V and 0.9V power rails.

4.2.2 Power Jack

The 12V DC input draws about 2A, excluding any additional use from the Expansion header.

4.2.3 PCIe 2.0 – OCuLink Connector

The LAN9692 implements a single-lane PCIe® Gen2 end-point controller, that can be connected to any PCIe-capable system. The PCIe interface can be used by an external CPU to read and write the Switch registers.

The reference board offers PCIe® Gen 2.0 connection over a standard OCuLink Internal end-point when configured as a PCIe end-point.

4.2.4 SMA Connectors Used for 1PPS Input and Output

There are two SMA connectors intended for 1PPS input and output.

Both signals are connected to separate PTP engines within the Switch.

The SMA input is LVTTL and 3V3 tolerant – it is not 5V tolerant.

The SMA output also provides LVTTL level.

4.2.5 Management Port and Status LED

The Management port with LAN8840 supports normal tri-speed links (10M/100M/1000M) through its RJ45 ICM connector.

The connector has two LEDs (green/yellow). These port status LEDs are automatically controlled by the CuPHY. The left LED signals 1G link/traffic (green solid/blinks) and right LED signals 10M/100M link/traffic (yellow solid/blinks).

4.2.6 USB 2.0 Type-C Serial Port

The USB-C port uses an on-board serial-to-USB converter MCP2200. The USB driver software (Windows, Mac, Linux) is found at <https://www.microchip.com/en-us/product/MCP2200>.

The USB converter has 8 GPIOs, which can control board Reset and VCORE boot mode. Two GPIOs are controlling two LEDs for Tx and Rx data traffic indication.

4.2.7 Reset Button

A **Reset** button is available on the reference board. When pressed, it drives the input of a voltage supervisor low, and hereby creating a hard Reset to the board.

The green USB Rx LED will light up for board Reset indication.

If the **Reset** button is held, Reset is released on the voltage supervisor, but the state of the **Reset** button can then be read by software, once it is running again, to determine long press and hereby setting the board back to default setup. There is currently no support for this in the Switch Application.

4.2.8 Board Status and Reset LEDs

A double-LED (green/yellow) is available to show the current board status. The green LED is controlled by the Switch application, and the yellow LED is (shortly) turned ON during board Reset.

4.3 ADDITIONAL ON-BOARD CONNECTORS

4.3.1 Expansion Header

The Expansion header can give an external CPU control over the SPI client register access interface, or it can be used for programming the on-board NOR Flash device as the header implements a simple level conversion by using resistor dividing to support NOR Flash programming using a standard 3.3V Flash Programmer.

The Expansion header is partially compatible with Raspberry Pi. GNSS modules (designed for RPI) can be mounted to provide GNSS time input to the system using UART and 1PPS signals.

The Expansion header exposes various LAN9692 GPIO signals in Alternate mode as shown in [Table 4-1](#).

TABLE 4-1: GPIO SIGNALS IN ALTERNATE MODE

Signal	Alternate Mode
SI	SPI.SCK, SPI.D1, SPI.D0, and SPI.nCS
I ² C	SCL, SDA (Host mode, FLEXCOM 3)
UART	RXD, TXD – RS-232 (Host mode, FLEXCOM 0)
PTP	1PPS_IN (PTP.SYNC2)
VCORE_[3:0]	Boot mode selection. SW1 must be set to '0000'.
Reset	Board Reset. Note that NOR Flash has no Reset.

From VCORE_[3:0], the on-board boot mode strapping can also be overruled when DIP switch is set to '0000'.

4.3.2 ARM CPU JTAG Connector

The board has a standard JTAG/Debug 10-pin (0.05") header, which can be used for boundary scan and ICE. System default is selecting ICE mode through resistor strapping.

4.3.3 QSPI Flash Program Header, 1.8V

The NOR Flash can in a production environment be programmed on-board using an external 1.8V Programmer through a QSPI Flash Program header. See [Section 5.2.5 “QSPI Flash Programming”](#).

4.3.4 On-die Temperature Sensor Header

Footprint for a 2-pin header makes it possible to do measurements on the anode and cathode signals of the on-die thermal diode, if required.

The LAN9692 includes another internal thermal diode for measuring the junction temperature and an embedded A/D converter for monitoring it through the register interface.

4.4 BOOT MODE AND REFERENCE CLOCK

LAN9692 boot mode is strapped through its VCORE[3:0] pins by using an on-board 4-pin DIP switch. System default is to boot from the on-board NOR Flash device.

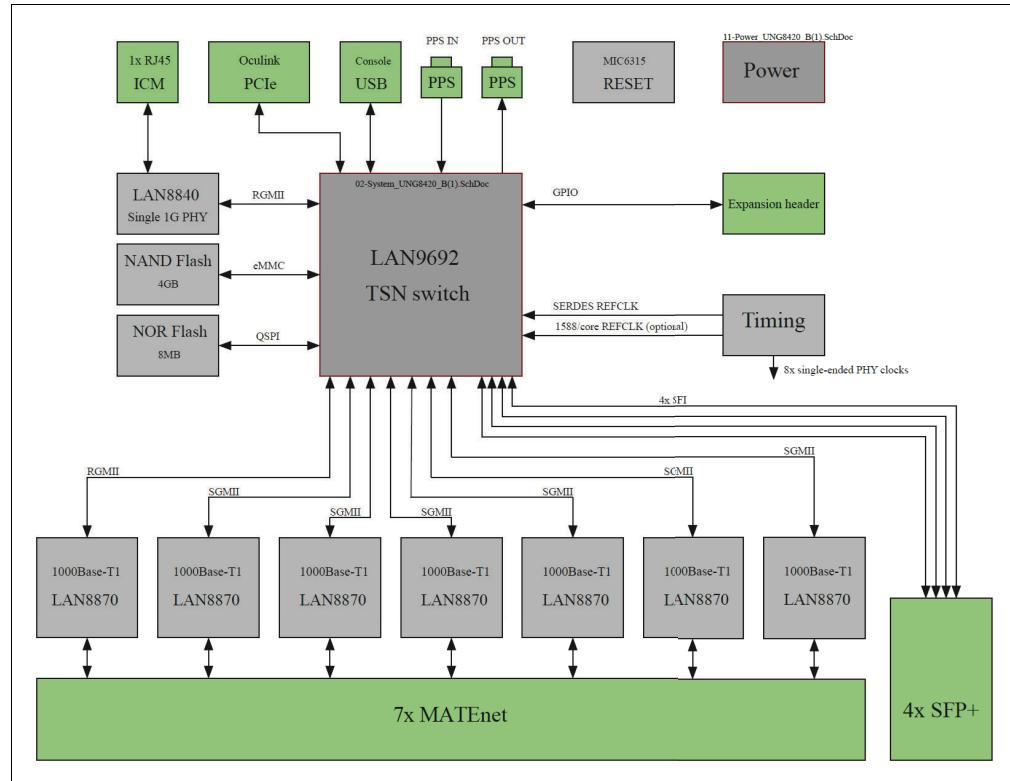
Additionally, it is possible to select the source of the core reference clock through REF_CLK_SEL. This signal can also be controlled from a GPIO located on the UART-to-USB converter. Default is selecting the differential 156.25MHz clock input.

Chapter 5. Detailed Hardware Description

5.1 BLOCK DIAGRAM

Figure 5-1 depicts the block diagram of the EVB-LAN9692-LM Reference board with its 7x T1 (100M/1G) copper ports and 4x SFP+ (10G) slots placed on the front.

FIGURE 5-1: EVB-LAN9692-LM BLOCK DIAGRAM



The design is based on LAN9692 TSN Switch, which includes an ARM CPU running on its internal 2MB SRAM and bootable Flash devices; QSPI NOR and eMMC NAND.

The CPU subsystem runs a machine protocol for external management through the Management Cu port located on the back of the board. The Management port uses a LAN8840 tri-speed CuPHY.

Optionally, LAN9692 can be managed from an external CPU system connected through a PCIe/OCuLink connector, J21 or through the SPI client interface found in the Expansion header, J4.

Board bringup and software debugging are performed through a dedicated UART port, J30. A UART-to-USB serial converter, MCP2200, is used to provide terminal access.

A local 156.25MHz OSC feeds the LAN9692 SerDes macro's reference clock input. Per default, this reference clock also serves the Switch core and CPU subsystem.

A local 25MHz OSC clock is distributed to all 8x CuPHYs using a ZL40241 Clock buffer. Optionally, this clock can be used by the Switch core and CPU subsystem.

There are two SMA connectors to support IEEE 1588 1PPS IN, J13 and OUT, J14. Likewise, for PHY time-stamp adjustment a 1PPS signal is distributed to all CuPHYs by using another ZL40241 Clock buffer.

5.2 VCORE-IV CPU SUBSYSTEM

The LAN9692 includes an internal CPU subsystem called VCORE-IV. This subsystem has an embedded ARM Cortex-A53 single core 64-bit processor operating at 1GHz and various peripheral host controllers for SD/eMMC, MIIM, ULPI, UART and QSPI.

5.2.1 VCORE Configuration Strapping

LAN9692 has four dedicated strapping pins for selection of the initial boot mode. These are named VCORE[3:0]. On the reference board boot mode strapping is made through a DIP switch, SW1. Default boot mode when using the Lightly Managed Application is booting from NOR Flash '0001' or '0100'.

[Table 5-1](#) shows the possible boot modes that the reference board offers.

TABLE 5-1: BOOT MODE STRAPPING

VCORE[3:0]	Mode	Description
0000	eMMC	Boot from eMMC Flash. Boot trace on Flexcom0 (115200/8/N).
0001	QSPI0	Boot from NOR Flash. Boot trace on Flexcom0 (115200/8/N).
0011	eMMC	Boot from eMMC Flash.
0100	QSPI0	Boot from NOR Flash.
1000	QSPI0	Boot from NOR Flash. Boot trace on Flexcom0 (921600/8/N).
1010	TF-A	TF-A monitor on Flexcom0 (115200baud/8/N).
1011	TF-A	TF-A monitor on Flexcom0 HS (921600baud/8/N).
1111	SPI client	QSPI0 is configured as SPI client. Internal CPU is disabled.

To let the ARM CPU boot from the eMMC interfaced NAND Flash device, the strapping must be set to '0000' or '0011'.

Traces on the Flexcom0 UART interface is connected to the on-board serial-to-USB converter and is exposed on the USB-C connector, J30.

When the SPI client is selected, an external CPU can access the Switch register interface to set up and control the Switch device.

5.2.2 Clock Source Configuration Strapping

The SerDes required 156.25MHz differential clock is per default used as base frequency for the VCORE-IV subsystem. It is however possible by resistor strapping through the REFCLK_SEL pin strap, or from software to change configuration to use the 25MHz reference clock in IEEE 1588 applications to separate the SerDes Sync-E and the PTP engines timing domains. Since the reference board does not offer any external DLL device to clean up recovered clock signals, there is no support for SyncE.

5.2.3 eMMC NAND Flash

The VCORE-IV subsystem can boot directly from an eMMC interfaced NAND Flash.

The reference board is equipped with 4GB eMMC NAND. Larger devices can be used, presently up to 64GB. The NAND IO supply, VDDQ is supplied with 1.8V to match LAN9692 IO. The primary use for the on-board eMMC device has been for SW development and production test usage. There is no requirement to have the eMMC populated in a VelocityDRIVE solution.

5.2.4 QSPI NOR Flash

The reference board is equipped with 8 MB NOR QSPI boot Flash, SST26WF064C (SOIJ-8). This Flash device can operate both in normal SPI and in QSPI IO mode.

The NOR IO supply, VDD is supplied with 1.8V to match to the dedicated QSPI interface on LAN9692.

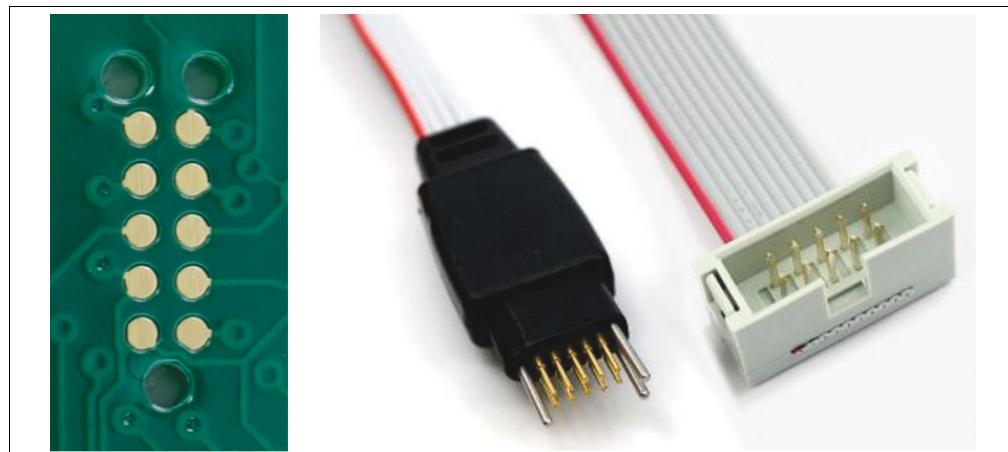
5.2.5 QSPI Flash Programming

During production the NOR Flash device can be programmed using an external Programmer either through a 2x5 pin footprint header, J1 or through the Expansion header, J4 described in [Section 5.6 “Expansion Header”](#).

Both headers include a Reset signal, through which the Programmer can keep the VCore-IV subsystem in Reset, and hereby releasing control of the SI Data output. This will allow the Programmer to drive the signal, while programming the NOR Flash device.

Figure 5-2 shows the footprint header on the PCB and its associated probe.

FIGURE 5-2: TC2050-NL-FP FOOTPRINT AND ASSOCIATED PROBE



The probe used is TC2050-IDC-NL from Tag-Connect.

[Table 5-2](#) describes the location of the different signals in the 2x5 pin header, J1.

TABLE 5-2: QSPI NOR FLASH PROGRAMMING FOOTPRINT HEADER

Pin	Direction	Signal
1	In	QSPI.CK – SPI clock to SPI Flash
2	—	GND
3	BiDir	QSPI.D1 – SPI data to/from SPI Flash
4	In	1.8V Reset signal to Switch
5	BiDir	QSPI.D2 – SPI data to/from SPI Flash
6	Out	1.8V from board
7	In	QSPI.nCS – SPI chip select to SPI Flash
8	BiDir	QSPI.D3 – SPI data to/from SPI Flash
9	BiDir	QSPI.D0 – SPI data to/from SPI Flash
10	—	GND

5.2.6 ARM CPU JTAG Header

A standard ARM 10-pin header is used for boundary scan and ICE. [Table 5-3](#) describes the 10-pin header.

TABLE 5-3: ARM JTAG HEADER (10-PIN, PITCH 0.05")

Pin	Direction	Signal	Description
1	Out	1V8 supply	Local 1.8V supply and signal level
2	In/BiDir	TMS	JTAG Test Mode Select Input (See Note 1)
3	—	GND	Ground
4	In	TCK	Test Clock Input
5	—	GND	Ground
6	Out	TDO	JTAG Test Data Output
7	—	KEY	—
8	In	TDI	JTAG Test Data Input
9	—	nDETECT	Not used. 10 kΩ pull-up resistor
10	In	nRSTD	JTAG_CPU_nRST – can be modified to be general Switch Reset, nRESET

Note 1: Bidir in SingleWire Debug mode.

LAN9692 provides a JTAG_SEL input signal used for selecting JTAG mode of operation. [Table 5-4](#) shows which tap controller can be selected. Default mode is CPU Tap controller.

TABLE 5-4: JTAG MODE OF OPERATION

JTAG_SEL	Mode
Low	Test Tap controller
High	CPU Tap controller

5.2.7 FLEXCOM Usage

The VCore-IV CPU subsystem has four multi-purpose COM modules called FLEXCOM. The FLEXCOM[3:0] IOs are available as alternate functions on the GPIO pins.

5.2.7.1 FLEXCOM0 UART FOR TF-A MONITOR AND TRACE OUTPUT

The FLEXCOM0 UART is used as console port and is connected to an USB-to-UART serial converter, MCP2200.

The MCP2200 has 256-bytes user EEPROM and eight general purpose input/output pins. Four of the pins have alternate functions to indicate USB and communication status. The reference board uses the MCP2200 Tx/Rx functionality to indicate UART traffic through two green LEDs.

The MCP2200 must initially be programmed to set the on-chip signals GP[5:0] mode as input. Otherwise, factory default settings will keep holding the reference board in Reset.

[Table 5-5](#) describes the MCP2200 GPIO usage.

TABLE 5-5: MCP2200 GPIO USAGE

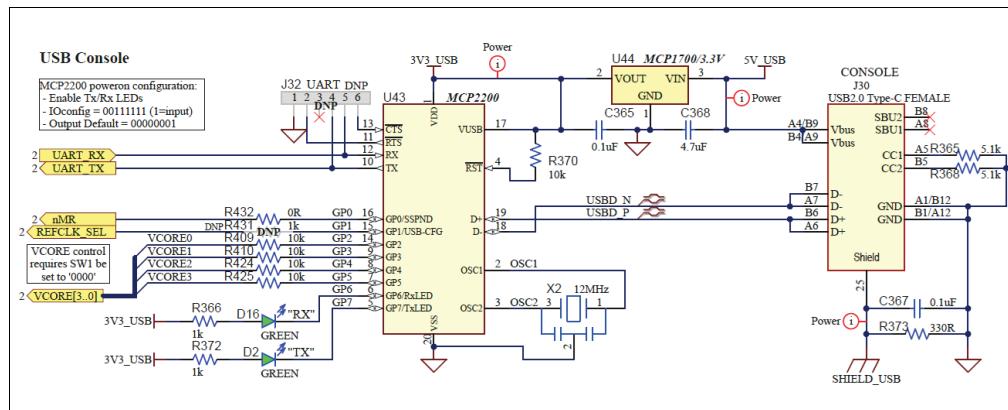
GP	Direction	Signal
0	In	nMR. Board Reset (Default set to high)
1	In	REFCLK_SEL. Core clock select, 0: 25 MHz, 1: 156.25 MHz.
2	In	VCORE0 (See Note 1)
3	In	VCORE1
4	In	VCORE2
5	In	VCORE3
6	Out	RxLED functionality
7	Out	TxLED functionality

Note 1: SW1 must be set to '0000'.

- 2: The MCP2200 must initially be programmed to set the on-chip signals GP[5:0] mode as input. Otherwise, the factory default settings will keep holding the reference board in Reset.

[Figure 5-3](#) shows the USB-to-UART Serial Conversion.

FIGURE 5-3: UART-TO-USB SERIAL CONVERSION



The USB converter is locally powered through its USB Type-C connector using a low dropout (LDO) voltage regulator, MCP1700. It awakes smoothly, when connected to a Host USB.

5.2.7.2 FLEXCOM1 I²C INTERFACE

FLEXCOM1 TWIHS is being used to offer a general I²C interface for various usage like the SFP slots and to support devices connected on the Expansion header, J4. Before use, the two I²C signals, SCL and SDA, are voltage level converted to 3.3V by using a PCA9306.

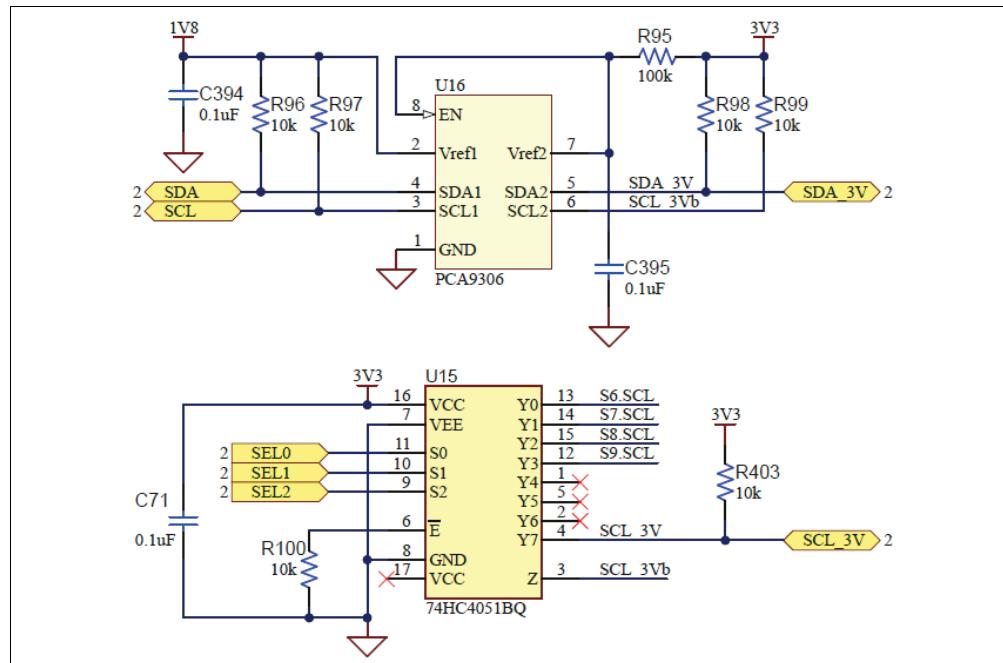
SFP modules include an I²C EEPROM used for identification. However, all SFPs reside on the same I²C address, 1010_000, thus a multi-SFP system needs an I²C segment per SFP in order to avoid I²C address conflicts.

The LAN9692 has a built-in I²C multiplexer targeting this issue by offering ten gated clock signals. These separate TWI_GATE_SCL[9:0] lines are available on the Switch GPIO pins in alternate mode. However, the overall GPIO usage is constrained, as RGMII0 uses the same GPIO pins. Therefore, the reference design implements the use of an external 8-channel analog multiplexer, 74HC4051BQ.

The three select pins, SEL[2:0], are controlled through the Switch GPIOs and is on-board level converted to 3.3V.

The four S[9:6] SCL signals are routed to the SFP+ slots on the front. The remaining clock signal, SCL_3V, is routed to the Expansion header, J4. See [Figure 5-4](#).

FIGURE 5-4: TWI LEVEL CONVERSION AND MUXING



5.2.8 Serial GPIO Controller

The LAN9692 incorporates a Serial GPIO controller. It is documented in the application note, *Serial GPIO User's Guide*.

Through four pins, a Serial GPIO engine can interface to 74-series shift registers on the board to provide a flexible GPIO mechanism. The four Serial GPIO pins are located on the Switch GPIO in alternate mode and named SG0_CLK, SG0_DO, SG0_DI, and SG0_LD. These signals are locally converted between 1.8V and 3.3V.

Instead of using discrete shift registers, the external circuitry can be implemented in e.g., a central PLD. However, the parallel inputs and outputs would then need to be routed across the board between the PLD and individual endpoints. By using shift registers, only the four LAN9692 Serial GPIO signals need to be routed over long distances as each shift register can be distributed across the board as applicable.

Detailed Hardware Description

In the reference design, the Serial GPIO controller is configured to use four bits per port and running 5 MHz. Its main task is to handle the out-of-band control signals towards the SFP slots. [Table 5-6](#) shows the Serial GPIO port usage.

TABLE 5-6: SERIAL GPIO CONTROLLER PORT USAGE

SG Port	Description
0-5	Disabled
6-9	SFP out-of-band control and port LEDs
10-29	Disabled

The SFP MSA defined signals, Tx Fault, Module Detect, and Rx Loss-of-Signal (LOS), are inputs and read through 74HC165 shift registers. Each of these signals has a 10k pull-up, as required per SFP MSA.

The SFP Rx LOS signals are each assigned to p[n]b[0] Serial GPIO input, which allows for a default connection within LAN9692 to the port PCS layer as Signal Detect input.

Likewise, the output signals, Tx Disable, Rate Select, LED1 (green), and LED2 (yellow), are individually controlled through another set of shift registers using 74HC594.

As the shift register outputs are set low by the board Reset, additional inverters may be required to set TX Disable high (active) during Reset. This can be done using inverting buffers, 74HC240. Likewise, the need for using pull-up resistors can be avoided.

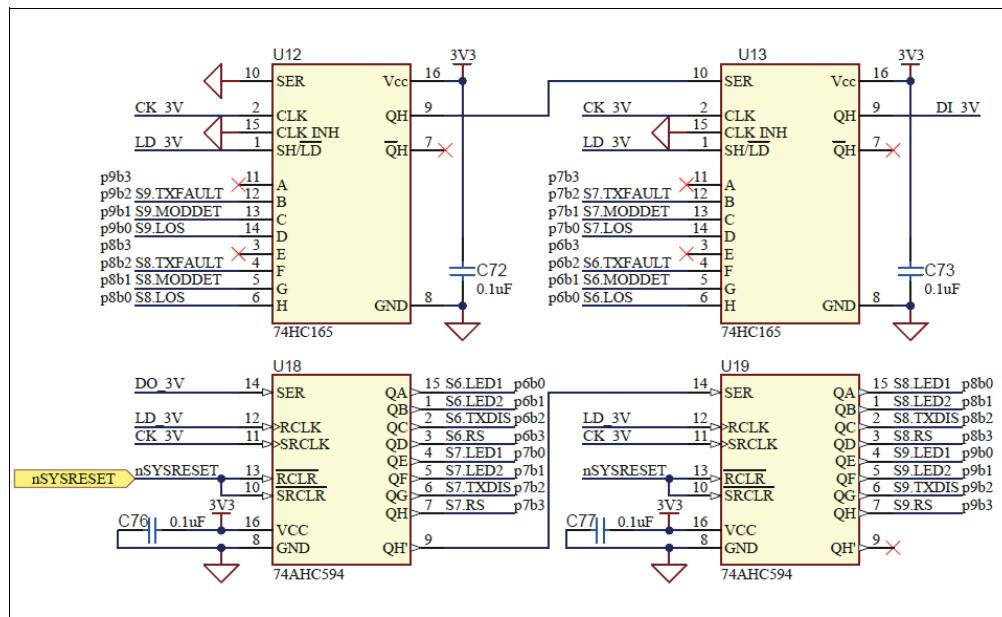
[Table 5-7](#) describes where the additional GPIO signals are located in the Serial GPIO controller.

TABLE 5-7: SERIAL GPIO CONTROLLER PIN DESCRIPTION

Port/Bit	Input	Output
p6b0	S6.LOS (1=LOS from SFP)	S6.LED1 – Green
p6b1	S6.MODDET (0=SFP present)	S6.LED2 – Red
p6b2	S6.TXFAULT (1=TX fault on SFP)	S6.TXDIS
P6b3	—	S6.RATESEL (RS1 and RS2)
p7b0	S7.LOS (1=LOS from SFP)	S7.LED1 – Green
p7b1	S7.MODDET (0=SFP present)	S7.LED2 – Red
p7b2	S7.TXFAULT (1=TX fault on SFP)	S7.TXDIS
p7b3	—	S7.RATESEL (RS1 and RS2)
p8b0	S8.LOS (1=LOS from SFP)	S8.LED1 – Green
p8b1	S8.MODDET (0=SFP present)	S8.LED2 – Red
p8b2	S8.TXFAULT (1=TX fault on SFP)	S8.TXDIS
p8b3	—	S8.RATESEL (RS1 and RS2)
p9b0	S9.LOS (1=LOS from SFP)	S9.LED1 – Green
p9b1	S9.MODDET (0=SFP present)	S9.LED2 – Red
p9b2	S9.TXFAULT (1=TX fault on SFP)	S9.TXDIS
p9b3	—	S9.RATESEL (RS1 and RS2)

Figure 5-5 shows the reference board Serial GPIO implementation using shift registers.

FIGURE 5-5: SERIAL GPIO SHIFT REGISTERS



5.2.9 MII-Management Controllers

The VCore-IV CPU subsystem has 2 MII-Management bus interfaces. Both are available on the Switch GPIO pins in Alternate mode.

MIIM0 is daisy-chained to 4x LAN8870 PHYs, T1_1 to T1_4 with MII-Management addresses 16 to 19, respectively.

MIIM1 is daisy-chained to 3x LAN8870 PHYs, T1_5, T1_6 and T1_0, and the Management port LAN8840. The MII-Management addresses are 16 to 18, and 3.

The reason for using both MII-Management bus interfaces is to allow the CPU to access two PHYs at the same time, improving setup speed or PHY status polling for link changes. While waiting for a reply to a PHY read on one bus, it is possible to setup a new PHY read/write command to another PHY on the other bus. This functionality is currently not implemented in the Switch Application.

Both MII-Management buses are terminated at the end using pull-up resistor on MDIO and MDC. The drive strength for MDC is set to 3.

5.2.9.1 PHY SHARED INTERRUPTS PINS ON GPIO

The LAN9692 Interrupt Controller has six dedicated Interrupt pins (operating as either input or output)—all located on the Switch GPIO pins in alternate mode. Two pins are meant for MIIM usage, MIIM0_IRQ/IRQ2 and MIIM1_IRQ/IRQ5.

Note: There is no physical binding between the two MII-Management controllers and the Interrupt controller. The GPIO placement of the two IRQ signals close to the MIIM MDC/MDIO buses is purely to ease customer routing, when using these buses.

When an interrupt occurs on a shared interrupt source, the Switch Application polls the possible sources for their current interrupt status through the MII-Management interface as it is otherwise not possible to distinguish which source port has activated the shared interrupt signal.

The PHY shared interrupt signals, MIIM0_IRQ and MIIM1_IRQ, each have a 10k pull-up resistor.

5.2.10 LAN9692 GPIO Usage

The previous sections have described the reference board usage of the alternate GPIO features. [Table 5-8](#) summarizes the usage of all 67 GPIO pins in LAN9692. All GPIOs have an internal pull-up resistor as their default setting.

TABLE 5-8: GPIO USAGE

GPIO	Mode	Signal	Description
0	ALT3	PCIe.PERST	PCIe Reset input
1	GPIO	PHY_nRESET	PHY Reset output
2	GPIO	nBUTTON	Push button input. Long press detection
3	ALT1	FC0.RXD	FLEXCOM0 UART for TF-A and CLI
4	ALT1	FC0.TXD	
5	ALT1	SGPIO.CK	Serial GPIO controller 0
6	ALT1	SGPIO.LD	
7	ALT1	SGPIO.DO	
8	ALT1	SGPIO.DI	
9	ALT1	MIIM0_MDC	MII-Management controller 0 IRQ2 used
10	ALT1	MIIM0_MDIO	
11	ALT1	MIIM0_IRQ	
12	GPIO	nBRDRESET	Board Reset
13	GPIO	STATUS	Board Status LED
14	ALT1	eMMC.CMD	SD/eMMC Host controller 0
15	ALT1	eMMC.CLK	
16	ALT1	eMMC.D0	
17	ALT1	eMMC.D1	
18	ALT1	eMMC.D2	
19	ALT1	eMMC.D3	
20	ALT1	eMMC.D4	
21	ALT1	eMMC.D5	
22	ALT1	eMMC.D6	
23	ALT1	eMMC.D7	
24	ALT1	eMMC.RSTn	
25	GPIO	SEL0	I ² C clock selection
26	GPIO	SEL1	
27	GPIO	SEL2	
28	ALT2	FC1.RXD	FLEXCOM1 I ² C for PHYs
29	ALT2	FC1.TXD	
30	ALT1	ULPI.CLK	1PPS output to PHYs
31	ALT1	ULPI.D0	1PPS output from PTP OUT SMA
32	ALT1	ULPI.D1	1PPS input from PTP IN SMA, Expansion hdr
33	GPIO	Spare	TP4
34	GPIO	Spare	TP5
35	GPIO	Spare	TP6
36	GPIO	Spare	TP7
37	GPIO	Spare	TP8
38	GPIO	Spare	TP9

TABLE 5-8: GPIO USAGE (CONTINUED)

GPIO	Mode	Signal	Description
39	ALT3	MIIM0_MDC	MII-Management controller 1 IRQ5 used
40	ALT3	MIIM0_MDIO	
41	ALT3	MIIM0_IRQ	
42	RGMII1	RX_D0	RMII/RGMII 1 interface
43	RGMII1	RX_D1	
44	RGMII1	RX_D2	
45	RGMII1	RX_D3	
46	RGMII1	RX_CLK	
47	RGMII1	RX_CTL	
48	RGMII1	TX_D0	
49	RGMII1	TX_D1	
50	RGMII1	TX_D2	
51	RGMII1	TX_D3	
52	RGMII1	TX_CLK	
53	RGMII1	TX_CTL	
54	RGMII0	RX_D0	RMII/RGMII 0 interface
55	RGMII0	RX_D1	
56	RGMII0	RX_D2	
57	RGMII0	RX_D3	
58	RGMII0	TX_CLK	
59	RGMII0	TX_CTL	
60	RGMII0	RX_D0	
61	RGMII0	RX_D1	
62	RGMII0	TX_D2/BRD_ID	
63	RGMII0	TX_D3	
64	RGMII0	TX_CLK	
65	RGMII0	TX_CTL	
66	GPIO	GPIO	TP10

5.3 SWITCH CORE

5.3.1 Network Ports

The EVB-LAN9692-LM reference board exposes one Base-T Cu-port on the back for Management, and seven Base-T1 Cu-ports and four SFP+ ports on the front.

The Management port uses a single port CuPHY, LAN8840 connected to LAN9692 RGMII_1 interface. The front Cu-ports uses the single port, LAN8870, whereas the first is connected to RGMII_0 and the others are connected to the first six SerDes interfaces using SGMII. All PHY SerDes signals are AC coupled to ensure Common-mode voltage compatibility. See [Table 5-9](#).

Each PHY is controlled over a MII-Management bus by using individual MIIM addresses. The configuration of the PHYs is handled by the Switch Application.

Details of the two MII-management interfaces used are described in [Section 5.2.9 “MII-Management Controllers”](#). Likewise, the description of the interrupt signals from each CuPHY connected to the Switch Interrupt inputs, such as IRQ2 or IRQ5, can be found here.

TABLE 5-9: EVB-LAN9692-LM PORT MAPPING

Port	Interface	Type	Internal Port	Management	PHY
Management	R1	RGMII	D29	MIIM1 address 3	LAN8840
T1_0	R0	RGMII	D28	MIIM1 address 18	LAN8870
T1_1	S0	SGMII	D0	MIIM0 address 16	LAN8870
T1_2	S1	SGMII	D4	MIIM0 address 17	LAN8870
T1_3	S2	SGMII	D8	MIIM0 address 18	LAN8870
T1_4	S3	SGMII	D12	MIIM0 address 19	LAN8870
T1_5	S4	SGMII	D16	MIIM1 address 16	LAN8870
T1_6	S5	SGMII	D20	MIIM1 address 17	LAN8870
SFP1	S6	SFI	D24	S6.SCL, SEL 0	SFP slot
SFP2	S7	SFI	D25	S7.SCL, SEL 1	SFP slot
SFP3	S8	SFI	D26	S8.SCL, SEL 2	SFP slot
SFP4	S9	SFI	D27	S9.SCL, SEL 3	SFP slot

5.3.2 LAN8840 Copper PHY

5.3.2.1 MEDIA SIDE INTERFACE

The LAN8840 integrate all passive components required to connect the PHYs media interface to an external 1:1 transformer and Common-mode choke, CMC. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The LAN8840 support the IEEE standard range of 1m to 100m twisted pair cable. However:

- 1000Base-T mode requires Category 5 enhanced cable in accordance with the cabling specifications defined by IEEE802.3-2005.
- 100BASE-TX mode requires Category 5 cable and 10BASE-T requires Category 3 cable as specified in ISO/IEC 11801.

5.3.2.2 INTEGRATED MAGNETICS – ICM

Instead of separate magnetic and RJ45 connector, the reference board uses RJ45 connectors with integrated magnetics. This reduces the number of components on the board and the actual board area.

The Management port uses BEL L829-1J1T-43 ICM, which has the CMC placed on the PHY side. Other pin-compatible parts may exist.

Generally, using good magnetics has a huge influence on EMI performance.

5.3.2.3 PORT LEDS

The Management port has 2 LEDs, located in the RJ45 connector. One is green, and one is yellow LED. These are driven from the CuPHYs.

5.3.2.4 PHY GPIO USAGE

Table 5-10 shows the LAN8840 CuPHY GPIO mapping and strapping.

TABLE 5-10: LAN8840 GPIO USAGE AND PIN STRAPPING

GPIO	Signal	Description
0	LED1	LED1/ PHYAD0 /LEDPOL1. ‘1’: PHYAD = 3.
1	LED2	LED2/ PHYAD1 /LEDPOL2. ‘1’: PHYAD = 3.
2	PHYAD2	LED3/ PHYAD2 /LEDPOL3. ‘0’: PHYAD = 3.
3	ICMCT	LED4/ PHYAD3 /LEDPOL4. ‘0’: ICM with separate center taps.
4	ALLPHYAD	LED5/ ALLPHY /1PPS. ‘1’: Do not respond to MIIM address 0. 1PPS input from LAN9692.
5	MDINTn	LED6/INT_N. PHY interrupt output.
6	LEDMODE	CLK125_NDO/ LEDMODE . ‘1’: Individual.
—	MODE[4:0]	‘11001’: ANEG enabled, 10/100M FDX/HDX and 1000M FDX.
—	CLK125EN	CLK125EN . ‘0’: Disabled.

Note 1: Strap settings are shown in **bold**.

5.3.3 LAN8870 Copper PHY

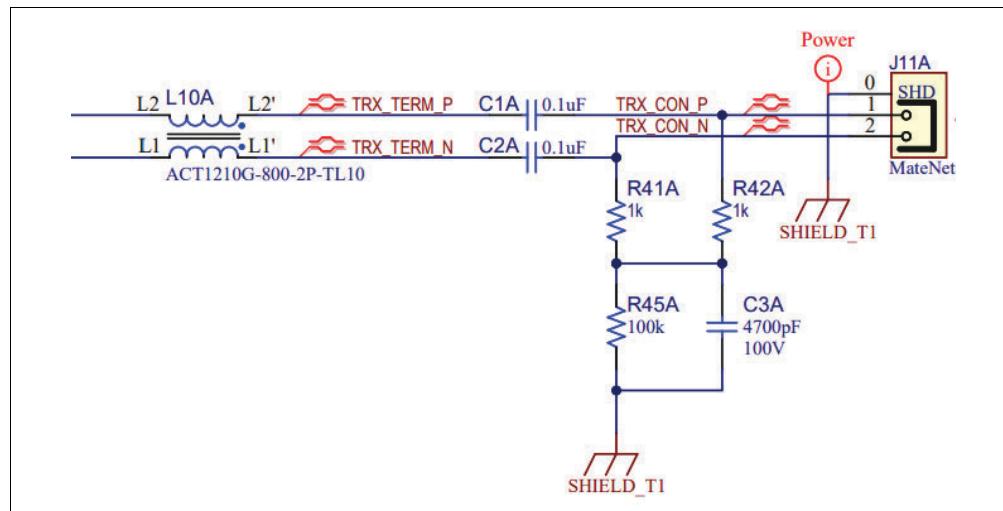
5.3.3.1 MEDIA SIDE INTERFACE - EMC-ESD NETWORK

The Automotive Ethernet standards utilize unshielded single twisted pair cables (UTP) to interconnect between PHYs. UTP cables are smaller, lighter and easier to handle, which are all critical requirements for automotive OEMs. However, the use of these more cost-effective cables introduces additional challenges in protecting against electromagnetic interference, EMI.

Likewise, ESD protection should be positioned at the connection point to ensure that ESD pulses are clamped directly to ground, providing maximum protection for all network circuits, including the PHY and its Common-mode choke.

The following used EMC-ESD Network is defined in the OPEN Alliance and IEEE 1000Base-T1 System Implementation specification to help with EMC and ESD-related issues. The network, consists of a Common-Mode Choke (CMC), three resistors and three capacitors.

FIGURE 5-6: EMC-ESD NETWORK RECOMMENDED EXAMPLE BY OPEN ALLIANCE



Detailed Hardware Description

The CMC is necessary to eliminate Common-mode signals between the lines. This improves EMC performance by suppressing these signals from transmitting to the link partner. Furthermore, the CMC attenuates the stress on the PHY caused by ESD pulses. That is, when a transient strikes the common-mode choke, it temporarily blocks the current.

The 0.1 μ F capacitors placed in-line between the CMC and the termination network is to AC couple the Ethernet signaling with Link Partner.

The 1 k Ω resistor are meant to provide a balanced termination to the incoming and outgoing signals between the lines. The resistors are capable of handling power of at least 0.625 Watt, as they are to dissipate up to 50 VDC on the line to ground.

The 4.7 nF capacitor is designed to provide a balanced termination at the 100BASE-T1/1000BASE-T1 signal operating frequency with respect to ground.

The 100 k Ω resistor is designed to prevent ESD transient voltage signals resulting from a cable harness connection. At DC, the 100 k Ω resistor greatly dissipates most of the transient signal.

5.3.3.2 TC10 - LOW-POWER REMOTE SLEEP AND WAKE-UP SUPPORT

The LAN8870 supports the OPEN Alliance TC10 sleep/wake-up functionality, when configured in Managed mode. It offers a low-power sleep mode with local wake-up support.

The EVB-LAN9692-LM reference board implements a simple control for testing the TC10 functionality on the first T1 PHY, T1_0 only.

TC10 test setup:

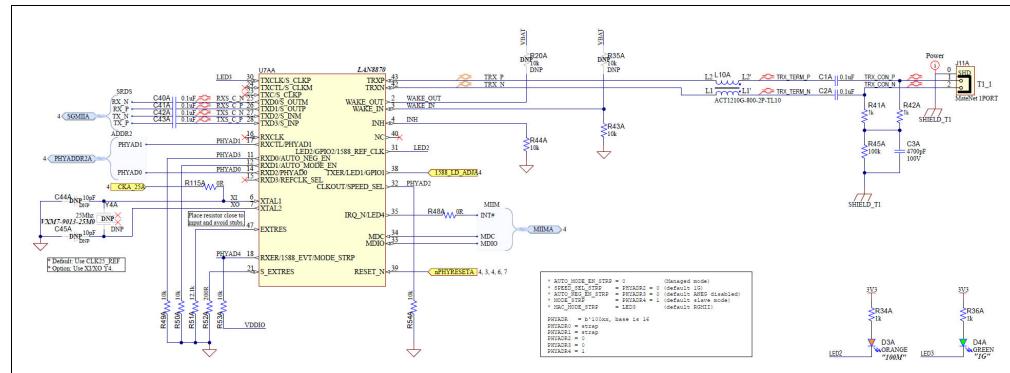
On WAKE_IN pin, change default pull-down resistor, R142 to become pull-up resistor to VBAT, R139 and mount pin header J16 for external input control.

The LAN8870 monitors the WAKE_IN pin for valid pulses. Pulses <10 μ s are ignored, while pulses >40 μ s are recognized, and when asserted the part is moved out of Sleep state.

MDI Wakeup. The LAN8870 may be awakened via activity on the MDI interface by monitoring for the WUP (Wake-up Packet) defined in the TC10 specification.

Optionally, add R112 resistor and J15 pin header to implement WAKE_OUT. The signal is asserted, when the part moves out of Sleep state.

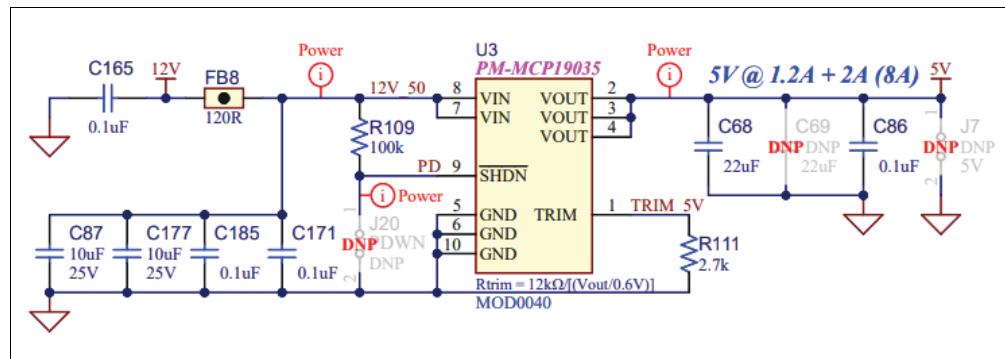
FIGURE 5-7: TC10 SLEEP AND WAKE-UP PINS



Mount pin headers J17 and J20 and interconnect INH with PD (power down input) on the main board supplies. This will effectively power down the board, while in Sleep state.

The INH indicates LAN8870 Active/Low-power status. It is driven high in Active state and pulled low in Low-power (pin is high-Z during TC10 Sleep) state. Inhibit means inhibit shutdown of the external power supply.

FIGURE 5-8: MAIN BOARD SUPPLY PD PIN

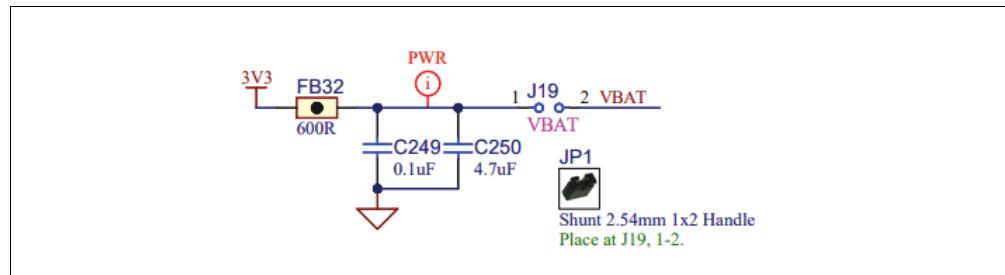


Note: This pin operates on the VBAT domain. The VBAT supply must always be powered to keep the LAN8870 operational in TC10 Sleep state.

The VBAT supply is also used for the wakeup detection circuitry. The LAN8870 VBAT module detects activity on the WAKE_IN pin and/or the MDI interface to determine wakeup signaling and hereby asserting the INH pin to reactivate the main board supplies within 1 ms.

Remove jumper JP1 and prepare/add external 3.3V battery source on pin header J19.2.

FIGURE 5-9: ATTACHING A 3.3V BATTERY POWER SOURCE ON J19.2



Last, control WAKE_IN from pin header J15.2 to change TC10 state.

Note, the Wakeup Common Control 0 Register has fields for controlling:

- the INH pin operational modes defined by the inh_mode bit,
- the WAKE_IN polarity by the wkinpol bit,
- the WAKE_OUT polarity by the wkoutpol bit,
- and last mode of operation determined by the wkoutmode field, allowing for open-source, open-drain, and push-pull operation.

5.3.3.3 PORT LEDS

The T1 ports have 2 LEDs, located above each MATEnet connector. One Green LED indicating 1G and one Orange LED indicating 100M. Both are driven by the T1 PHY.

Detailed Hardware Description

5.3.3.4 PHY GPIO MAPPING AND STRAPPING

Table 5-11 shows the LAN8840 CuPHY GPIO mapping and strapping.

TABLE 5-11: LAN8840 GPIO USAGE AND PIN STRAPPING

GPIO	Signal	Description
1	1588_LD_ADJ	LED1/1588_CLK_LD_ADJ. 1PPS from LAN9692.
2	LED2	LED2/1588_REF_CLK. Orange LED for 100M link/activity.
3	LED3	LED3/MAC_MODE_STRP. Green LED for 1G link/activity. A pull-up resistor sets LAN8870 to SGMII mode.
4	INT_N	LED4/IRQ_N. PHY interrupt output.
—	PHYAD[1:0]	PHYADR[1:0] . Strap.
—	PHYAD2	PHYADR2/SPEED_SEL_STRP . ‘0’. Managed mode.
—	PHYAD3	PHYADR3/AUTO_NEG_EN_STRAP . ‘0’. Managed mode.
—	PHYAD4	PHYADR4/MODE_STRP :‘1’. Managed mode.
—	—	AUTO_MODE_EN_STRP . ‘0’: Managed mode.

Note 1: Strap settings are shown in **bold**.

The strapping, AUTO_MODE_EN_STRP = 0 sets the PHY in Managed mode. In Managed mode, the other strap pins (MODE_STRP, AUTO_NEG_EN_STRP, SPEED_SEL_STRP) becomes PHYAD[4:2].

Default setup in Managed mode is then ANEG disabled, 1G FDX forced speed and Slave clock mode.

The MAC_MODE_STRP is located on VDD_RGMII_VPH. A 1.8V enables RGMII, while 2.5V/3.3V selects SGMII.

Note: During the design phase it was not fully clear, if powering VDD_RGMII_VPH with 3.3V was allowed/worked properly. Therefore, the T1 PHYs running SGMII has each a local 2.5V LDO, which can be substituted with a ferrite bead to 3.3V.

5.3.4 SFP+, SFI Interfaces

SFP signals are AC coupled in the SFP module and can therefore connect directly to the LAN9692 SFI high speed interfaces. The SFI interface can host a variety of optical modules by complying to different speeds: 10Gbit/s, 2.5Gbit/s, 1000BASE-X, and 100Base-FX, as well as copper SFPs through XFI and SGMII. It is also possible to support 10GBase-KR, 5GBASE-KR, 2500Base-KR, and 1000Base-KX by using DAC cabling.

The EVB-LAN9692-LM serves four SFP+ slots using an on-board I²C clock multiplexer. The semi-static control signals (RxLos, TxFault, TxDisable, ModuleDetect, and Rate-Select of the SFPs) are connected to LAN9692 Serial GPIO as detailed in Table 5-7. Likewise, the green and yellow LED signals to each SFP slot are also controlled by the Serial GPIO engine.

5.3.5 PCIe 2.0 End-point

Once enabled, the PCIe Gen2 end-point controller provides access to the Switch registers. The PCIe end-point supports frame injection and subtraction, but lacks a dedicated hardware engine for doing TCP/IP offloading. Therefore, the maximum possible bandwidth depends solely on the horsepower of the external CPU system.

Note: The LAN9692 PCIe interface cannot operate as host/root-complex.

[Table 5-12](#) describes the signals found in the on-board PCIe cable connector (OCu-Link). (BPTYPE=0, no I2C, PERST# (SB5) is open drain)

TABLE 5-12: OCULINK PIN DESCRIPTION

Signal	Direction	Pin	Pin	Direction	Signal
3.3V act Rx	NC	A1	B1	NC	5V
GND	—	A2	B2	—	GND
PERp0/PCIE_RX_P	In	A3	B3	Out	PETp0/PCIE_TX_P
PERn0/PCIE_RX_N	In	A4	B4	Out	PETn0/PCIE_TX_N
GND	—	A5	B5	—	GND
PERp1	NC	A6	B6	NC	PETp1
PERn1	NC	A7	B7	NC	PETn1
GND	—	A8	B8	—	GND
2W-CLK	NC	A9	B9	In	BPTYPE/VSP, 10k pull-down
2W-DATA	NC	A10	B10	In	CWAKE _n , OBFF/VSP, 10k pull-up
GND	—	A11	B11	—	GND
PCIE_PERST _n (VSP), 10k pull-up	—	A12	B12	In	PCIE_CLK_P/VSP
CPRSNT(VSP), 1k pull-down	—	A13	B13	In	PCIE_CLK_N/VSP
GND	—	A14	B14	—	GND
PERp2	NC	A15	B15	NC	PETp2
PERn2	NC	A16	B16	NC	PETn2
GND	—	A17	B17	—	GND
PERp3	NC	A18	B18	NC	PETp3
PERn3	NC	A19	B19	NC	PETn3
GND	—	A20	B20	—	GND
5V	NC	A21	B21	NC	3.3V act TX

5.4 REFERENCE CLOCKS, SYNCHRONIZATION, AND PTP

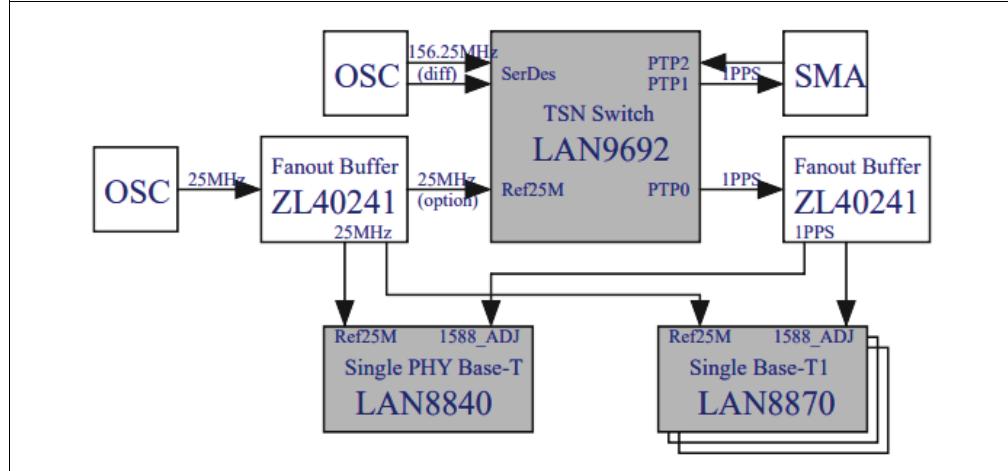
5.4.1 Switch and CuPHY Reference Clocks

The LAN9692 Switch is driven by an Automotive grade high performance differential MEMS oscillator, DSA12x2-156.25MHz. The same oscillator is per default also driving the VCore-IV CPU subsystem and 1588 PTP engines.

The use of a differential clock offers the advantage of less jitter than a single-ended clock. This is required for complying to the reference clock specifications, when operating the 10G ports. Typically, a differential clock and PCB traces also emit less radiated noise than a single-ended clock.

Detailed Hardware Description

FIGURE 5-10: REFERENCE CLOCKS AND PTP TIMING DIAGRAM



The eight LAN88xx CuPHYs are also driven by an Automotive grade single-ended MEMS oscillator, DSA11x1-25MHz.

A single-ended Clock buffer, ZL40241 is used for distribution of the 25 MHz clock to the PHYs. The use of the single-ended Clock buffer offers a cost advantage compared to a differential clock buffer.

Optionally, the VCore-IV CPU sub-system can also be sourced by this 25 MHz clock through changing the strapping resistor on REFCLK_SEL, or it can be controlled by a GPIO pin on the MIC2200 UART-to-USB serial converter.

The Switch 25 MHz reference clock input has an additional resistor divider to accommodate the Switch 1.8V IO-level.

5.4.2 PTP Engines

The EVB-LAN9692 reference design uses three out of LAN9692 eight PTP engines.

- PTP.SYNC0 is used to generate a 1PPS LOAD signal to the eight on-board CuPHYs for the PHY LTC time-stamp adjustment. The 1PPS signal is distributed as single-ended clocks to all CuPHYs by using a ZL40241 Clock buffer.
- PTP.SYNC1 is used to generate a 1PPS signal to an output dedicated SMA connector.
- PTP.SYNC2 is used to receive a 1PPS signal from either an input dedicated SMA connector or from a device, like a Raspberry Pi compatible GPS module, connected to the Expansion header, J4.

5.4.3 SMA Connectors

The EVB-LAN9692 reference board offers two SMA connectors to support IEEE 1588 1PPS input and output signalling as detailed in [Table 5-13](#).

The input SMA connector, PTP IN is available for a 1PPS signal into the LAN9692 PTP engine 2. The input is LVTTL and 3.3V tolerant – it is not 5V tolerant.

The output SMA connector, PTP OUT is controlled by LAN9692 PTP engine 1.

The output also provides 3.3V levels

TABLE 5-13: SMA CONNECTORS

SMA name	Connector	Description
PTP IN	J13	1PPS to Switch PTP.SYNC2 engine
PTP OUT	J14	11PPS to Switch PTP.SYNC1 engine

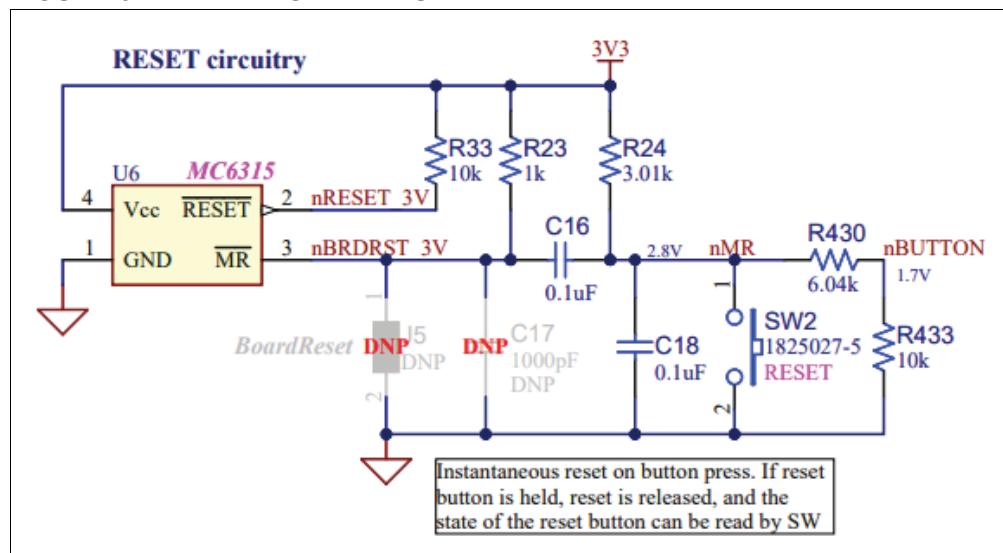
5.5 RESET CIRCUITRY

The nRESET signal is the overall board Reset and is generated by using a Microchip MIC6315-26D2UY (2.6V, 20ms) voltage supervisor. nRESET is asserted, when the 3.3V supply falls below the threshold, the **Reset** button SW2 is being pressed or when the nMR (Master-Reset) is asserted through the UART-to-USB serial converter GPIO.

The **Reset** button (SW2) is available on the back of the reference board. When pressed, it drives the input of the voltage supervisor low, and hereby creating a hard board Reset. It functions as a one-shot, so pressing it causes a Reset pulse, but it (nBUTTON) can afterwards be sampled by firmware to determine if it is still being pressed during boot-up.

Finally, board Reset can be generated or prolonged through nRESET_3V in the Expansion header, J4. See [Figure 5-11](#).

FIGURE 5-11: RESET CIRCUITRY



During board Reset, a yellow LED, D1 is switched on. nPHYRESET is controlled through LAN9692 GPIO output. The nPHYRESET has a 1 kΩ pull-up resistor to avoid Reset, when not being controlled.

5.6 EXPANSION HEADER

The Expansion header, J4, is a 2x20, 0.1" pin connector and is partially Raspberry Pi compatible. It can be used for programming the NOR Flash or give an external CPU control over the SPI client register interface. It is also exposing various LAN9692 GPIO signals in alternate mode.

The GPIO mapping towards the Expansion header can be seen in [Table 5-14](#). All signals are 3.3V levels.

TABLE 5-14: 2X20-PIN EXPANSION HEADER, J4

Signal	Direction	Pin	Pin	Direction	Signal
3.3V	Out	1	2	Out	5V
I2C SDA (FLEXCOM1)	BiDir	3	4	Out	5V
I2C SCL (SEL=7)	Out	5	6	—	GND
Spare	NC	7	8	Out	UART TXD (FLEXCOM1)
GND	—	9	10	In	UART RXD (FLEXCOM1)
Spare	NC	11	12	In	PTP_IN (SYNCE5) (1PPS)

Detailed Hardware Description

TABLE 5-14: 2X20-PIN EXPANSION HEADER, J4 (CONTINUED)

Signal	Direction	Pin	Pin	Direction	Signal
Spare	NC	13	14	—	GND
Spare	NC	15	16	NC	Spare
3.3V	Out	17	18	In	VCORE2
Spare	NC	19	20	—	GND
Spare	NC	21	22	In	nRESET
Spare	NC	23	24	In	VCORE0
GND	—	25	26	In	VCORE1
Spare	NC	27	28	NC	Spare
Spare	NC	29	30	—	GND
Spare	NC	31	32	NC	Spare
VCORE3	In	33	34	—	GND
SPI.DI	In	35	36	In	SPI.nCS
Spare	NC	37	38	Out	SPI.D0
GND	—	39	40	In	SPI.SCK

Note: An add-on board using the Expansion header MUST have its own Power-on Reset (POR), and the overall power consumption should be considered. Likewise, ensure that the VCORE[3:0] strapping settings are not overridden unintentionally. If the add-on board is intended to overwrite the board strapping, SW1 must be set to '0000'.

5.7 POWER DISTRIBUTION

The reference board is powered through either a standard 12V DC barrel jack, J23. When being unplugged – a 10 kΩ resistor is sinking the bulk capacitors placed on the input side of the 12V DC/DC converters.

5.7.1 DC/DC Converters

The 12V power supply sources a number of different 12V DC/DC converters:

- 0.9V for LAN9692 core supply (VDD, 5A) and SerDes10G IO (VDDHS, 1.6A and VDDHV, 0.1A). The DC/DC converter carries a calculated total load of 6.7A. Max current is 8A.
- 3.3V for SFP (3.0A) and CuPHYs IO and analog high (0.5A).
- The calculated load is 3.5A + 2A from Expansion header. Maximum current is 8A.
- 5V for additional DC/DC converters.
- The calculated load is 1.2A + 2A from Expansion header. Maximum current is 8A.

Table 5-15 summarizes the 12V power usage.

TABLE 5-15: 12V DC POWER USAGE

12V DC/DC Converters	Supply (V)	Maximum Current (A)	Power (W)
PM-MCP19035, LAN9692 core and 10G SerDes	0.9	6.7	6.0
PM-MCP19035, LAN8870/LAN8840 IO and SFP+	3.3	5.5	18.0
PM-MCP19035, additional DC/DC conversion\	5.0	3.2	16.0
Power Dissipation in Supply (at 80% efficiency)	—	—	—
Total 12V	12.0	4.0	48.0

A 5V DC power supply is generated from the 12V supply and sources the following local DC/DC converters:

- 1.1V for CuPHYs core supply and analog low. LAN8840(0.2A)+LAN8870(2.8A). The calculated load is 3.0A. Maximum current is 3A.
- 1.8V for LAN9692 (VDDIO18, 0.5A), SerDes (VDDH, 0.3A) + other (0.4A). The calculated load is 1.2A. Maximum current is 3A.

The 5V power supply also feeds direct power to the Expansion header. [Table 5-16](#) summarizes the 5V power usage.

TABLE 5-16: 5V DC POWER USAGE

5V DC/DC Converters	Supply (V)	Maximum Current (A)	Power (W)
PM-MIC22405, PHY core and analog low	1.1	3.0	3.3
PM-MIC22405, LAN9692: VDDIO, VDDH	1.8	1.2	2.2
Power dissipation in supply (at 80% efficiency)	—	—	—
Total 5V	5.0	1.2	6.0

The 3.3V DC power supply sources most of the board components, like eMMC NAND Flash, OSC's, clock buffers, shift registers, SFP slots and Expansion header.

To source the T1 PHYs running SGMII with 2.5V, a local LDO, MIC5377-YC5-TR is being populated at each LAN8870, VPH supply.

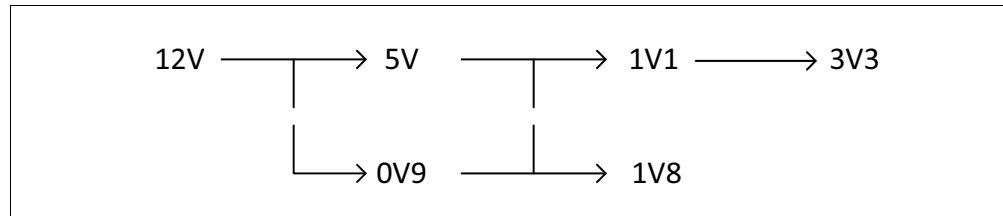
5.7.2 Power Supply Sequencing

The strategy for the power supply sequencing is not to let a higher-powered supply feeding lower-level powered grids through the device internal protection diode network. The general power supply sequence is therefore:

- LAN9692: 0V9 -> 1V8
- Others: 1V1 -> 3V3

The overall power sequencing is illustrated in [Figure 5-12](#).

FIGURE 5-12: POWER SEQUENCING



Detailed Hardware Description

5.7.3 Power Supply, Test Points and LEDs

To measure the output voltage of the various power supplies, test points are populated close to each supply and consist of a 2-pin header/footprint (power, return ground). In addition, a green LED on each supply indicates power is ON.

One red LED, D6 will indicate, if one of the supplies fails. It is located at the 3.3V power-enable signal.

TABLE 5-17: TEST POINT AND LEDS

Supply	Direction	Green LED	Red LED
12V	CR23	—	—
5V	J7	D9	D6
3.3V	J9	D12	—
1.8V	J6	D14	—
1.1V	J10	D13	—
0.9V	J8	D10	—

Chapter 6. Environmental Requirements

6.1 STORAGE AND OPERATING CONDITIONS

The reference board is designed to operate within the following temperatures (case and airflow dependent):

- Operating temperature: -40° to +85°C
- Storage temperature: -10° to +70°C
- Operating humidity: 10% to 95% relative humidity, non-condensing

Environmental Requirements

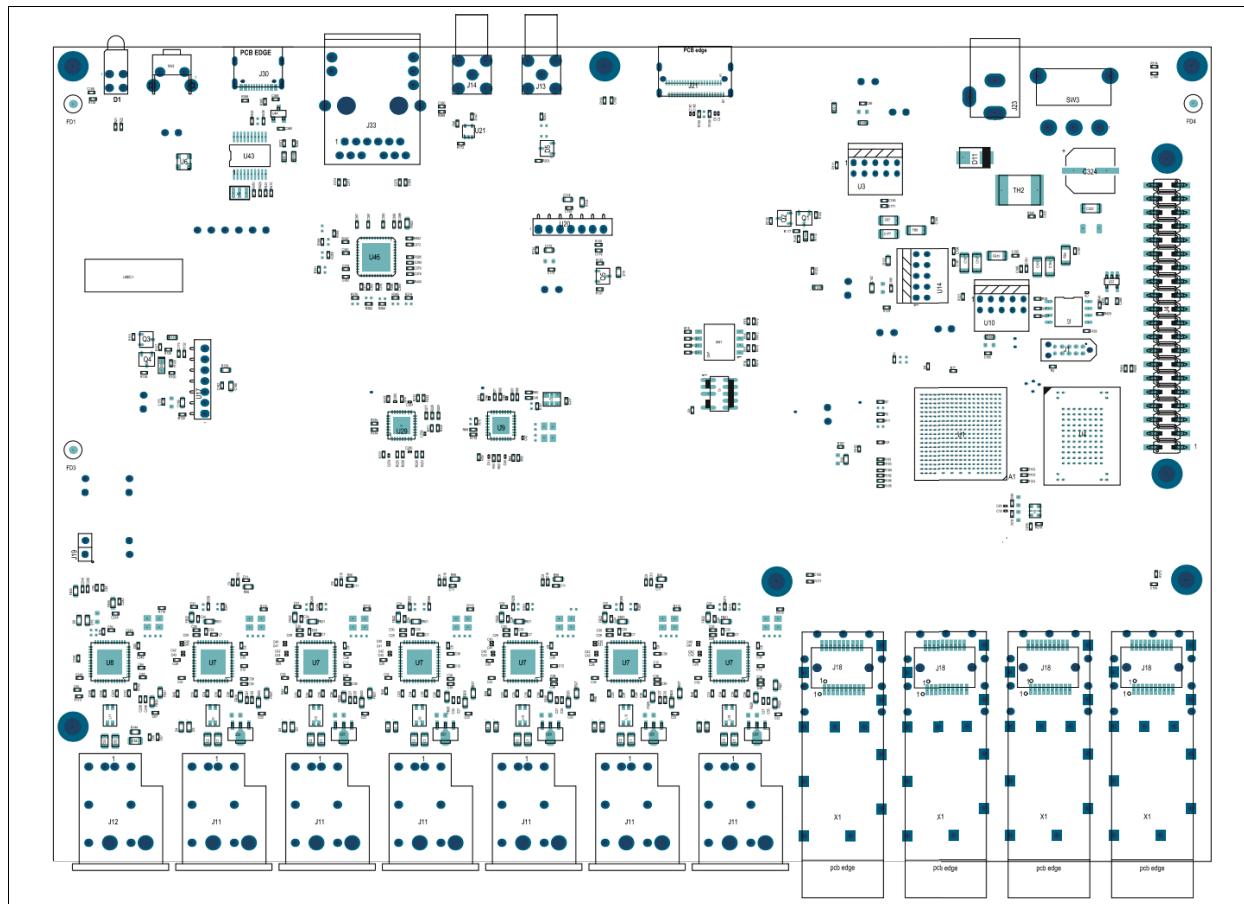
NOTES:

Appendix A. PCB Layout

A.1 DIMENSION

Figure A-1 shows the board outline. The board dimensions are 214 x 150 mm.

FIGURE A-1: EVB-LAN9692-LM REFERENCE BOARD OUTLINE



A.2 PCB LAYERS

The reference board uses four PCB layers. Refer to [Table A-1](#).

The ground shield serves as **quiet** ground for PHY copper media signals and SFP cages. It couples capacitively to the ground plane, providing a low-impedance return path for high-frequency noise.

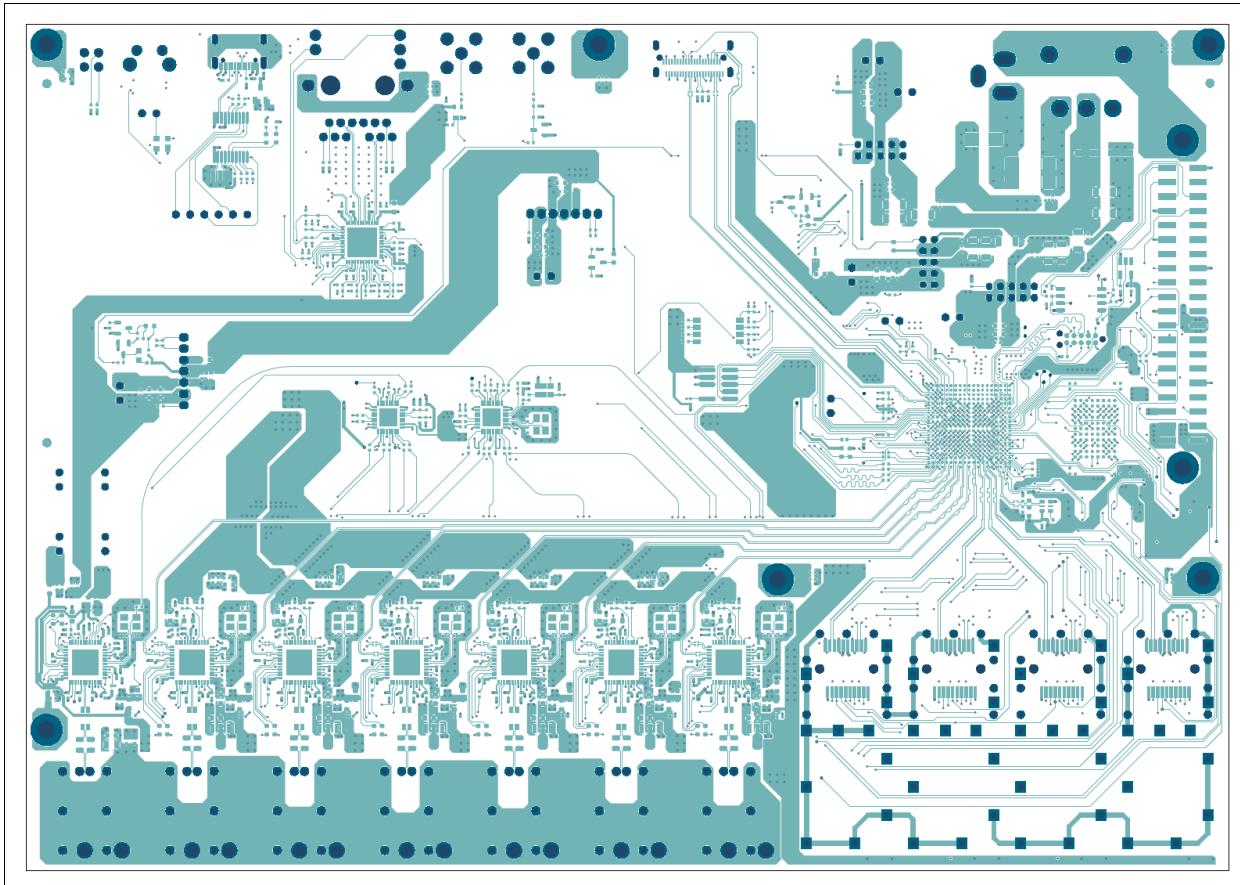
TABLE A-1: PCB LAYER OVERVIEW

Layer	Description
1	Top. LAN9692 signal traces. SerDes Tx paths to PHYs and SFP.
2	Ground
3	Ground and power
4	Bottom. LAN9692 signal traces. SerDes Rx paths to PHYs and SFP.

A.2.1 Layer 1 – Top Layer

SerDes Tx Macros. See [Figure A-2](#).

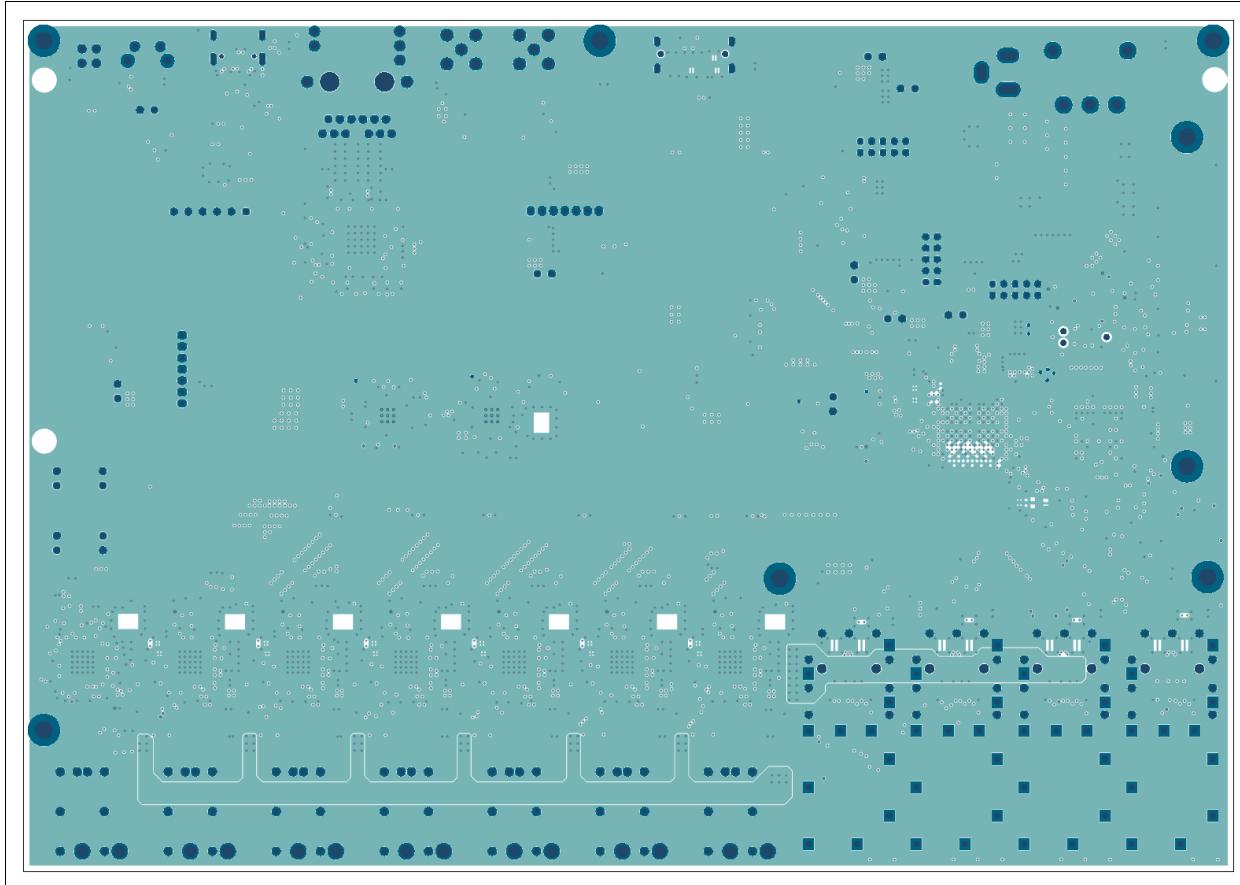
FIGURE A-2: LAYER 1 – TOP LAYER



A.2.2 Layer 2 – Ground Layer

Ground plane. See [Figure A-3](#).

FIGURE A-3: LAYER 2 – GROUND LAYER



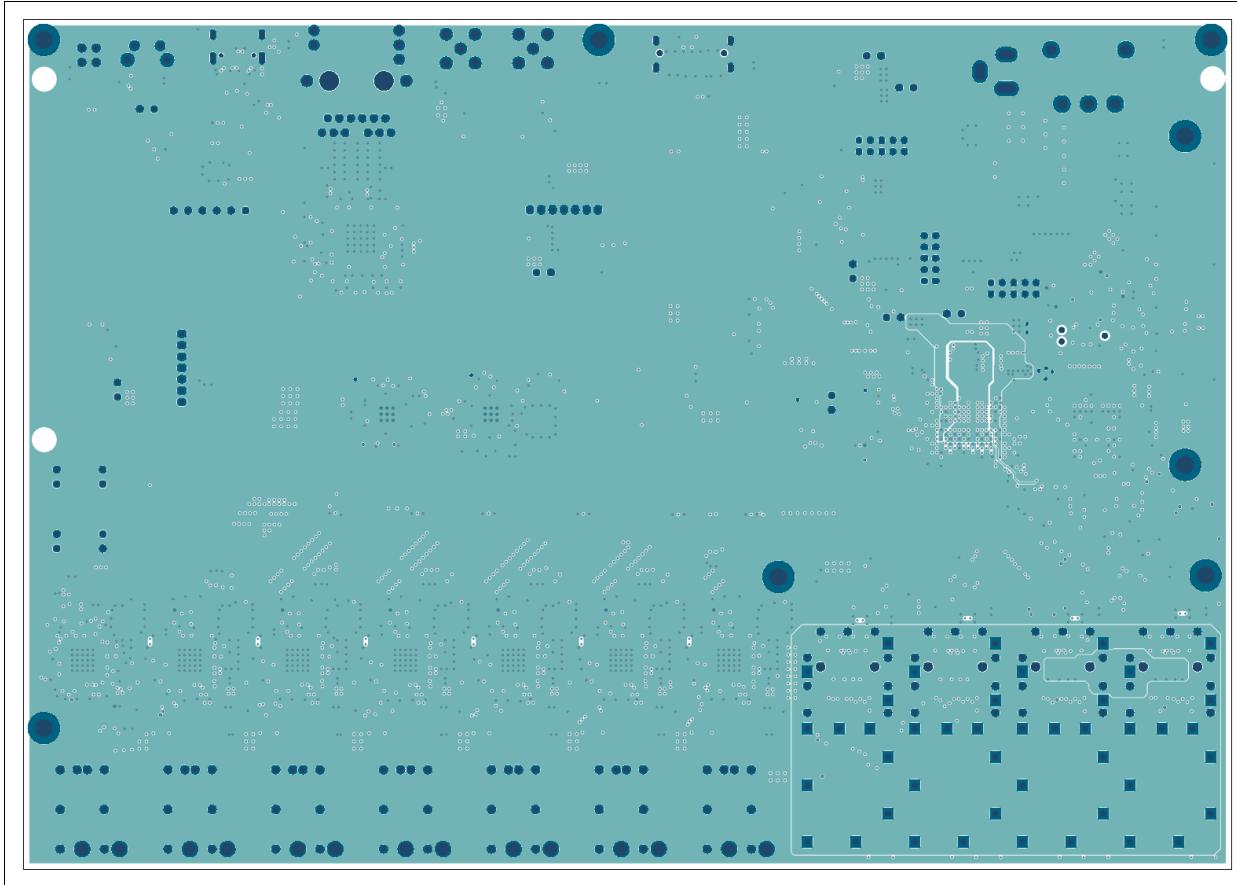
A.2.3 Layer 3 – Combined Power and Ground Layer

Various power planes. Refer to [Figure A-4](#).

Power planes, mainly the 3V3. The 1V1 is made *short and wide* as possible.

The plane is the SFP shield ground. Signal traces for RGMII to Single PHYs.

FIGURE A-4: Layer 3 – Combined Power and Ground Layer

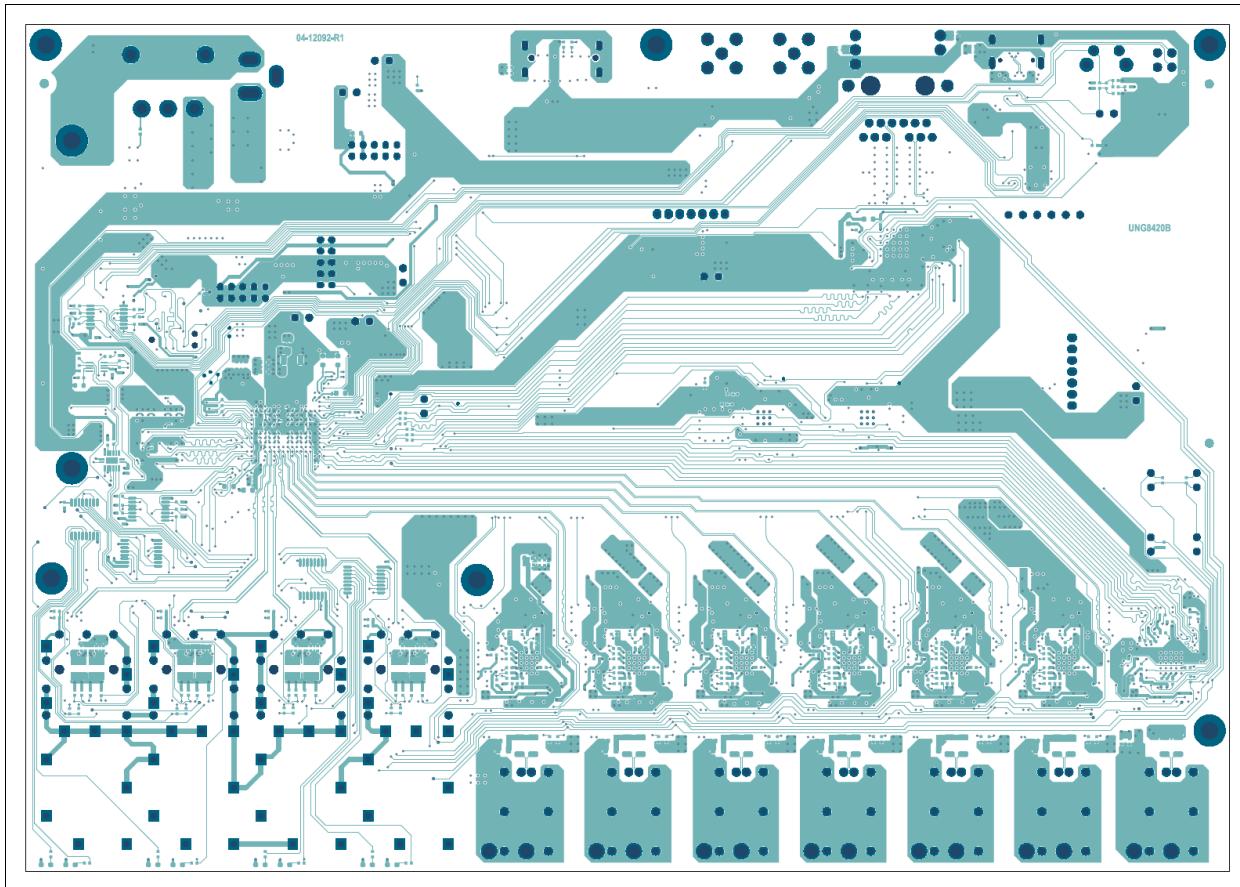


A.2.4 Layer 4 – Bottom Layer

Signal traces for SerDes Rx macros. See [Figure A-5](#).

Copper PHY MIIM

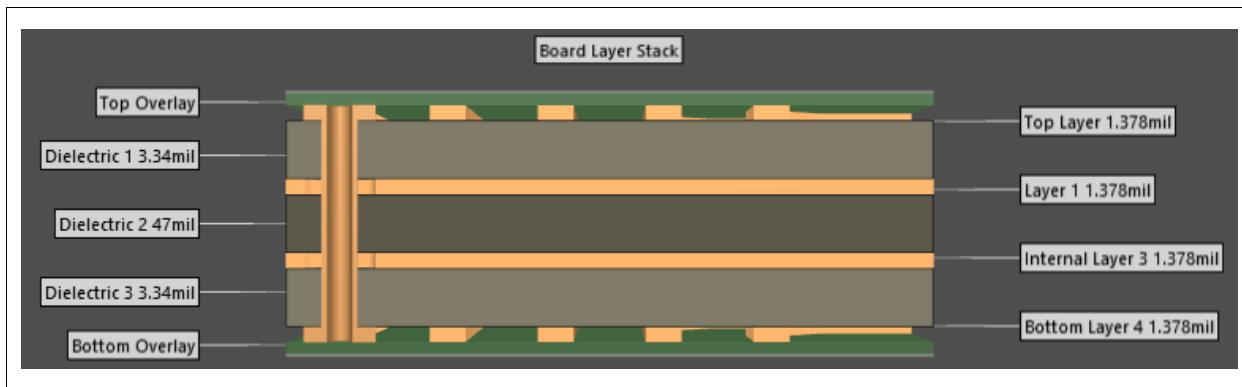
FIGURE A-5: LAYER 4 – BOTTOM LAYER



A.3 PCB LAYER STACK-UP

The EVB-LAN9692-LM reference board is a four-layer impedance-controlled PCB. The stack-up is shown in [Figure A-6](#).

FIGURE A-6: BOARD LAYER STACK



A.3.1 PCB Trace Widths, Clearance, and Impedance

TABLE A-2: PCB STACK-UP, TRACE WIDTHS, AND IMPEDANCE

Name	Material	Thickness	Constant Dk/Df	Impedance Width/Spacing
Top overlay	—	—	—	—
Top solder	LPI Green	0.500 mil	3.5/0.025	—
Top finish	ENIG_3-6um Ni, 0.05-0.1um Au.	0.157 mil	—	—
Top layer	CF-002 1/3 oz. plated up per IPC	1.350 mil	—	50Ω SE: 6.0 mil 60Ω SE: 5.0 mil 85Ω Diff: 6.5/5.0, 8/12 mil 100Ω Diff: 5.0/5.0 mil
Dielectric1	PP-370HR_1086_65.0_-3.4	3.340 mil	3.88/0.0234	—
Layer 2	CF-004	1.378 mil	—	—
Dielectric 2	CR-FR408HR-28mil	47 mil	4.4/0.02	—
Layer 3	CF-004 1 oz. Base	1.378 mil	—	—
Dielectric 3	PP-370HR_1086_65.0_-3.4	3.340 mil	3.88/0.0234	—
Bottom layer	CF-002 1/3 oz. plated up per IPC	1.350 mil	—	50Ω SE: 6.0 mil 60Ω SE: 5.0 mil 85Ω Diff: 6.5/5.0, 8/12 mil 100Ω Diff: 5.0/5.0 mil
Bottom finish	ENIG_3-6um Ni, 0.05-0.1um Au.	0.157 mil	—	—
Bottom solder	LPI-Green	0.500 mil	3.5, 0.025	—
Bottom overlay	—	—	—	—
Board thickness	(1.535 mm)	60.45 mil	—	—

TABLE A-3: NET IMPEDANCE AND LENGTH MATCHING

Net Group	Type	Impedance	Length matching	Tolerance (mm)	Max vias	Via type	Layers	Notes
Clock	SE	50Ω	None	—	4	All	Outer	—
SI	SE	50Ω	None	—	4	All	Outer	Daisy-chain
USB	DIFF	85Ω	P/N only	1	2	All	Outer	—
DiffClock	DIFF	100Ω	P/N only	1	4	All	Outer	—
DiffClockCrit	DIFF	100Ω	P/N only	1	2	All	Outer	4
SerDes10G	DIFF	100Ω	P/N only	0	2	—	Outer	1
Sense	Analog	—	—	—	—	All	Outer	—
Power	Power	—	—	—	—	—	All	—
Static	SE	—	—	—	—	—	Outer	2
Unspecified	SE	60Ω	—	—	—	—	Outer	3

Note 1: Differential signal on outer layers.

2: No impedance => 4 mil trace on any layer.

3: Any unspecified nets should be routed as 60Ω.

4: Critical clock nets: CLK156 - route with extra clearance.