Cryptuino01 – Main part

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To-do until 14.01.2021

1. The Project name must be formatted like this: Cryptuino01_**FPG** (**F**amily name, **P**atronym, **G**iven Name= **ФИО**)
2. Enter the schematic correctly into KiCAD. Add all necessary things to pass the ERC check without errors.
3. Assign footprints to components:
    a. All passive components (RLC) are 0805
    b. The FT245RL Chip is SSOP-28 – the correct pitch is to be looked up in the datasheet
    c. The ATTiny is a QFN-20 Package
    d. All Logic chips are SOP-14 / SOIC-14
    e. For the USB-C Connector use the "USB_C_Receptacle_HRO_TYPE-C-31-M-12" footprint
    f. All other connectors are Pin sockets with 100mil pitch
    g. You can change the 1x06 Programming Connector to a 2x03. Keep the same pitch.

4. Create a complete PCB Design using 2 Layers and a surface smaller or equal 50x70mm
    a. Use different trace widths for power and data
    b. Route correctly all differential signal trace pairs (if there are)
    c. Ground net copper fills on both layers. Place enough vias to extend the copper fills to keep a constant "copper density" across the board (as much as possible)
    d. Use only 0.6mm/0.3mm vias
    e. Place decoupling elements correctly!
    f. DO NOT USE AUTOMATIC ROUTING
    g. See that inscriptions on the Silkscreen Layer don't overlap or cover other footprints
    h. Annotate the Programming Connector and the 8-bit Data Connector (Silkscreen)
    i. Add Board Dimensions on Eco2.User Layer

5. The Board MUST PASS a complete DRC Check without errors or unconnected elements
6. You are required to send a zipped archive of your project to following mail address : pcb_iu10@mail.ru
   no later than : **Friday 15.01.2021, 13:00 MSK (GMT+3)**

7. There will be an oral part of the exam (15min max.) where you'll have to argument your choices

8. For questions, first try really hard to solve them yourself. If you're still clueless, you'll have at your disposal a Telegram channel where you can consult each other. (Please consult, but do not copy without thinking). You can always ask me on Discord per DM.

Cryptuino01 – Bonus tasks

The bonus tasks are available for students advanced enough who need an additional challenge. They can give additional points that will be added to the next tests.

Nota Bene: However, they will be only taken into account if there are no errors (imperfections are ok) on the main part. So make sure, you master the main part before attacking the dragons of the bonus tasks ☺.

Medium difficulty:

There are 23 passive components, reduce them to 17 without changing the number of symbols on the electrical schema. (Hint: Do not touch the capacitors), and route the PCB accordingly.

High difficulty:

Instead of the USB_C_Receptacle_HRO_TYPE-C-31-M-12 for the USB-C Connector, use the following :

U262-161N-4BVC11 (see datasheet in /Bonus Folder)