

1

2

3

4

U1A

BANK 1

IO	D4	EXT3_11
IO	E5	EXT3_8
IO	F5	EXT3_6
IO, (DQS2L/CQ3L)/(DQS2L/CQ3L)	B1	SD_DAT1
IO, DIFFIO_L1p	C2	SD_DAT0
IO, DIFFIO_L1n, (DATA1_ASDO)	C1	FPGA_ASDO
IO, VREFB1N0	E3	
IO, DIFFIO_L2p, (FLASH_nCE,nCSO)	D2	FPGA_NCSO
IO, DIFFIO_L2n	D1	SD_CLK
IO	G5	EXT3_5
IO	F2	SD_CMD
IO, DIFFIO_L3p	F1	SD_DAT3
IO, DIFFIO_L3n	G2	SD_DAT2
IO, DIFFIO_L4p, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)	G1	
IO, DIFFIO_L4n	H2	FPGA_DATA
IO, (DATA0)		

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U1B

BANK 2

IO, DIFFIO_L5p, (DQ1L)/(C)	J2	
IO, DIFFIO_L5n, (DQ1L)/(C)	J1	EXT1_1
IO	K6	EXT0_3
IO, DIFFIO_L6p	K6	EXT0_4
IO, DIFFIO_L6n	L6	EXT0_8
IO, DIFFIO_L7p	K2	EXT1_3
IO, DIFFIO_L7n, (DQ1L)/(C)	K1	EXT1_2
IO, DIFFIO_L8p, (DQS1L/CQ1L#,DPCLK1)/(DQS1L/CQ1L#,DPCLK1)	L2	EXT1_5
IO, DIFFIO_L8n, (DQ1L)/(C)	L1	EXT1_4
IO, VREFB2N0	L3	EXT0_6
IO, DIFFIO_L9p, (DQ1L)/(C)	N2	EXT1_6
IO, DIFFIO_L9n, (DQ1L)/(C)	N1	EXT1_7
IO, RUP1, (DQ1L)/(C)	K5	EXT0_5
IO, RDN1, (DQ1L)/(C)	L4	EXT0_7
IO, (DQS3L/CQ3L#)/(DQS3L/CQ3L#)	R1	EXT1_11
IO, DIFFIO_L10p, (DQ1L)/(C)	P2	EXT1_10
IO, DIFFIO_L10n, (DM1L/BWS#1L)/(C)	P1	EXT1_9

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U1C

BANK 3

IO, DIFFIO_B1p	N3	EXT1_8
IO, DIFFIO_B1n, (DM3B/BWS#3B)/(DM5B/BWS#5B)	P3	EXT0_10
IO, DIFFIO_B2p, (DQ3B)/(DQ5B)	R3	EXT1_13
IO, DIFFIO_B2n	L3	EXT1_14
IO, (DQS1B/CQ1B#,DPCLK2)/(DQS1B/CQ1B#,DPCLK2)	L2	EXT1_12
IO, PLL1_CLKOUTp	R4	EXT1_15
IO, PLL1_CLKOUTn	L4	EXT1_16
IO, DIFFIO_B4p, (DQ3B)/(DQ5B)	N5	EXT0_9
IO, DIFFIO_B4n, (DQ3B)/(DQ5B)	N6	EXT0_11
IO, (DQ3B)/(DQ5B)	M6	EXT0_13
IO, VREFB3N0	P6	EXT0_12
IO, DIFFIO_B5p, (DQS3B/CQ3B#)/(DQS3B/CQ3B#)	M7	EXT0_14
IO, DIFFIO_B5n	K8	EXT0_2
IO, DIFFIO_B6p, (DQ3B)/(DQ5B)	R5	EXT1_17
IO, DIFFIO_B6n	L5	VGA_VS
IO, DIFFIO_B7p, (DQ3B)/(DQ5B)	R6	VGA_HS
IO, DIFFIO_B7n	L6	VGA_B0
IO, (DQ3B)/(DQ5B)	L7	EXT1_18
IO, DIFFIO_B8p, (DQ3B)/(DQ5B)	R7	VGA_B1
IO, DIFFIO_B8n, (DQS5B/CQ5B#)/(DQS5B/CQ5B#)	L7	VGA_B2
IO, DIFFIO_B9p, (DQ3B)/(DQ5B)	L8	SM_SEL0
IO, DIFFIO_B9n, (DM5B/BWS#5B)/(DM5B/BWS#5B)	M8	EXT0_16
IO, DIFFIO_B10p, (DQ5B)/(DQ5B)	N8	EXT0_15
IO, DIFFIO_B10n, (DQ5B)/(DQ5B)	P8	VGA_B3
IO, DIFFIO_B11p	R8	
IO, DIFFIO_B11n	L8	VGA_B4

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U1D

BANK 4

IO, DIFFIO_B12p	R9	VGA_G2
IO, DIFFIO_B12n	L9	VGA_G1
IO, DIFFIO_B13p	K9	
IO, DIFFIO_B13n	L9	SM_SEL1
IO, DIFFIO_B14p	M9	SM_SEL3
IO, DIFFIO_B14n, (DQ5B)/(DQ5B)	N9	SM_SEL2
IO, DIFFIO_B15p, (DQ5B)/(DQ5B)	R10	VGA_G4
IO, DIFFIO_B15n, (DQS4B/CQ5B)/(DQS4B/CQ5B)	L10	VGA_G3
IO, DIFFIO_B16p, (DQ5B)/(DQ5B)	R11	VGA_R0
IO, DIFFIO_B16n	L11	VGA_G5
IO, DIFFIO_B17p, (DQ5B)/(DQ5B)	R12	VGA_R2
IO, DIFFIO_B17n, (DQ5B)/(DQ5B)	L12	VGA_R1
IO, DIFFIO_B18p	K10	SDRAM1_DQ12
IO, DIFFIO_B18n	L10	EXT3_25
IO, (DQS2B/CQ3B)/(DQS2B/CQ3B)	P9	VGA_G0
IO, VREFB4N0	P11	SM_G
IO, DIFFIO_B19p	R13	VGA_R3
IO, DIFFIO_B19n, (DQ5B)/(DQ5B)	L13	UART_TXD
IO, RUP2	M10	SM_F
IO, RDN2	N11	SM_DP
IO, DIFFIO_B20p, (DQ5B)/(DQ5B)	L14	VGA_R4
IO, DIFFIO_B20n, (DQS0B/CQ1B,DPCLK3)/(DQS0B/CQ1B,DPCLK3)	L15	KEY1
IO	R14	KEY0
IO, DIFFIO_B21p	P14	SM_B
IO, DIFFIO_B21n	L11	EXT3_26
IO, DIFFIO_B22p	M11	EXT3_27
IO, DIFFIO_B22n	N12	UART_RXD

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BANK 5

IO	N13	FPGA_P22
IO	M12	FPGA_P21
IO	L12	FPGA_P26
IO	K12	FPGA_P27
IO	N14	FPGA_P20
IO, RUP3, (DM1R/BWS#1R)/(C)	P15	FPGA_P23
IO, RDN3, (DQ1R)/(C)	P16	SM_C
IO, DIFFIO_R11n, (DQS3R/CQ3R#)/(DQS3R/CQ3R#)	R16	SM_A
IO, DIFFIO_R11p, (DQ1R)/(C)	K11	EXT3_28
IO	N16	SM_E
IO, DIFFIO_R10n, (DQ1R)/(C)	N15	SM_D
IO, DIFFIO_R10p, (DQ1R)/(C)	L14	FPGA_P25
IO, VREFB5N0	L13	FPGA_P24
IO, (DQ1R)/(C)	L16	FPGA_P33
IO, DIFFIO_R9n, (DQ1R)/(C)	L15	FPGA_P34
IO, DIFFIO_R9p	P11	SDRAM1_DQ13
IO	K16	FPGA_P31_TXD
IO, DIFFIO_R8n, (DQ1R)/(C)	L15	FPGA_P32
IO, DIFFIO_R8p, (DQS1R/CQ1R#,DPCLK4)/(DQS1R/CQ1R#,DPCLK4)	L16	FPGA_P17_SCK
IO, DIFFIO_R7n, (DEV_OE)	L15	FPGA_P30_RXD
IO, DIFFIO_R7p, (DEV_CLRn)	L14	IR_IN
IO, DIFFIO_R6n, (DQ1R)/(C)	L12	SDRAM1_DQ14
IO, DIFFIO_R6p	L13	SDRAM1_DQ15
IO, (DQ1R)/(C)		

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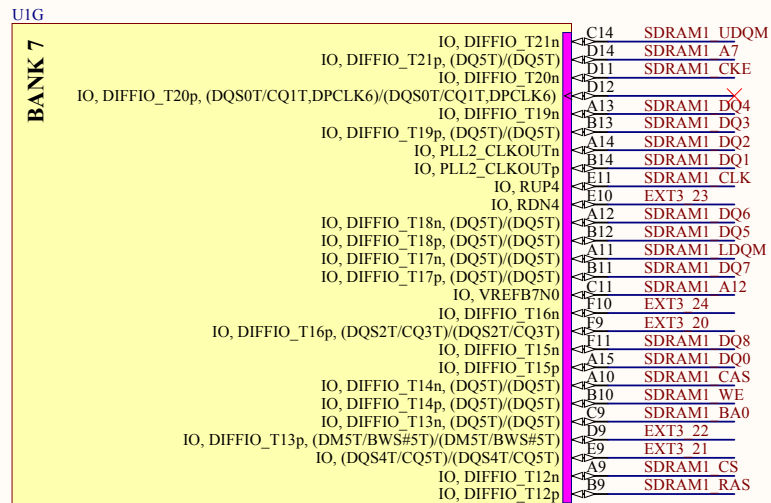
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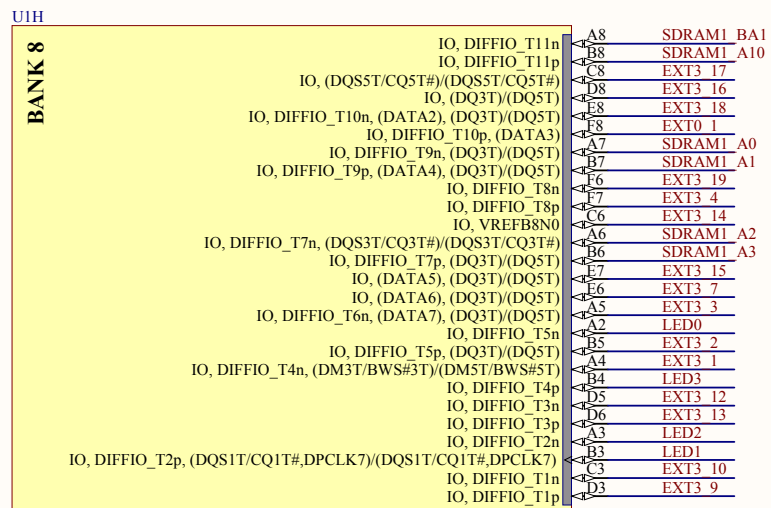
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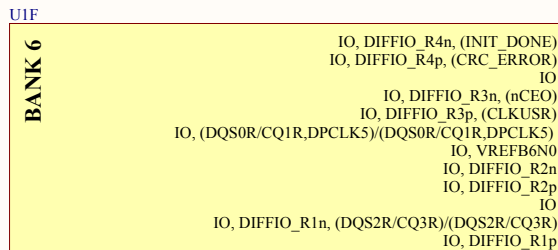
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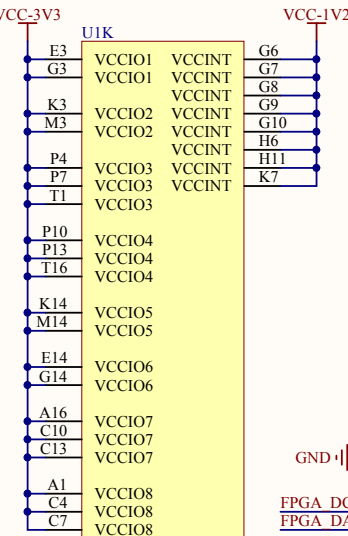
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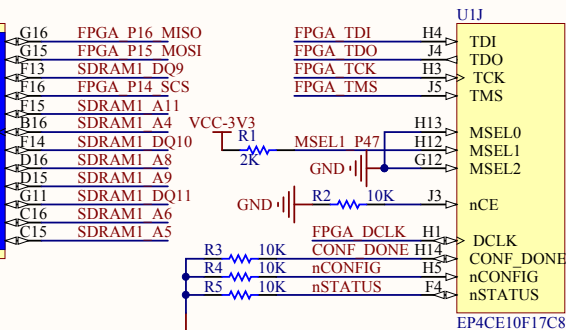
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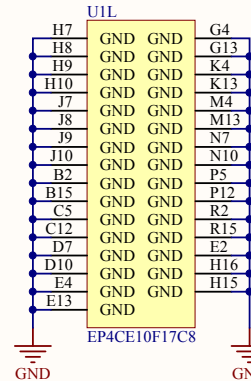
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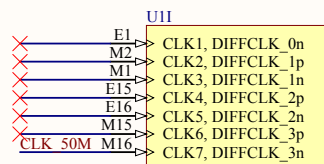
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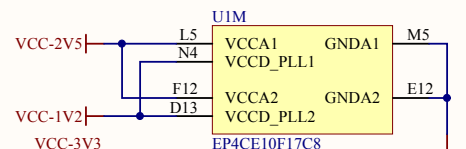
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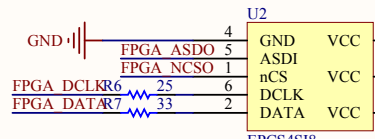
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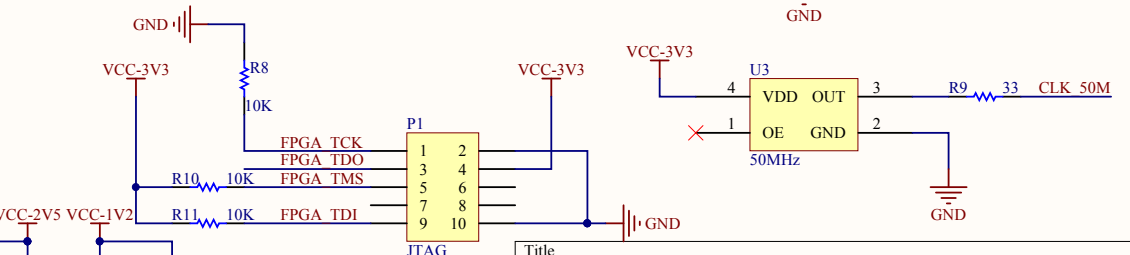
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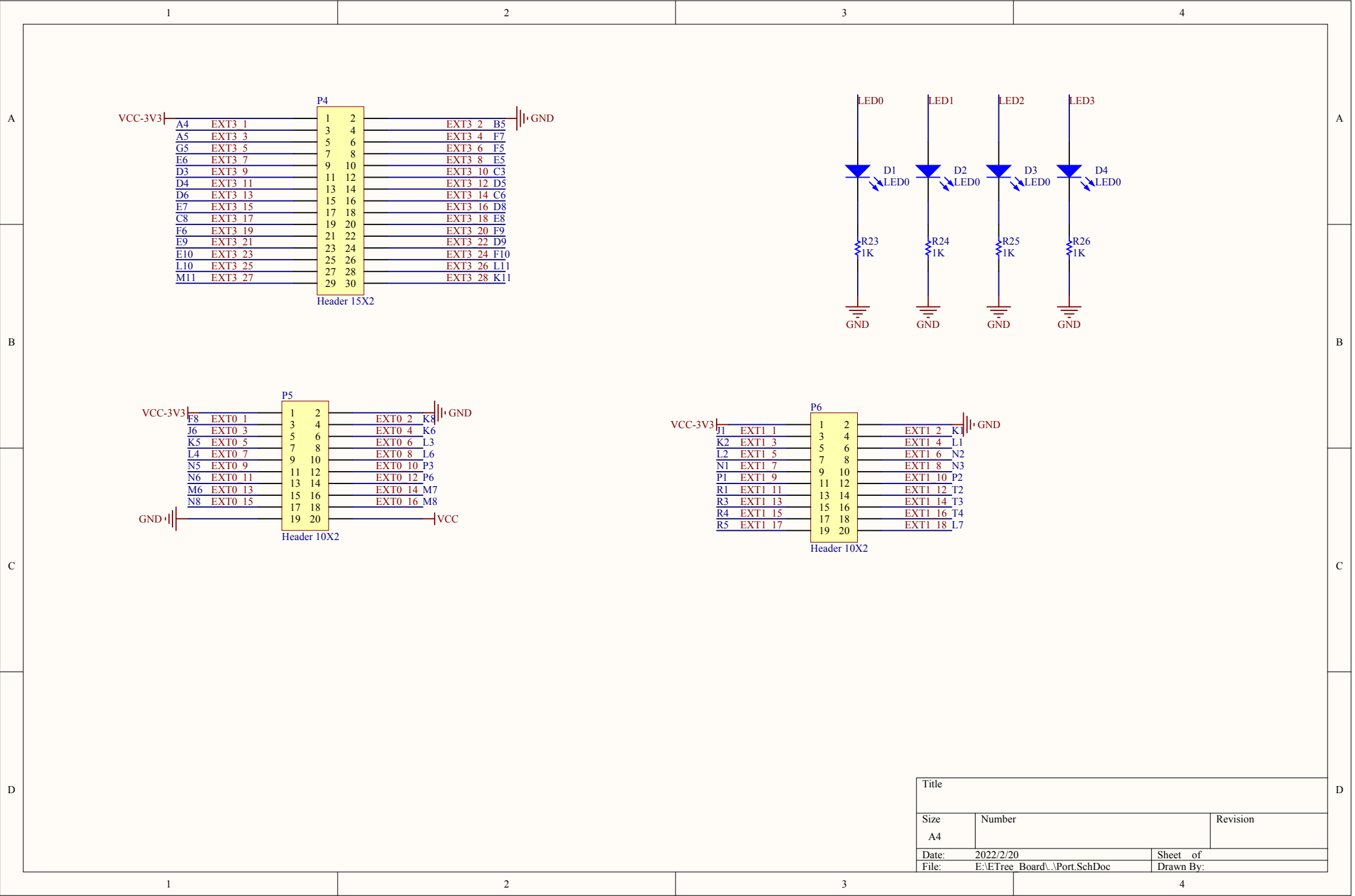


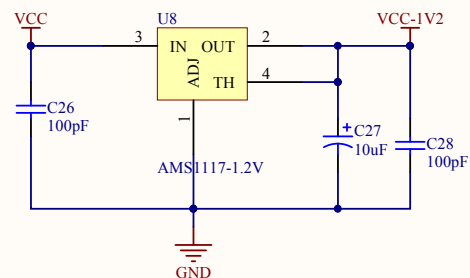
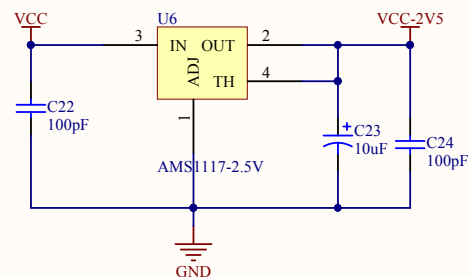
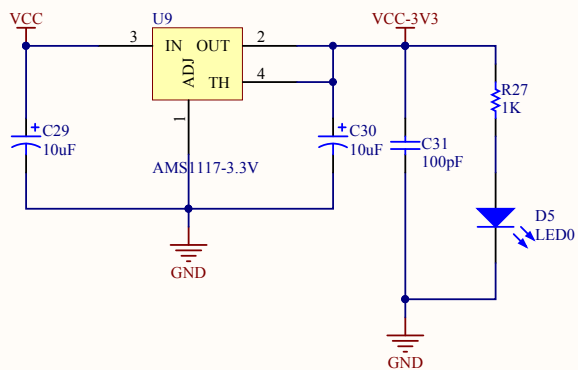
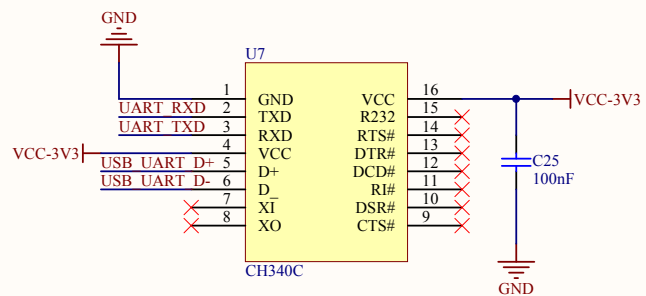
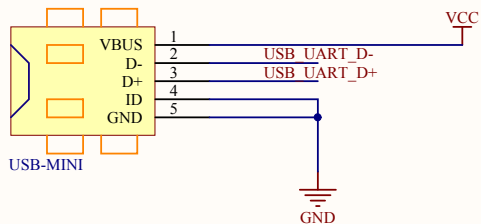
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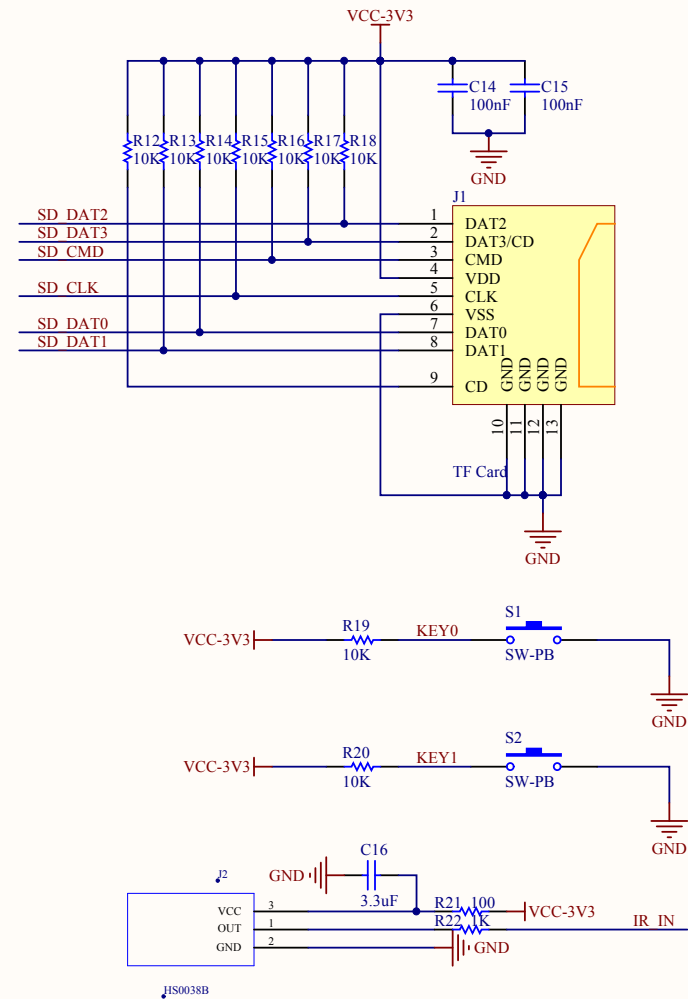
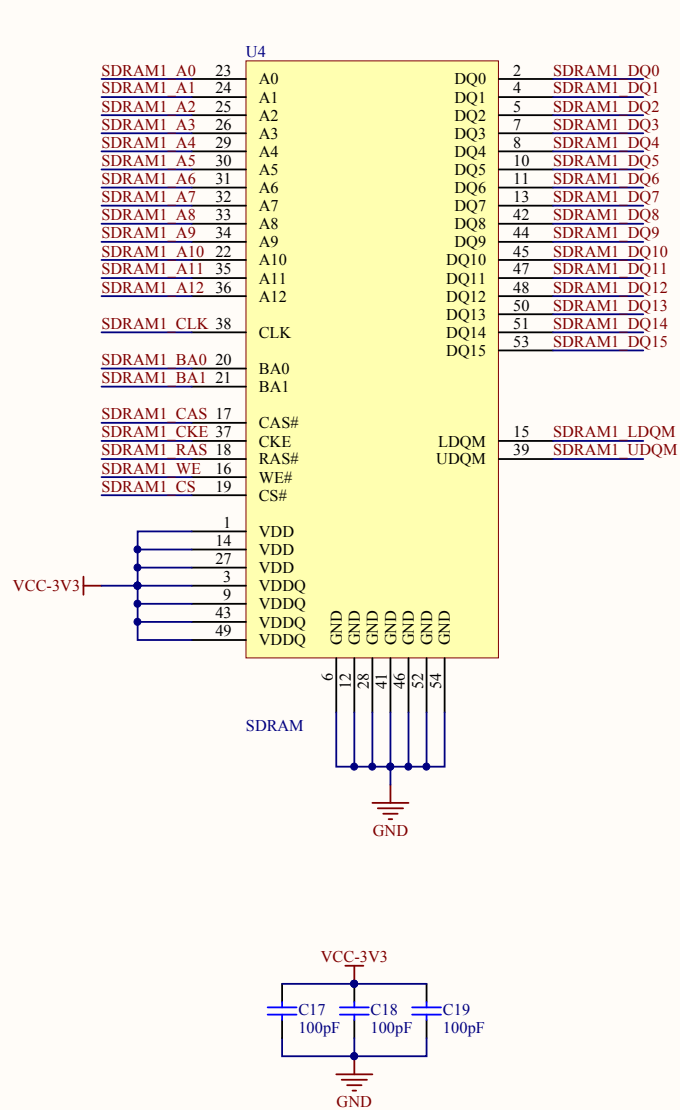
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