Xiaofeng Hu

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Education

Huazhong University of Science and Technology (HUST) **Wuhan, China**
School of Optical and Electronic Information 09/2016—06/2020
B.Eng in **Integrated Circuits and Systems (Expected)** **GPA**: 3.84/4.0

Academic scholarship 1200 RMB, School of Optical and Electronic Information, HUST 09/2018& 09/2017

Research Experience

Department of Electrical and Computer Engineering, Rutgers University **NJ, USA**
Intern of Summer Research 07/2019—09/2019
Project: Tensor decomposition accelerator **Advisor:** Dr. Bo Yuan
Object: Design an accelerator from algorithm level to hardware architecture for Tucker decomposition Algorithm

- ✧ Mastered current Tensor Decomposition Algorithm - Tucker Decomposition and its popular implementation methods
- ✧ Proposed two optimized implementation methods of SVD (Singular Value Decomposition) part of Tucker Decomposition and used Matlab to verify its superiority
- ✧ Evaluated proposed optimization's performance in the hardware platform
- ✧ Submitted a paper for IEEE-ICASSP-2020

School of Electronic Information and Communication, HUST **Wuhan, China**
Member 04/2019—06/2019
Project: Bi-Real Res-Net CNNs Implementation on FPGA **Advisor:** A/Prof. Xin Yang

- ✧ Determined the Hardware Streaming Architecture after paper-reading on the Binary Res-Net Module
- ✧ Completed Hardware Verilog RTL module and simulation work for Batch Normalization, SUM, and STATISTIC, DATA Distributor modules in the whole structure
- ✧ Integrated all modules into a single network layer for overall simulation to find out bottleneck that restricted the throughput of the system
- ✧ Modified hardware architecture based on simulation result by adding more parallel convolution modules and more cache to increase overall parallelism
- ✧ **Result:** Finally, the hardware speedup of the 3*3 binary convolutional layer was 15.8 times, and the overall speedup was 7.38 times, which reached the result of theoretical test from this paper

Undergraduate Training Program for Innovation and Entrepreneurship, HUST **Wuhan, China**
Team Leader 03/2018—01/2019
Project: Wavelength Locking of a Si-Ring Modulator Using an Integrated OMA Monitoring Circuit (Analog)
Advisor: Dr. Min Tan
Innovation Point: Apply fully integrated Silicon CMOS feedback circuit to stabilize Micro-ring tuning point

- ✧ Designed basic analog functional modules, including transimpedance amplifier(TIA), comparator, and then invoked the micro-ring model for the initial simulation
- ✧ Conducted full-integrated module design and synthesized the digital logic into analog module by myself
- ✧ Implemented system simulation in Cadence using TSMC 180nm process library to achieve promising result
- ✧ **Result:** Partly finished the fully-integrated feedback circuit's design and simulation, except for DAC/ADC module, and achieved the similar performance as the one proposed in 2016's JSSC

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Academic Activities

3rd Prize, ARM Cup National College Students Integrated Circuit Design Competition **Wuhan, China**
Team Leader 03/2019—06/2019
Project: Image recognition based on ARM Cortex-M3 processor

- ✧ Successfully drove OV 5640 camera by Verilog module and completed the corresponding configuration of Frames Per Second (FPS) and resolution ratio in ARM
- ✧ Finished hardware interconnection of whole SoC with AXI/AMBA Bus in Vivado, and successfully debugged CORTEX-M3 softcore with Arm Keil
- ✧ Built Video-streaming data path based on AXI4-VDMA and CORTEX-M3 softcore and achieved the real-time output of 30Hz video stream to VGA Screen in the end

Curriculum Project, Digital Integrated Circuit Project, HUST **Wuhan, China**
12/2018—01/2019
Project: Voltage Signal Spectrum Analyzer using Radix-4 FFT **Advisor:** Prof. Zhaoxia Zheng

- ✧ Completed the Radix-4 FFT module in Verilog and simulation work with Modelsim and verified its performance by Matlab
- ✧ Transplanted the module to the FPGA MicroBlaze SoC platform and finished the AXI-Lite interconnection
- ✧ Completed the FPGA implementation and functional test of the spectrum analyzer and verified that the computation efficiency of the FFT module was comparable to that of Vivado FFT Logic Core
- ✧ Source Code: https://github.com/hxfycy/1024-point-fft

1st prize, TI Cup National Undergraduate Electronics Design Contest in Hubei Province **Wuhan, China**
Team Leader 07/2018
Project: Current Signal Detection Device

- ✧ Built Peripheral Filter circuit on PCB and respectively finished SoC design on FPGA board to drive ADC, LCD Screen
- ✧ Conducted overall debugging after functional simulation of each module, identifying the spectral leakage problem deteriorated FFT module's frequency measurement accuracy
- ✧ Modified FFT module by Window function to obtain better measurement accuracy with higher frequency and amplitude
- ✧ Wrote final report and refined LCD module and GUI(Graphical User Interface), improved PCB connections for increasing stability

Extra-curricular activities

Debate Team, School of Optical and Electronic Information, HUST **Wuhan, China**
Leader 08/2017—07/2018

- ✧ Responsible for recruiting, debate training, and organizing team members to participate in various debate competitions
- ✧ Led the team to win the second place in the Freshman Cup debate competition, and Top 8 in the Well-known-Peak debate competition in the college

Language & Professional Skills

- ✧ TOEFL (08/24/2019): Total: 107 (R:29 L:27 S:25 W:26)
- ✧ GRE (10/21/2018): Total: 324 (V: 154>65% Q: 170>96% R:3.5>41%)
- ✧ Programming: C, C++, Python, Verilog, System Verilog, Verilog-A, Assembly
- ✧ Software: Vivado, Matlab, Cadence, Latex, Quartus, Altium Designer,