工作表1

Address	RegName	Signal	BitPos	Default
0x0	UART_FIFO		[31:8]	24'h0
		rxfifo_rd_byte	[7:0]	8'b0
0x4	UART_INT_RAW	UART_INT_RAW		
		rxfifo_tout_int_raw	[8]	1'b0
		brk_det_int_raw	[7]	1'b0
		cts_chg_int_raw	[6]	1'b0
		dsr_chg_int_raw	[5]	1'b0
		rxfifo_ovf_int_raw	[4]	1'b0
		frm_err_int_raw	[3]	1'b0
		parity_err_int_raw	[2]	1'b0
		txfifo_empty_int_raw	[1]	1'b0
		rxfifo_full_int_raw	[0]	1'b0
0x8	UART_INT_ST	UART_INT_ST		
		rxfifo_tout_int_st	[8]	1'b0
		brk_det_int_st	[7]	1'b0
		cts_chg_int_st	[6]	1'b0
		dsr_chg_int_st	[5]	1'b0
		rxfifo_ovf_int_st	[4]	1'b0
		frm_err_int_st	[3]	1'b0
		parity_err_int_st	[2]	1'b0
		txfifo_empty_int_st	[1]	1'b0
		rxfifo_full_int_st	[0]	1'b0
0xC	UART_INT_ENA	UART_INT_ENA		
		rxfifo_tout_int_ena	[8]	1'b0
		brk_det_int_ena	[7]	1'b0
		cts_chg_int_ena	[6]	1'b0
		dsr_chg_int_ena	[5]	1'b0
		rxfifo_ovf_int_ena	[4]	1'b0
		frm_err_int_ena	[3]	1'b0
		parity_err_int_ena	[2]	1'b0
		txfifo_empty_int_ena	[1]	1'b0
		rxfifo_full_int_ena	[0]	1'b0
0x10	UART_INT_CLR	UART_INT_CLR		
		rxfifo_tout_int_clr	[8]	1'b0
		brk_det_int_clr	[7]	1'b0
		cts_chg_int_clr	[6]	1'b0
		dsr_chg_int_clr	[5]	1'b0
		rxfifo_ovf_int_clr	[4]	1'b0
		frm_err_int_clr	[3]	1'b0
		parity_err_int_clr	[2]	1'b0
		txfifo_empty_int_clr	[1]	1'b0
		rxfifo_full_int_clr	[0]	1'b0

工作表1

0x14	UART_CLKDIV	UART_CLKDIV		
		uart_clkdiv	[19:0]	20'h2B6
0x18	UART_AUTOBAUD	UART_AUTOBAUD		
		glitch_filt	[15:8]	8'h10
			[7:1]	7'h0
		autobaud_en	[0]	1'b0
UART_STATU	UART_STATUS	UART_STATUS		
		txd	[31]	8'h0
		rtsn	[30]	1'b0
		dtrn	[29]	1'b0
			[28:14]	5'b0
		txfifo_cnt	[23:16]	8'b0
		rxd	[15]	1'b0
		ctsn	[14]	1'b0
		dsrn	[13]	1'b0
			[12:8]	5'b0
		rxfifo_cnt	[7:0]	8'b0
0x20	UART_CONF0	UART_CONF0		
		uart_dtr_inv	[24]	1'h0
		uart_rts_inv	[23]	1'h0
		uart_txd_inv	[22]	1'h0
		uart_dsr_inv	[21]	1'h0
		uart_cts_inv	[20]	1'h0
		uart_rxd_inv	[19]	1'h0
		txfifo_rst	[18]	1'h0
		rxfifo_rst	[17]	1'h0
		tx_flow_en	[15]	1'b0
		uart_loopback	[14]	1'b0
		txd_brk	[8]	1'b0
		sw_dtr	[7]	1'b0
		sw_rts	[6]	1'b0
		stop_bit_num	[5:4]	2'd1
		bit_num	[3:2]	2'd3
		parity_en	[1]	1'b0
		parity	[0]	1'b0
		UART_CONF1		
0x24	UART_CONF1	rx_tout_en	[31]	1'b0
		rx_tout_thrhd	[30:24]	7'b0
		rx_flow_en	[23]	1'b0
		rx_flow_thrhd	[22:16]	7'h0
			[15]	1'b0
		txfifo_empty_thrhd	[14:8]	7'h60

工作表1

			[7]	1'b0
		rxfifo_full_thrhd	[6:0]	7'h60
0x28	UART_LOWPULSE	UART_LOWPULSE		
		lowpulse_min_cnt	[19:0]	20'hFFFFF
0x2C	UART_HIGHPULSE	UART_HIGHPULSE		
		highpulse_min_cnt	[19:0]	20'hFFFFF
0x30	UART_RXD_CNT			
		rxd_edge_cnt	[9:0]	10'h0
0x78	UART_DATE	uart_date	[31:0]	32'h062000
0x7C	UART_ID	uart_id	[31:0]	32'h0500

SW(R/W)
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
RO
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RO
R/W
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R/W
R/W
R/W
RO
R/W

RO
R/W
RO
RO
RO
R/W
R/W

工作表1

Description
UART FIFO,length 128
R/W share the same address
UART INTERRUPT RAW STATE
The interrupt raw bit for Rx time-out interrupt(depands on the UART_RX_TOUT_THRHD)
The interrupt raw bit for Rx byte start error
The interrupt raw bit for CTS changing level
The interrupt raw bit for DSR changing level
The interrupt raw bit for rx fifo overflow
The interrupt raw bit for other rx error
The interrupt raw bit for parity check error
The interrupt raw bit for tx fifo empty interrupt(depands on UART_TXFIFO_EMPTY_THRHD bits)
The interrupt raw bit for rx fifo full interrupt(depands on UART_RXFIFO_FULL_THRHD bits)
UART INTERRUPT STATE REGISTER（UART_INT_RAW&UART_INT_ENA）
The interrupt state bit for Rx time-out event
The interrupt state bit for rx byte start error
The interrupt state bit for CTS changing level
The interrupt state bit for DSR changing level
The interrupt state bit for RX fifo overflow
The interrupt state for other rx error
The interrupt state bit for rx parity error
The interrupt state bit for TX fifo empty
The interrupt state bit for RX fifo full event
UART INTERRUPT ENABLE REGISTER
The interrupt enable bit for rx time-out interrupt
The interrupt enable bit for rx byte start error
The interrupt enable bit for CTS changing level
The interrupt enable bit for DSR changing level
The interrupt enable bit for rx fifo overflow
The interrupt enable bit for other rx error
The interrupt enable bit for parity error
The interrupt enable bit for tx fifo empty event
The interrupt enable bit for rx fifo full event
UART INTERRUPT CLEAR REGISTER
Set this bit to clear the rx time-out interrupt
Set this bit to clear the rx byte start interrupt
Set this bit to clear the CTS changing interrupt
Set this bit to clear the DSR changing interrupt
Set this bit to clear the rx fifo over-flow interrupt
Set this bit to clear other rx error interrupt
Set this bit to clear the parity error interrupt
Set this bit to clear the tx fifo empty interrupt
Set this bit to clear the rx fifo full interrupt

工作表1

UART CLK DIV REGISTER
BAUDRATE = UART_CLK_FREQ / UART_CLKDIV
UART BAUDRATE DETECT REGISTER
Set this bit to enable baudrate detect
UART STATUS REGISTER
The level of the uart txd pin
The level of uart rts pin
The level of uart dtr pin
Number of data in UART TX fifo
The level of uart rxd pin
The level of uart cts pin
The level of uart dsr pin
Number of data in uart rx fifo
UART CONFIG0(UART0 and UART1)
Set this bit to inverse uart dtr level
Set this bit to inverse uart rts level
Set this bit to inverse uart txd level
Set this bit to inverse uart dsr level
Set this bit to inverse uart cts level
Set this bit to inverse uart rxd level
Set this bit to reset uart tx fifo
Set this bit to reset uart rx fifo
Set this bit to enable uart tx hardware flow control
Set this bit to enable uart loopback test mode
RESERVED, DO NOT CHANGE THIS BIT
sw dtr
sw rts
Set stop bit: 1:1bit 2:1.5bits 3:2bits
Set bit num: 0:5bits 1:6bits 2:7bits 3:8bits
Set this bit to enable uart parity check
Set parity check: 0:even 1:odd
UART CONFIG1
Set this bit to enable rx time-out function
Config bits for rx time-out threshold,uint: byte,0-127
Set this bit to enable rx hardware flow control
The config bits for rx flow control threshold,0-127
The config bits for tx fifo empty threshold,0-127

The config bits for rx fifo full threshold,0-127
used in baudrate detect
used in baudrate detect
used in baudrate detect
UART HW INFO