工作表1

Address	RegName	Signal	BitPos	Default	SW(R/W)
0x0	FRC1_LOAD_ADDRESS	frc1_load_value	[22:0]	23'b0	R/W
0x4	FRC1_COUNT_ADDRESS	frc1_count	[22:0]	23'h7fffff	RO
0x8	FRC1_CTRL_ADDRESS		[31:9]	23'b0	RO
		frc1_int	[8]	1'b0	RO
		frc1_ctrl	[7:0]	8'b0	R/W
0xC	FRC1_INT_ADDRESS		[31:1]	30'b0	RO
		frc1_int_clr_mask	[0]	1'b0	R/W
0x20	FRC2_LOAD_ADDRESS	frc2_load_value	[31:0]	32'b0	R/W
0x24	FRC2_COUNT_ADDRESS	frc2_count	[31:0]	32'b1	RO
0x28	FRC2_CTRL_ADDRESS		[31:9]	23'b0	RO
		frc2_int	[8]	1'b0	RO
		frc2_ctrl	[7:0]	8'b0	R/W
0x2C	FRC2_INT_ADDRESS		[31:1]	30'b0	RO
		frc2_int_clr_mask	[0]	1'b0	R/W
0x30	FRC2_ALARM_ADDRESS	frc2_alarm	[31:0]	32'b0	R/W

工作表1

Description
the load value into the counter
the current value of the counter. It is a decreasing counter.
the status of the interrupt, when the count is dereased to zero
bit[7]: timer enable
bit[6]: automatically reload, when the counter is equal to zero
bit[3:2]: prescale-divider, 0: divided by 1, 1: divided by 16, 2 or 3: divided by 256
bit[0]: interrupt type, 0:edge, 1:level
write to clear the status of the interrupt, if the interrupt type is "level"
the load value into the counter
the current value of the counter. It is a increasing counter.
the status of the interrupt, when the count is equal to the alarm value
bit[7]: timer enable
bit[6]: automatically reload, when the counter is equal to zero
bit[3:2]: prescale-divider, 0: divided by 1, 1: divided by 16, 2 or 3: divided by 256
bit[0]: interrupt type, 0:edge, 1:level
write to clear the status of the interrupt, if the interrupt type is "level"
the alarm value for the counter