

A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter

Tzu-Fan Wu, Cheng-Ru Ho, and Mike Shuo-Wei Chen

Abstract—This paper introduces different classes of analog-to-digital converter (ADC) architecture that non-uniformly samples the analog input and shifts from conventional voltage quantization to a hybrid quantization paradigm wherein both voltage and time quantization are utilized. In this architecture, the sampling rate adapts to the input frequency, which maintains an alias-free spectrum and enables an anti-aliasing (AA) filtering in the digital domain to relax the analog AA filter. In addition, the digital AA filter can generate uniform outputs from non-uniform samples to interact with the synchronous digital signal processor seamlessly and benefit from reconfigurability and technology scaling. To prove the concept, a flash-based non-uniform sampling ADC is proposed and the circuit non-idealities of key building blocks are analyzed. A silicon prototype is implemented in a 65-nm CMOS, which utilizes a 15-level voltage quantizer and a shared time quantizer with maximum resolution of 9 ps. Combined with the digital AA filter it improves SNR by 30 dB in comparison with a conventional 4-bit uniformly sampled Nyquist-rate ADC and measures an EVM of -28 dB for a 64 quadrature amplitude modulation input signal under a 30-dB higher blocker.

Index Terms—Alias free, analog-to-digital converter (ADC), anti-aliasing (AA) filter, asynchronous processing, event driven, level-crossing sampling (LCS), non-uniform sampling (NUS), offset calibration, time-to-digital converter (TDC).

I. INTRODUCTION

TRADITIONALLY, analog-to-digital converters (ADCs) sample an analog signal at a fixed clock frequency, which is shown as f_s in Fig. 1(a). An inevitable consequence of the uniform time grid of the sampling instants is “spectral aliasing.” This means that any frequency component higher than the Nyquist frequency will be folded back into the first Nyquist zone. Therefore, in the wireless communication with multi-standard and multi-band operations [1]–[3], tunable analog filters or switched filter banks are needed to provide sufficient anti-aliasing (AA) filtering prior to a uniformly sampled Nyquist-rate ADC to attenuate unwanted out-of-band signals. Another type of sampling scheme is non-uniform sampling (NUS) [4], [5]; one way to achieve NUS is level-crossing

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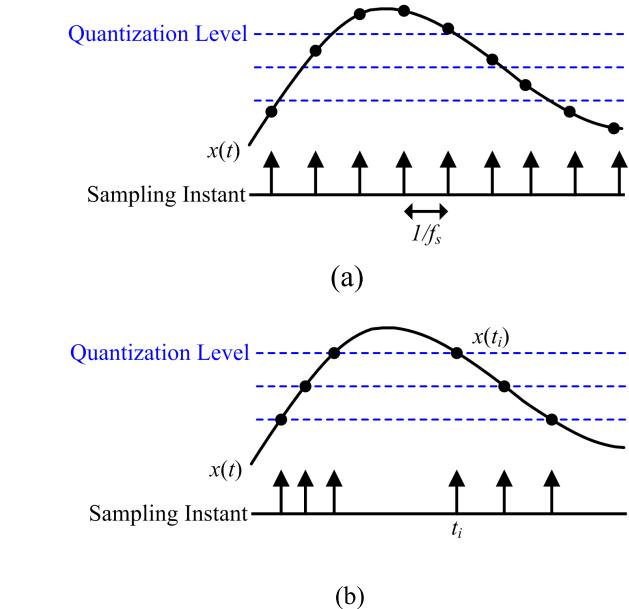


Fig. 1. (a) Uniform sampling. (b) NUS.

sampling (LCS) [4]–[15]. There are unique properties of this sampling scheme. First, instead of a fixed-period sampling clock, the sampling rate is signal dependent and adapts to the signal frequency achieving an alias-free sampling. Second, because of the LCS, there is no voltage quantization error at the level-crossing points, unlike the conventional uniformly sampled ADCs. It can potentially achieve an error-free signal reconstruction as long as the average sampling rate meets the Nyquist rate of the input signal [4], [16]. Third, a new sample is generated only when the analog input crosses a certain quantization level, as shown in Fig. 1(b). It is completely event-driven, making the sampling more efficient, especially in applications such as ultra-wideband impulse radio [17], [18], sensor networks [19], and biomedical electronics [20] where signals are often sparse in time.

In this paper, we explore this unique alias-free sampling property and propose an ADC architecture that shifts from conventional voltage quantization to a hybrid quantization paradigm wherein both voltage quantization and time quantization are utilized. Through this hybrid quantization, the outputs can work with the digital AA filter [21], [22] to preserve the unique properties of LCS quantization throughout the entire signal path achieving an signal-to-quantization-noise ratio (SQNR) much greater than $6.02 NvQ + 1.76$, where NvQ is the number

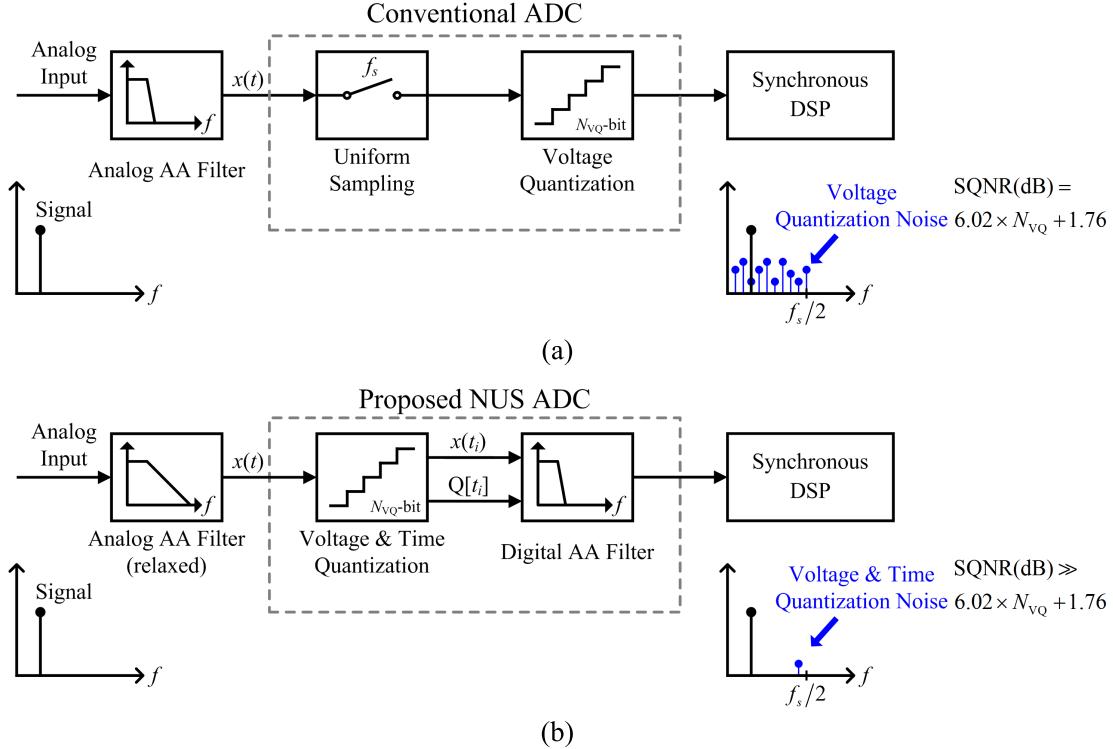


Fig. 2. (a) Conventional ADC architecture. (b) Proposed NUS ADC architecture.

of bits in the voltage quantizer. Since the digital AA filter can also attenuate unwanted out-of-band signals, the burden of AA filtering can be moved from the analog to the digital domain, which benefits from technology scaling and leads to a highly flexible system as the computation can be easily reconfigured. To prove the concept, an NUS ADC prototype with a 15-level voltage quantizer and a 9-ps time quantizer is implemented in 65-nm CMOS. The remainder of this paper is organized as follows. Section II discusses the proposed NUS ADC architecture, and Section III provides the circuit non-ideality analysis. The digital AA filter is described in Section IV, and implementation details of several key building blocks are elaborated in Section V. Measurements of the porotype are presented in Section VI.

II. PROPOSED NON-UNIFORM SAMPLING ADC

A conventional uniform sampling Nyquist-rate ADC architecture is shown in Fig. 2(a). An analog AA filter is typically required before the uniform sampling to attenuate any unwanted out-of-band signal. In addition, the voltage quantization noise will be folded without any filtering, resulting in the well-known quantization noise power, $\text{LSB}^2/12$. In this paper, the proposed NUS ADC architecture swaps the sequence of conventional ADC blocks, as shown in Fig. 2(b). The voltage quantizer is moved to the very first block, and the time information of the sampling instants is subsequently quantized and recorded, where $Q[\cdot]$ represents the time quantization process. Both voltage and time information are utilized in the digital AA filter, which essentially performs a true analog filtering but in the digital domain. Therefore, it can relax the

analog AA filter, which will be discussed in Section IV-B. The voltage quantization noise in Fig. 2(b) represents the interpolation error from a practical signal reconstruction method, e.g., zero-order hold (ZOH), in the digital AA filter, and there is a tradeoff between the complexity of the reconstruction method and the number of levels in the voltage quantizer. The time quantization noise, which results from the finite time resolution, can cause an aliasing effect on the voltage quantization noise and introduce time skews being converted to additive voltage errors after signal reconstruction. However, the technology scaling generally can improve the time accuracy. More discussions on the quantization noise can be found in [6] and [21]–[23]. Finally, the digital AA filter will output uniform samples that can interact with existing synchronous digital signal processors (DSPs) seamlessly. Therefore, on the top level, the proposed ADC architecture appears as a uniformly sampled ADC even though it is internally processed in a non-uniform domain.

III. CIRCUIT NON-IDEALITY MODELING

The circuit non-ideality modeling of quantizers in the proposed NUS ADC is shown in Fig. 3. For the voltage quantizer, which is composed of multiple multi-stage continuous-time comparators connected to different threshold voltages, the propagation delay variation [23]–[26] is derived as a function of input slope at the level crossing and various circuit parameters. Ideally, the voltage and time quantizers should generate $V_{in}(t_i)$ and $Q[t_i]$, respectively, where t_i is the ideal level-crossing time instant. However, a signal-dependent propagation delay (t_d) is added to t_i and can cause harmonics,

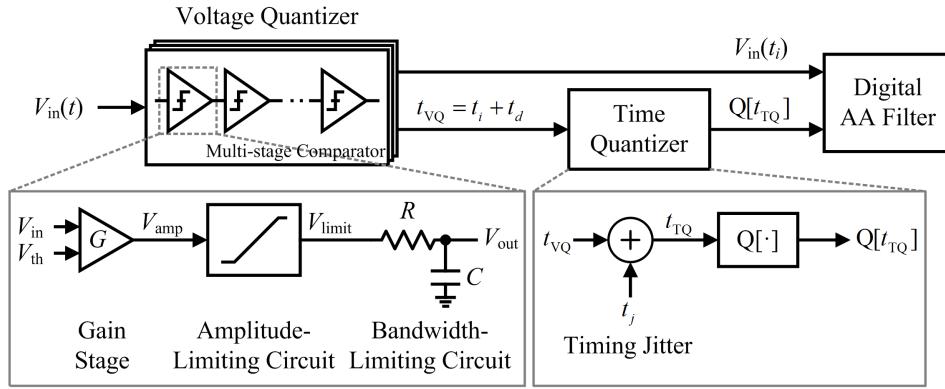


Fig. 3. Model of non-idealities in the NUS ADC front end.

particularly in the LCS [23]. Additionally, the impact of comparator offset is analyzed, which can also lead to distortions in the reconstructed signal. For the time quantizer, SNR degradation due to jitter (t_j) of the time quantizer is considered, which is added to the time instant at the voltage quantizer output (t_{VQ}). Finally, the analysis can also be extended to model the noise impact from the voltage quantizer.

A. Comparator Propagation Delay Variation

Considering a full-scale single sinusoidal input $A_{FS} \cdot \sin\omega_{in}t$, the maximum delay variation can be calculated at the middle and topmost quantization levels with the maximum and minimum input slopes, respectively. The comparator model presented in [24] is used for delay variation analysis, as shown in Fig. 3. The sinusoidal input is approximated to a ramp with slope S_{in} , which is the input slope at the threshold voltage (V_{th}). The voltage difference between the input and threshold voltage $V_{in,diff} = (V_{in} - V_{th})$ as shown in Fig. 4 is first amplified, that is, $V_{amp} = GV_{in,diff}$, and then passed to an amplitude-limiting circuit with output swing from $-A_{max}$ to A_{max} . The last stage is a bandwidth-limiting circuit with time constant $RC = 1/2\pi f_{comp}$, where f_{comp} is the comparator bandwidth. Assuming $A_{FS} = A_{max}$ for simplicity, the propagation delay of a single comparator from V_{in} to V_{out} can be obtained by using Laplace transforms on a ramp signal applied to the RC network. As shown in the time-domain waveform in Fig. 4, t_2 is the time at which V_{limit} reaches A_{max} , and t_3 is the time at which V_{out} reaches zero. Therefore, the propagation delay is defined as the difference between the input and output zero-crossing time instants, i.e., $t_3 - t_1$. They can be derived for the following two cases:

$$t_d = \frac{-1}{2\pi f_{comp}} \left[\ln \frac{A_{max} 2\pi f_{comp}}{GS_{in}} + \frac{A_{max} 2\pi f_{comp}}{GS_{in}} - \ln \left(e^{2 \frac{A_{max} 2\pi f_{comp}}{GS_{in}}} - 1 \right) \right] \text{ for } t_3 \geq t_2 \quad (1)$$

$$t_d = \frac{1}{2\pi f_{comp}} \left[1 - e^{-2\pi f_{comp} \left(\frac{A_{max}}{GS_{in}} + t_d \right)} \right] \text{ for } t_3 < t_2. \quad (2)$$

In this paper, the comparator is designed in multi-stage topology to achieve a wide bandwidth and high gain with lower cost [27]. The total propagation delay of a K -stage comparator

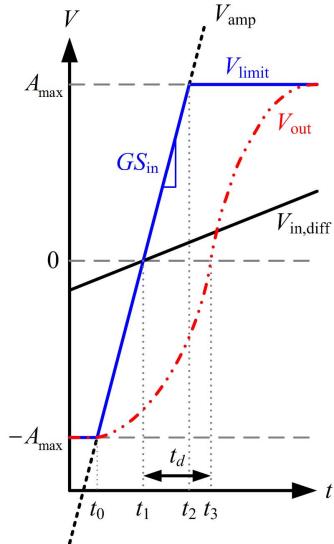


Fig. 4. Time-domain waveform within the comparator model using a ramp input.

can be calculated as $t_{d,tot} = \sum_{i=1}^K t_{d,i}$, where $t_{d,i}$ is the single-stage propagation delay of the i th stage. $t_{d,i}$ can be obtained from either (1) or (2) by replacing f_{comp} with the bandwidth of the i th stage ($f_{comp,i}$) and keeping S_{in} as the input slope at the first stage but replacing G with the accumulated gain, $G_{acc,i} = \prod_{m=1}^i G_m$, where G_m is the m th-stage gain.

In this prototype, multiple comparators connected to different threshold voltages are utilized, and their outputs will eventually be converted to single ended. The triggering threshold mismatch of the following single-ended stage between different comparators can introduce an extra delay variation. According to the Monte Carlo analysis, an overall gain of >45 dB is needed to ensure a sufficiently sharp single-ended transition edge to keep the extra delay variation negligible compared to the delay variation generated from the comparator. Considering a four-stage comparator where the overall gain is evenly distributed on each stage with the same bandwidth, Fig. 5 shows the delay variation and degradation on distortions over different bandwidths for a 15-level voltage quantizer with an input of 20-MHz full-scale single tone or two equal amplitude tones located at ~ 20 MHz with 1-MHz spacing. Presenting multiple frequencies at the input can generate a

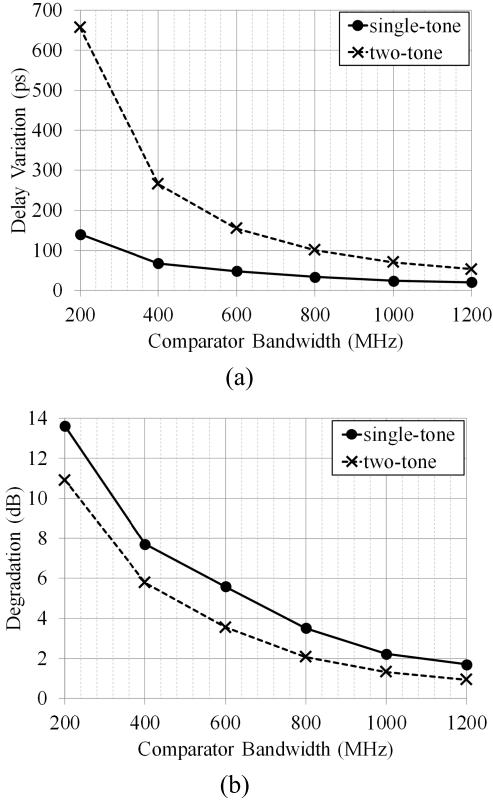


Fig. 5. (a) Delay variation and (b) degradation on distortions of various f_{comp} , where spline interpolation is applied as a reference reconstruction algorithm.

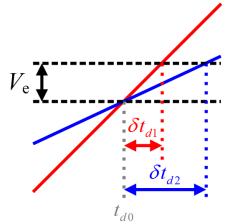


Fig. 6. Voltage error introduced by the delay variation with different input slopes.

larger delay variation because of the wider range of the input slope, but a smaller input slope at level crossing can tolerate more delay variation. It can be illustrated in Fig. 6, where δt_{d1} and δt_{d2} represent the delay deviation from a nominal delay value (t_{d0}). This delay variation effect can be approximated as an error voltage via the product of the input slope and the time deviation. Therefore, given a certain error voltage bound (V_e), it can be observed that more delay variation ($\delta t_{d2} > \delta t_{d1}$) can be tolerated when the input slope at the level-crossing point is smaller. Based on the above analyses, a four-stage comparator is designed in this prototype, where each stage has more than 12-dB gain and 1-GHz bandwidth to keep the degradation on distortions less than 3 dB.

B. Offset of Comparator and Reference Voltage

Since the offset voltage (V_{off}) of the comparator and the reference voltage generator changes the threshold of the corresponding voltage quantization level, it effectively causes a timing error (δt_{off}) for the level-crossing time instant.

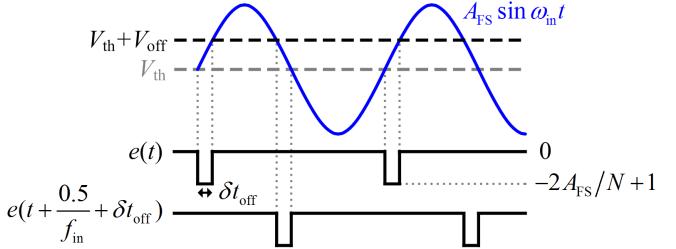


Fig. 7. Errors introduced by the offset voltage in the voltage quantizer.

Assuming an offset occurs only at the center level, δt_{off} can be approximated as $V_{\text{off}}/A_{\text{FS}}\omega_{\text{in}}$ for a sinusoidal input ($A_{\text{FS}} \cdot \sin \omega_{\text{in}} t$). Considering the reconstruction method of ZOH, this δt_{off} -induced error [$e_{\text{off}}(t)$] is modeled as a superposition of two pulse trains $e(t)$ and $e(t + 0.5/f_{\text{in}} + \delta t_{\text{off}})$, where $e(t)$ is a square wave with period of $1/f_{\text{in}}$ as shown in Fig. 7. Since $e_{\text{off}}(t)$ is repetitive, it can be expressed via Fourier series expansion

$$e_{\text{off}}(t) = \frac{-2V_{\text{off}}}{\pi(N+1)} - \frac{4A_{\text{FS}}}{\pi(N+1)} \sum_{k=1}^{\infty} \frac{1}{k} \sin\left(\frac{kV_{\text{off}}}{2A_{\text{FS}}}\right) \times [\cos(k\omega_{\text{in}}t) + (-1)^k \cos(k\omega_{\text{in}}(t + \delta t_{\text{off}}))] \quad (3)$$

where N is the number of levels in the voltage quantizer. It can be observed that V_{off} introduces harmonic distortions. The above derivation can be extended to multiple threshold voltages with offset, and the errors can be combined by superposition. Based on the analysis, the maximum offset voltage should be less than 1.3 mV to achieve spurious-free dynamic range (SFDR) higher than 65 dB, which is accomplished by an offset calibration scheme elaborated in Section V-C.

C. Noise in Time Quantizer and Voltage Quantizer

The noise of a time quantizer can be modeled as timing jitter [28]. To calculate the effect of timing jitter [$t_j \sim N(0, \sigma_{tj})$], t_j is multiplied by the input slope at the level-crossing point, that is, the induced voltage error, similar to jitter analysis on sampling clocks in conventional ADCs [29]. However, the varying sampling rate in the NUS ADC spreads the noise spectrum from dc to half of the average sampling rate. Considering a sinusoidal input of $A \cdot \sin \omega_{\text{in}} t$, the average sampling rate ($f_{s,\text{avg}}$) is $p \cdot f_{\text{in}}$, where p is the number of non-uniform samples generated each cycle and proportional to A . The average oversampling ratio (OSR_{avg}) can be represented as $f_{s,\text{avg}}/2f_{\text{BW}}$, where f_{BW} is the desired bandwidth. Assuming the noise spectrum is white with a digital AA filter applied to attenuate out-of-band noise higher than f_{BW} , there is an additional processing gain $G_{\text{DAAF}} = \max(\text{OSR}_{\text{avg}}, 1) = \max(p \cdot f_{\text{in}}/2f_{\text{BW}}, 1)$. Therefore, the SNR over f_{BW} can be derived as

$$\text{SNR}_{\text{jitter}} = 10 \log_{10} \frac{\frac{1}{2} A^2 \cdot G_{\text{DAAF}}}{\frac{1}{p} \sum_{k=0}^{p-1} (\sigma_{tj}^2 S_k^2)} \text{ for } A > \frac{2A_{\text{FS}}}{N+1} \quad (4)$$

where S_k is the input slope at the k th non-uniform sample. Since an automatic gain control loop is typically applied to the system, $A > 2A_{\text{FS}}/(N+1)$ is always satisfied. Considering a 15-level voltage quantizer with 20-MHz input,

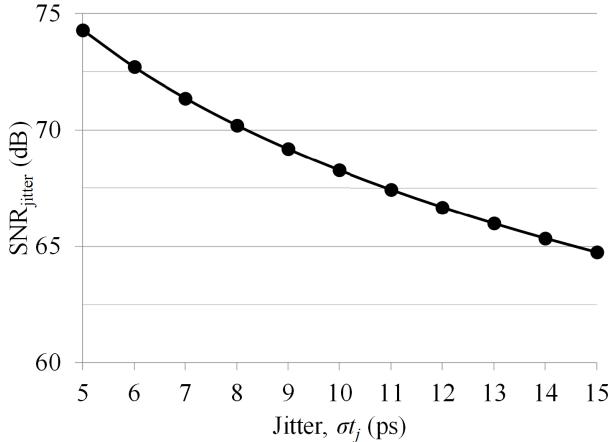


Fig. 8. SNR of a 20-MHz sinusoidal input over different jitter values.

the SNR_{jitter} over 20-MHz bandwidth is plotted over different jitter values with a full-scale input (Fig. 8). Practically, if the noise spectrum is not white, the analysis can be extended for a colored noise spectrum by reducing the G_{DAAF} factor in (4). Similarly, this analysis can be applied to the noise impact from the voltage quantizer by replacing the denominator in (4) with an equivalent input-referred noise power

$$\text{SNR}_{\text{VQ}} = 10 \log_{10} \frac{\frac{1}{2} A^2 \cdot G_{\text{DAAF}}}{V_{n,\text{VQ}}^2}. \quad (5)$$

With a 20-MHz input and 20-MHz bandwidth, an overall SNR of 65 dB can be achieved by 700 μV_{RMS} input-referred noise of the voltage quantizer and 9-ps jitter of the time quantizer.

IV. DIGITAL ANTI-ALIASING FILTER

A. Concept and Implementation

One unique property of the NUS ADC is the incorporation of an AA filter in the digital domain, which is proposed in [22]. The structure of the digital AA filter is similar to the conventional digital finite-impulse response (FIR) filter, except the tap delays and filter coefficients dynamically change in real time as a function of the input signal. It not only preserves the alias-free property of NUS but also achieves a true analog filter response, with no spectral replicas repeating every sampling frequency or 2π as in conventional FIR filters. Therefore, it can attenuate unwanted out-of-band signals prior to the final uniform sampler and alleviate in-band SNR degradation.

The derivation of the proposed digital AA filter algorithm originates from performing convolution between the input signal $x(t)$ and a continuous-time filter impulse response $h(t)$. To reconstruct $x(t)$ from quantized non-uniform samples $x(t_i)$ and $Q[t_i]$, the ZOH can be applied as an example. In Fig. 9, the variable delay τ_i represents the varying time interval between non-uniform samples $Q[t_{i+1}] - Q[t_i]$, and t_s is the uniform resampling period. Therefore, the resampled and filtered output can be written as

$$s[k] = \sum_{i=0}^{n-1} x(t_i) \cdot \underbrace{\int_{\Delta t_i}^{\Delta t_{i+1}} h(t) dt}_{c_i}, \quad k \in \mathbb{Z} \quad (6)$$

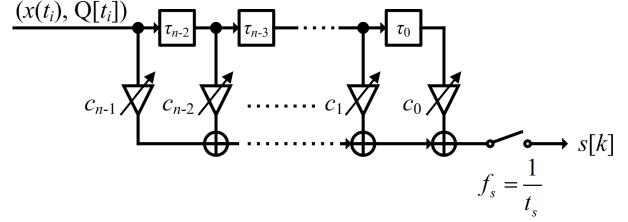


Fig. 9. Digital AA filter with dynamic changing delays and coefficients.

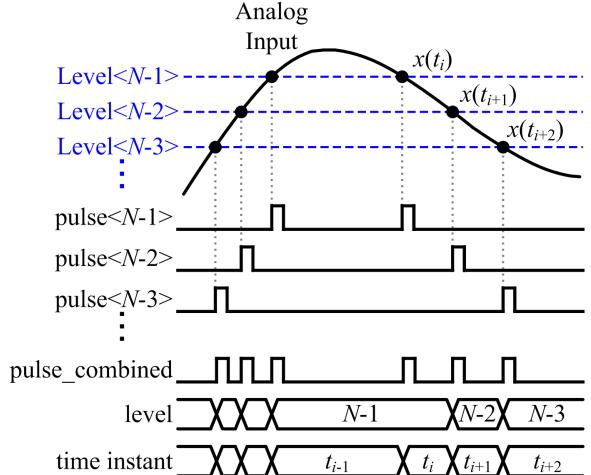


Fig. 10. Concept of generating and processing level-crossing events.

where $\Delta t_i = Q[t_i] - kt_s$ and n is the number of non-uniform samples within the finite length of the filter duration, i.e., the length of the impulse response, centered on each resampling instant. The filter duration can be pre-defined by the desired filter frequency response and is fully reconfigurable. Although the concept is convolving two continuous-time terms $x(t)$ and $h(t)$, only discrete-time output $s[k]$ is computed at the resampling rate (f_s), and the filter coefficient (c_i) is calculated according to τ_i and updated in real time.

Considering the implementation, an asynchronous first-in-first-out (FIFO) buffer can be used to store the incoming non-uniform samples and deserialize them to parallel outputs at f_s . The maximum possible n in (6) can be determined according to the specific filter duration, and defines the required FIFO depth. Since n at each resampling instant is proportional to the signal activities, the computation and power consumption are fully adaptive and signal dependent, which are different from the conventional digital FIR filter. In addition, the filter coefficient can be pre-calculated and stored in lookup tables as a function of τ_i to reduce the real-time computation.

To estimate its complexity, a representative digital AA filter with $n \leq 32$ is coded in RTL using 16-bit fixed-point representation and synthesized with 65-nm CMOS digital standard cell library. Considering the case that non-uniform samples are generated at a constant rate of 2 GS/s and converted into 200-MS/s uniform samples after filtering, the area and power consumption are estimated as $\sim 0.128 \text{ mm}^2$ and $\sim 10 \text{ mW}$ including 4-kB memory calculated using the memory density reported in [30]. Note that as the non-uniform sample rate is dependent on the input activities, the power consumption in the digital AA filter will scale proportionally in real time. For

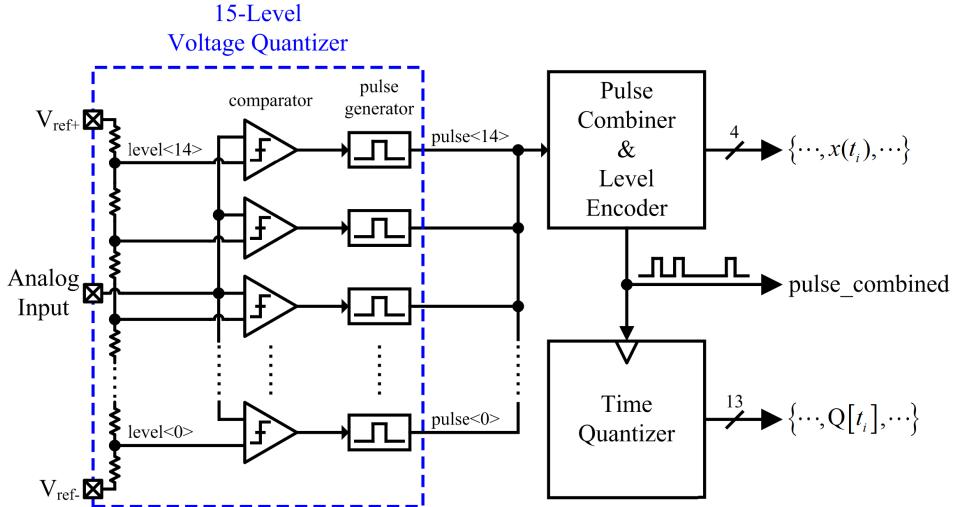


Fig. 11. Block diagram of the proposed flash-based NUS ADC.

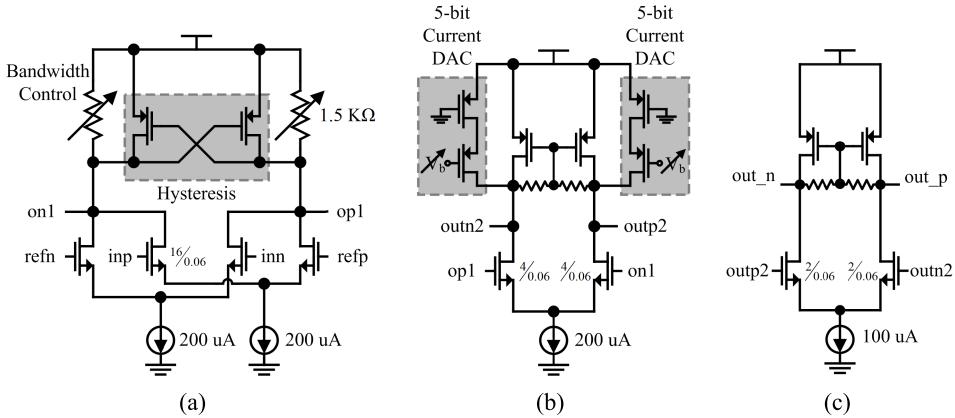


Fig. 12. Comparator implementation. (a) First stage. (b) Second stage with offset calibration. (c) Third and fourth stages.

example, if the input is a 64-quadrature amplitude modulation (QAM) signal with 100-MHz bandwidth, the digital AA filter consumes an average of 3.8 mW with more than fourth-order equivalent analog filtering. In the extreme case where there is no non-uniform sample, the digital AA filter consumes only the leakage current without any dynamic power.

B. Relaxed Analog Anti-Aliasing Filter Requirements

In addition to the reconfigurability and benefit from technology scaling, the possibility of using a digital AA filter relaxes of the analog AA filter requirements. For example, when a large out-of-band blocker is present near the pass band, a conventional Nyquist-rate ADC demands an analog AA filter to attenuate the blocker lower than the desired signal to maintain required SNR after uniform sampling, i.e., spectral aliasing. Additionally, the filtered signal is typically amplified by a programmable gain amplifier (PGA) to utilize the full dynamic range of the ADC, that is, to suppress the input-referred noise. In contrast, these requirements can be relaxed in NUS ADC architecture because of its alias-free sampling and digital AA filtering. For instance, considering a voltage quantizer has a full-scale input of 1 V and an input-referred thermal noise of 1 mVRMS, and the timing jitter is 1 ps; there is a 20-MHz bandwidth desired signal with a 50-dB higher

blocker at 80 MHz. A conventional Nyquist-rate ADC can achieve SNR of 40 dB but demands 90-dB attenuation on the blocker with 50-dB PGA gain. However, the NUS ADC with 15 levels requires only 20-dB attenuation on the blocker with 20-dB PGA gain to suppress the input-referred noise calculated from (4) and (5). This can yield a reduced cost on analog AA filters and PGAs.

V. CIRCUIT IMPLEMENTATION

A. Overall Implementation Architecture

Fig. 10 shows the high-level time-domain concept of the proposed ADC implementation. As mentioned in Section II, two essential elements of the input signal—level and time—are required for the signal processing in the digital AA filter. In the proposed ADC implementation, whenever an analog input signal crosses certain pre-defined quantization levels, it triggers a pulse to indicate an NUS event. Pulses from different levels are combined before being recorded by a shared time quantizer to minimize hardware complexity.

The simplified block diagram of the proposed flash-based NUS ADC front end is shown in Fig. 11. The voltage quantizer in the previous work [9] is composed of two comparators but keeps switching the reference voltage to track the input signal.

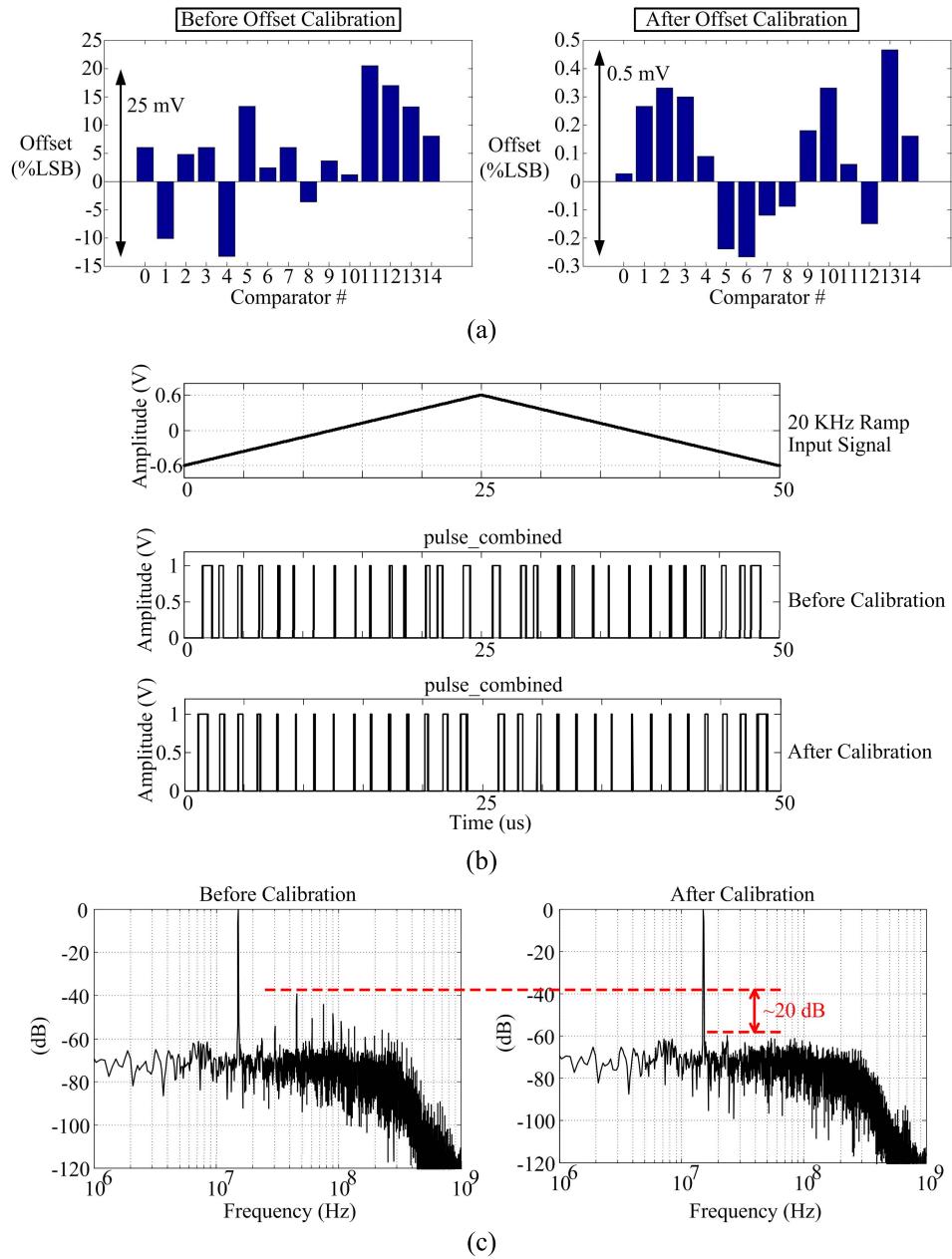


Fig. 13. Measured (a) comparator offset and (b) combined pulse using a 20-KHz ramp signal. (c) Measured reconstructed output spectrum using spline interpolation.

However, the settling time including the delay of the feedback loop must be shorter than the minimum time spacing between two adjacent sampling events and becomes a bottleneck for wider signal bandwidths. In order to maximize bandwidth, a parallel bank of comparators with fixed reference voltages is implemented. Assuming $t_{\text{diff},\min}$ is the minimum time spacing between two adjacent pulses at which the time quantizer can function properly, and N is the number of levels; the maximum input frequency ($f_{\text{in},\max}$) of a full-scale single tone can be determined by $f_{\text{in},\max} \leq 1/2\pi t_{\text{diff},\min} \sin^{-1}(2/N + 1)$. For $t_{\text{diff},\min} = 500$ ps and $N = 15$ in this prototype, it results in $f_{\text{in},\max}$ of 40 MHz. The outputs of comparators are followed by pulse generators to convert level-crossing events into non-uniform pulses. The pulse combiner then combines all pulses,

and the level encoder indicates which level is being crossed by the analog input. Finally, the combined pulse triggers the time quantizer and the time instant of each rising edge is recorded.

B. Reference Generator and Comparator

The reference generator and comparators are fully differential but are shown in single-ended configuration for simplicity. The reference generator consists of two matched poly-resistor ladders placed in parallel but opposite directions to minimize and balance the routings to comparators at the cost of doubling the power consumption. The positive and negative reference voltages are 1 and 0.4 V, respectively, resulting in maximum amplitude of 0.6 V for the differential input. The matching requirements are relaxed by the offset calibration as described

in Section V-C, and the peak mismatch between the two ladders is designed to be 0.5% based on the Monte Carlo simulation.

The four-stage comparator is shown in Fig. 12. Considering the level-crossing instant at the first stage, except the middle comparator where all inputs are at the same voltage, the differential output voltage can have a dependence on different operating conditions and result in a reference level-dependent delay variation in addition to the slope-dependent delay variation discussed in Section III-A. To minimize this effect, *inp* and *refp* are connected to one of the differential pairs, while *inn* and *refn* are connected to the other. That way, the differential input voltages of both differential pairs are zero upon level crossing, and operating at the most linear region of the transfer function. As a result, the comparator delay variation between different reference levels is minimized, which has been confirmed via SPICE simulations. Additionally, the gain of the first stage can attenuate the kick-back noise before being coupled to the reference generator, and hysteresis is applied to reduce unexpected multiple crossing events at the same reference level due to circuit noise. The offset calibration is performed at the outputs of the second stage by including 5-bit current-steering DACs at the positive and negative nodes. The third and fourth stages provide extra gain, sharpening the signal transition edge. According to the SPICE simulation, each stage achieves more than 1-GHz bandwidth, and the overall gain is around 45 dB with input-referred noise <600 μVRMS . To confine the delay variation within specifications, numerous SPICE simulations are performed over different process corners, supply voltages, and temperatures (PVT) with some tunability in the tail current, load resistors, and transistors.

C. Offset Calibration

The offset from both reference generator and comparators can be calibrated simultaneously by sending a known signal and calculating the difference between the measured time codes and the expected crossing-time instants. The measured time codes are averaged over multiple cycles to mitigate noise impact; then, a binary search can be applied to properly adjust the current DACs in comparators to compensate the offset. To minimize the delay variation due to different input slopes, a ramp can be applied during the calibration stage and its amplitude is overdriven to be greater than the full scale to reduce the effect of overdrive voltage in the comparator. After calibration, the offset voltage can be confined within 0.5 mV, resulting in more uniformly spaced pulses and a 20-dB improvement in SFDR (Fig. 13). The ADC can also be calibrated by a low-frequency sinusoid wave, for example, 1 MHz, which yields similar results as the delay variation is negligible. Although this calibration scheme is performed in the foreground, a Monte Carlo simulation shows the offset voltage due to temperature drift is 11 $\mu\text{V}/^\circ\text{C}$ after the initial calibration process, which is tolerable given the specification target. When a tighter offset control is required, the comparator can be re-calibrated whenever there is no signal-crossing event or an auxiliary comparator may be used to bring one of the comparators offline for calibration.

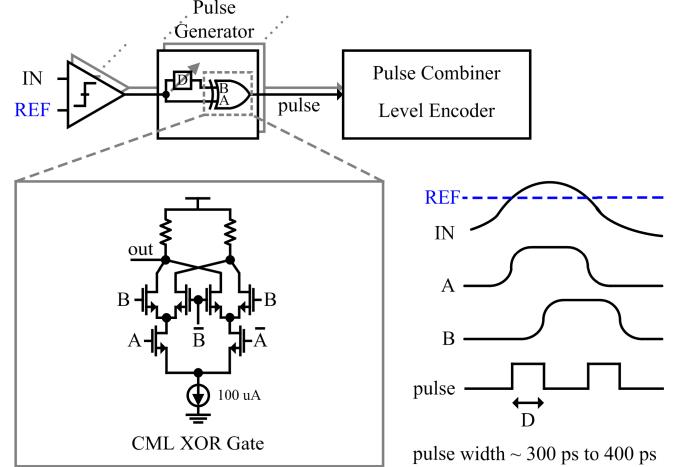


Fig. 14. Pulse generator with tunable pulse width.

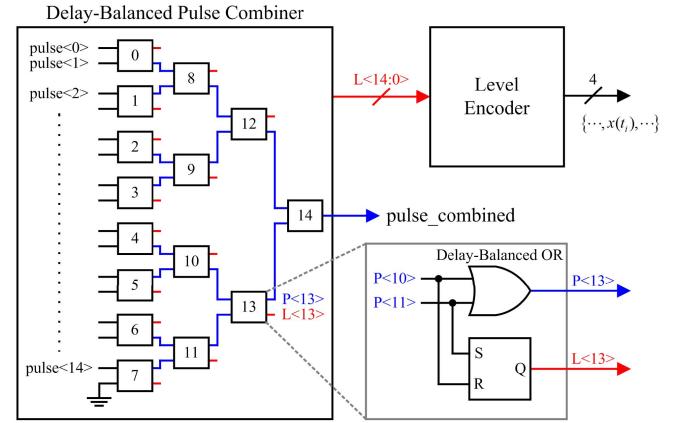


Fig. 15. Delay-balanced pulse combiner and level encoder.

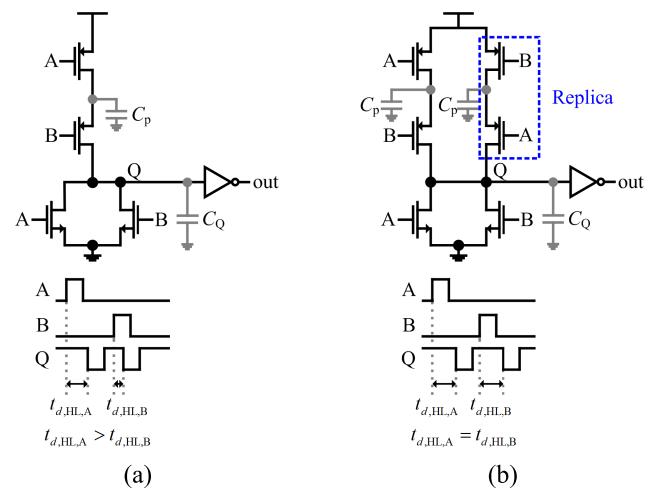


Fig. 16. (a) Conventional CMOS OR gate. (b) Delay-balanced OR gate.

D. Pulse Generator

The pulse generator shown in Fig. 14 contains an exclusive-OR gate and a delay cell, where differential current-mode logic (CML) is utilized to minimize the propagation delay

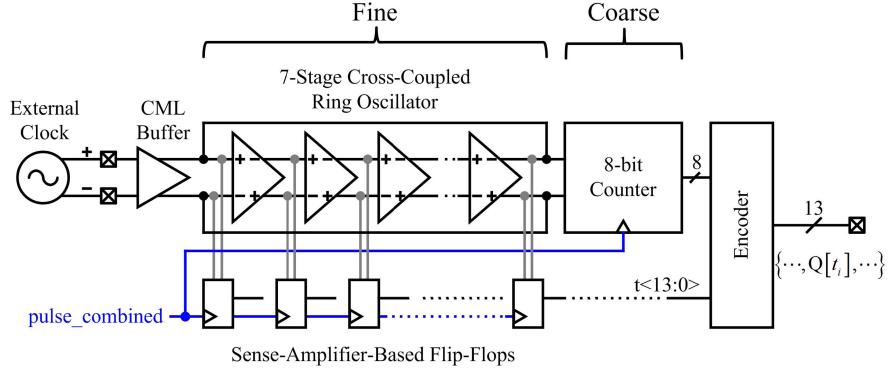


Fig. 17. Block diagram of the time quantizer including fine quantization and coarse quantization.

and delay variation. The pulse width is set between 300 and 400 ps to meet the minimum time spacing between two adjacent pulses (~ 500 ps) and can be controlled via the delay cell [12], which is tunable in this implementation for prototyping purposes.

E. Pulse Combiner and Level Encoder

In addition to minimizing the delay variation in the voltage quantization, it is important to match the propagation delay of each path in the pulse combiner all the way to the time quantizer input. Fig. 15 shows 15 identical sub-modules combining two pulses from adjacent comparators and pre-encoding the level information to indicate the origin of each pulse. A tree structure is utilized to match all the routing parasitics and guarantee each path passes the same number of sub-modules. A delay-balanced OR gate is compared in Fig. 16 to the conventional CMOS logic. Because the rising edge of the pulse contains the information of the sampling time instant, the propagation delay from either input port to the high-to-low transition at the Q port must be matched. In the conventional CMOS design, the high-to-low Elmore delay $t_{d,HL}$ can be written as $t_{d,HL,A} = R_N C_Q + (R_N + R_p) C_p$ and $t_{d,HL,B} = R_N C_Q$, where C_Q and C_p are the total parasitic capacitances at internal nodes, and R_N and R_p are the effective turn-ON resistance of NMOS and PMOS. To equalize two different delays $t_{d,HL,B} = t_{d,HL,A} = R_N C_Q + (R_N + R_p) C_p$, a replica of the pull-up circuit is added to match the load of the pull-down network. From the post-layout simulation, the delay difference can be limited < 1 ps with negligible performance degradation.

F. Time Quantizer

The time quantizer is implemented by a time-to-digital converter (TDC) (Fig. 17), which can be divided into coarse quantization and fine quantization [31]. The coarse time quantization is composed of an 8-bit counter via a 3-bit straight ring counter clocked at the ring oscillator frequency (> 4 GHz) and a 5-bit synchronous counter operating eight times more slowly. The fine time quantization is achieved by latching the internal states of the ring oscillator with the combined pulse. The ring oscillator contains seven pseudo-differential

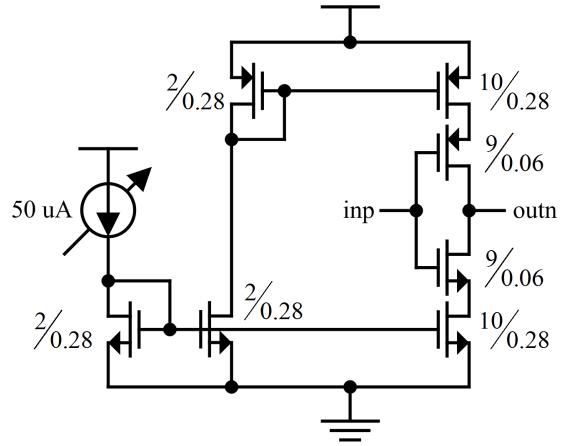


Fig. 18. Current-starved inverter with tunable delay used in the ring oscillator.

current-starved inverter stages (Fig. 18) and naturally provides 14 sub-phases within one oscillation period. The delay of each inverter sets the duration between sub-phases and hence defines the basic time quantization resolution [32]. To increase the time resolution, passive interpolation [33], [34] is applied with cross-coupled resistor ladders (Fig. 19) between inverter stages, which not only doubles TDC resolution but also mitigates the mismatch effects. Also, oscillation frequency can be adjusted in this prototype from 2 to 4.2 GHz to characterize impact of different time resolutions.

In addition, a sense-amplifier-based flip-flop [35] is used in the fine time quantization (Fig. 20) for better sensitivity and faster speed (up to 2 GHz). An additional pre-amplifier stage sharpens the waveforms from the passive phase interpolator and reduces the kickback noise from the following stages. Finally, an encoder with bubble correction logic combines both coarse and fine time codes and produces a final 13-bit output. In the case of low signal activity, two consecutive time codes may be recorded with multiple wraparounds in between because of the finite number of bits in the counter. Therefore, an extra overflow bit to indicate counter saturation is implemented and captured by another counter in the digital AA filter to properly unwrap the time code. However, to avoid

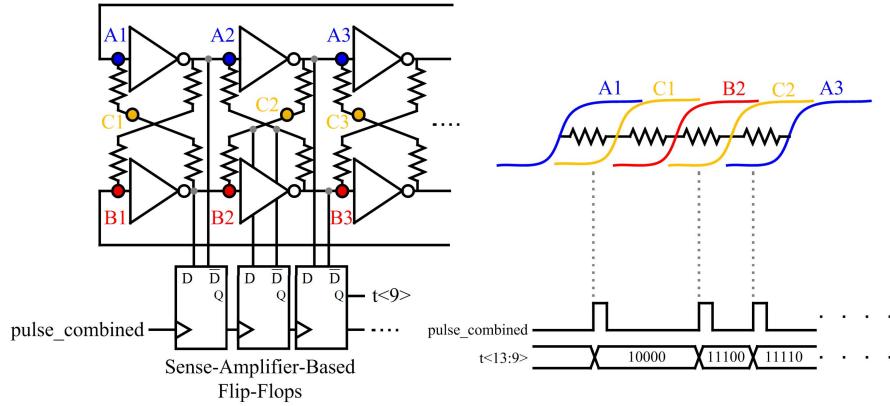


Fig. 19. Passive phase interpolation by cross-coupled resistors.

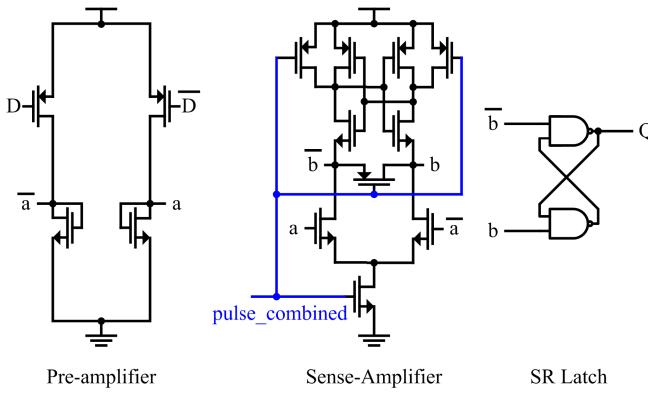


Fig. 20. Sense-amplifier-based flip-flop with pre-amplifier.

the time interval between samples being out of range in the case that the input signal frequency/amplitude is too small, a new sample with the same level code of the previous sample can be generated without a level-crossing event. This can be done either by forcing a pulse event to the pulse combiner or by inserting a new sample in the asynchronous FIFO queue. In this prototype, the full time-scale is designed sufficiently large to cover our test cases.

As it is difficult to achieve a well-defined oscillation frequency (time resolution) with a free-running ring oscillator over PVT, injection-locking is performed to synchronize the frequency and phase to the injected clock source in the steady state. In addition, the injection locking can suppress the phase noise accumulated throughout the delay elements, resulting in the less jitter. For sufficient coupling strength from the external clock source, which is proportional to the injection-locking bandwidth, a CML clock buffer is utilized featuring an adjustable coupling strength by tuning the current bias.

G. Design Tradeoffs

Considering different design spaces in terms of signal bandwidth, resolution, and power/area consumption, there are several design tradeoffs on the proposed architecture.

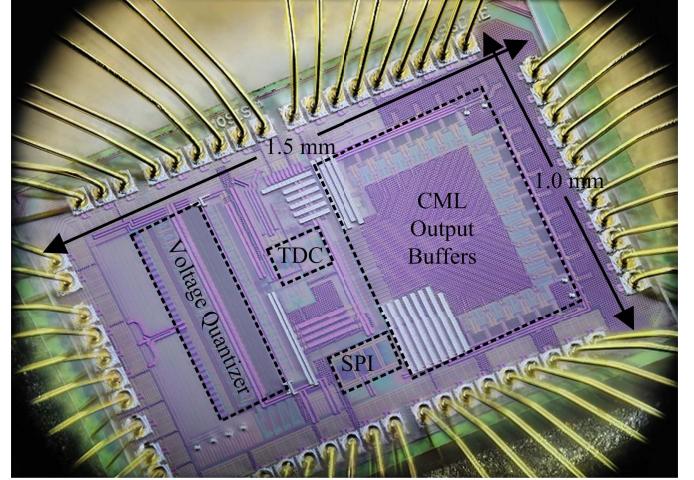


Fig. 21. Chip micrograph.

As mentioned in Section V-A, without a need to switch the reference voltage in the LCS the flash-based voltage quantizer can extend the signal bandwidth beyond tens of KHz [9]. In addition, the building blocks implemented in this prototype are intended for proof of concept and can be further optimized. For example, one may apply calibration techniques to address the signal-dependent delay variation, as the delay dependence on the signal slope or reference level can be learned and compensated in the time code. There are existing works that show learning the signal slope is feasible [13], [36], [37]. As a consequence, the desired bandwidth and gain of the comparators can be reduced to achieve a more power/area efficient design. For the time quantizer, since the time resolution is overdesigned for characterizing different noise sources, a coarser time resolution can be used to lower the oscillation frequency and the power consumption will be reduced accordingly.

It is also possible to further increase the signal bandwidth in the flash-based NUS ADC. For instance, the pulses from different comparators can trigger the time quantizer separately (bypass the pulse combiner) to increase the non-uniform sample throughput without reducing the input amplitude.

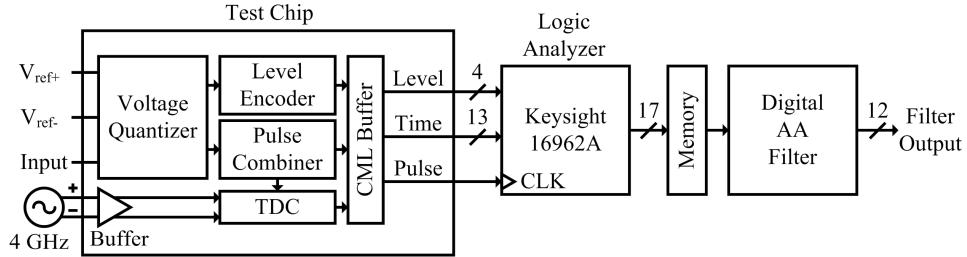


Fig. 22. Measurement setup.

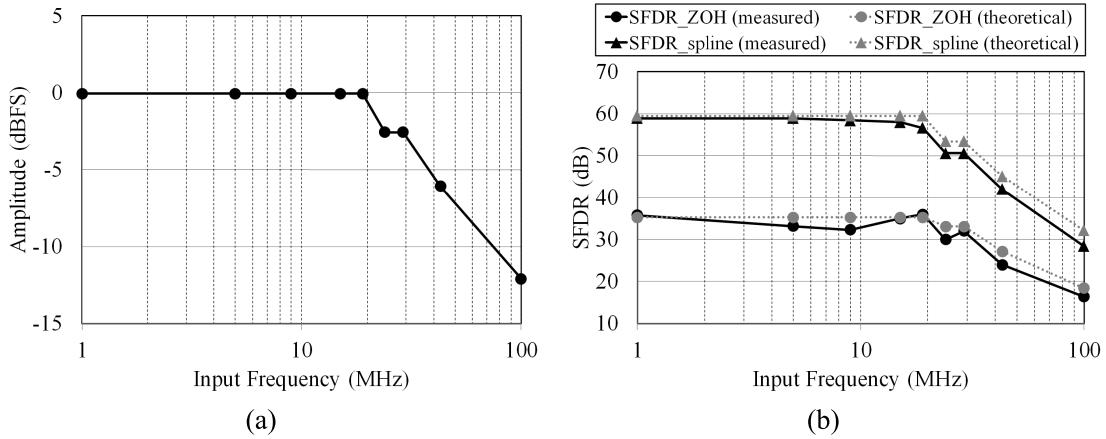


Fig. 23. (a) Input amplitude and (b) measured and theoretical SFDR (entire spectrum) over different frequencies with single sinusoidal input.

Another possible design choice is to use fewer numbers of levels in the voltage quantizer to tradeoff the signal bandwidth versus resolution while reducing power and area consumption. In an extreme case that only two quantization levels are deployed, the power and area consumption can lead to 70% reduction with around 4-bit resolution and hundreds of MHz signal bandwidth, using the same building blocks implemented in this prototype. Note that the building blocks can also be redesigned accordingly because of the reduced resolution. For example, the class-A continuous-time comparators can be replaced by the class-B architecture [12], e.g., inverter-based comparator, without static power consumption, and the requirements on the time quantizer will be relaxed as well. In summary, there is a wide range of design space that can be explored based on the proposed flash-based NUS ADC architecture while taking advantages of a flexible digital AA filter.

VI. MEASUREMENT RESULTS

The proof-of-concept prototype was fabricated in 65-nm CMOS on a core area of 0.3 mm^2 (Fig. 21). The core area includes the reference generator, comparators, pulse generators/combiner, level encoder, and time quantizer. Fig. 22 shows the measurement setup, where an external clock is applied for the injection locking, and voltage and time codes are recorded via a logic analyzer and local memory. To characterize the NUS ADC front end, the digital AA filter is configured to perform only interpolation without filtering, i.e., an all-pass filter response, with 12-bit output for a negligible finite word-length

effect. The SFDR is measured from the output interpolated using two representative reconstruction methods, ZOH and spline interpolation using Neville's algorithm, which consumes $0.002 \text{ mm}^2/0.3 \text{ mW}$ and $0.11 \text{ mm}^2/5.7 \text{ mW}$, respectively. The input swing is reduced when frequency is beyond 20 MHz [Fig. 23(a)] to ensure enough time spacing between non-uniform samples due to the bandwidth limitation from the PCB parasitics and data acquisition equipment. Fig. 23(b) shows the measured and theoretical (without circuit non-idealities) SFDR from the entire spectrum for a single sinusoidal input. The degradation mainly results from the delay variation due to finite comparator gain and the bandwidth. As shown in Fig. 24(a), the SNR (excluding harmonics from the interpolation error) with injection-locking enabled (with an external clock) and disabled (without an external clock) is measured from the output reconstructed at TDC resolution and is calculated within 20-MHz bandwidth around the input frequency as a reference study. The measured RMS jitter including on-chip drivers and time quantizer is 7 and 25 ps (integrated phase noise from frequency offset of 10 kHz to 20 MHz at 4 GHz) with injection-locking enabled and disabled, respectively. At low input frequency, the noise is dominated by the voltage quantizer which is around $900 \mu\text{V}_{\text{RMS}}$ calculated from (5), but the timing jitter begins to degrade SNR when the input frequency increases. The calculated SNR shown in Fig. 24 is computed using (4) and (5) assuming $900 \mu\text{V}_{\text{RMS}}$ input-referred noise of the voltage quantizer and 7-ps jitter of the time quantizer. The difference between the calculated and measured results at higher input frequency is due to the

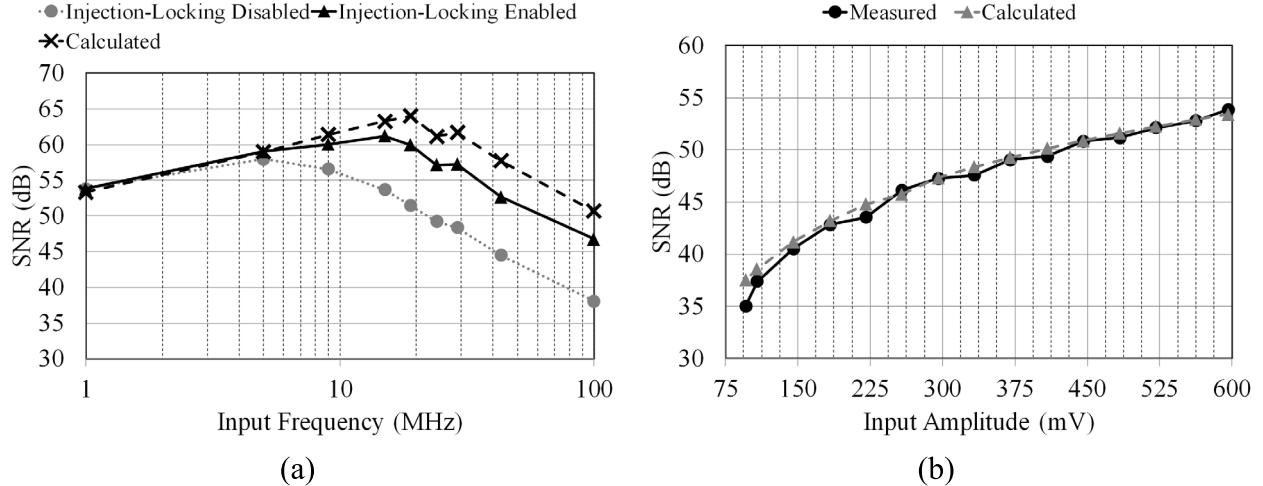


Fig. 24. Measured and calculated SNR (within 20-MHz bandwidth around the input frequency) (a) over different frequencies with single sinusoidal input and (b) over different input amplitude with 1-MHz input.

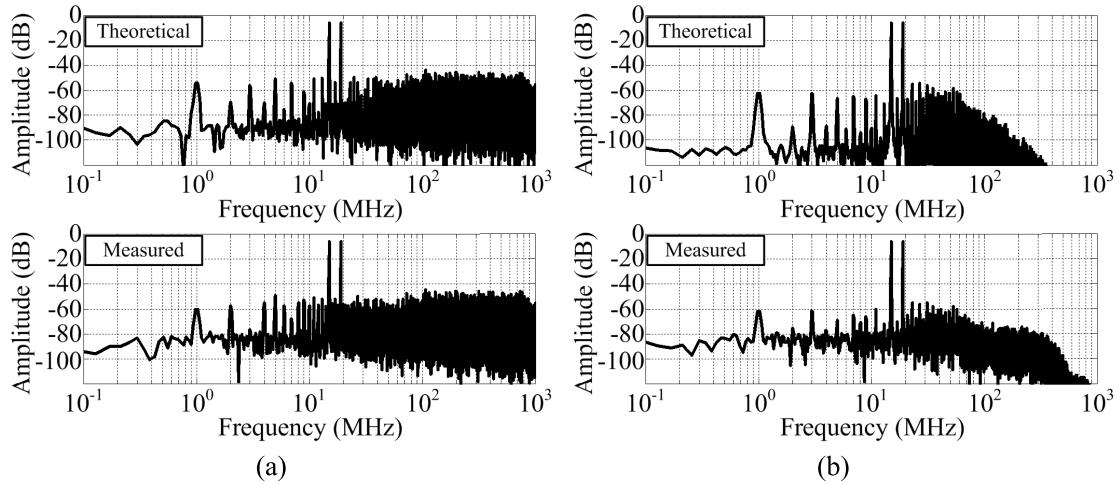


Fig. 25. Measured and theoretical spectra of two tones at 15 and 19 MHz using (a) ZOH and (b) spline interpolation.

kick-back noise from the comparators and the colored noise in the time quantizer. In addition, the supply noise and ground bounce also play a role in the pulse combiner because of the single-end implementation. Measured and calculated SNR over different input amplitudes are also shown in Fig. 24(b) with 1-MHz input. In Fig. 25, when two tones with equal amplitude at 15 and 19 MHz are injected, the measured output spectra compared to the theoretical ones (without circuit nonidealities) show the degradation in distortion terms within 2 dB, primarily resulting from the comparator propagation delay variation.

The linearity of the time quantizer can be characterized by disconnecting pulse combined from the pulse combiner and applying an external clock at a reference frequency of 300 MHz. By analyzing the code density statistic, the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of TDC are shown in Fig. 26, where the maximum DNL and INL are 0.41 and 0.43 LSB, respectively. Blocker tests are performed, including digital AA filter utilizing ZOH. Fig. 27 shows both low-pass filtering and bandpass filtering where a blocker is injected at 5 MHz, 40 dB higher than the

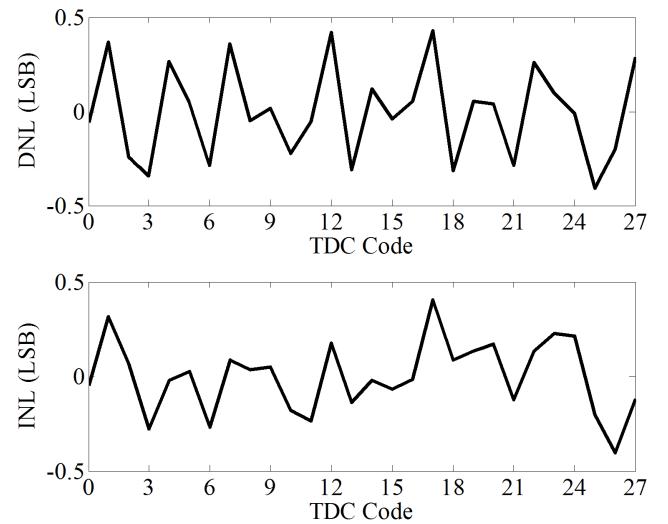


Fig. 26. Measured DNL and INL of the time quantizer.

desired signal at 4 MHz. In Fig. 28, a 30-dB higher single sinusoidal blocker is injected at 43 MHz with a 64-QAM

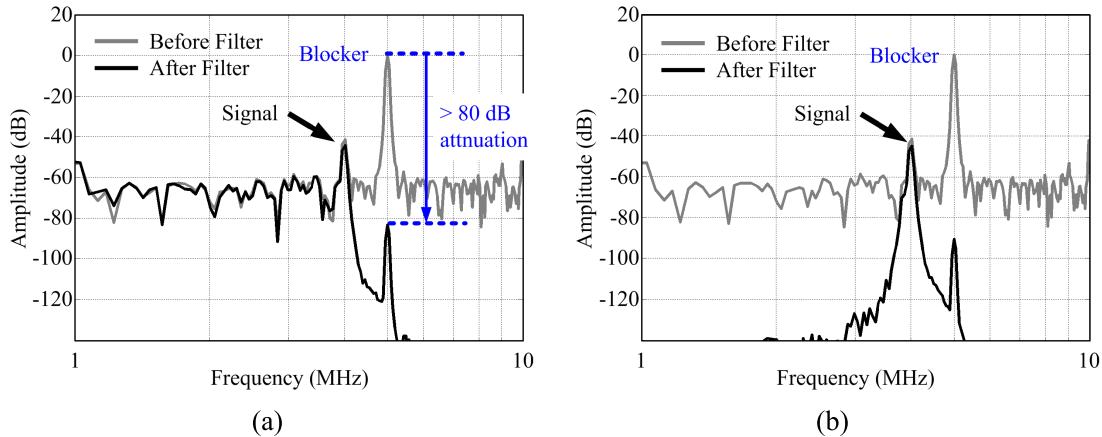


Fig. 27. Measured blocker tests with digital AA filter. (a) Low-pass. (b) Bandpass.

TABLE I
COMPARISON WITH ADCS UTILIZING NON-UNIFORM SAMPLES

	This Work ^b	[9] ^c	[10] ^d	[12] ^e
Alias-free Sampling	Yes	Yes	No	Yes
Alias-free Filtering	Yes	No	No	No
Uniform Digital Output	Yes	No	Yes	No
Supply Voltage	1.0 V	1.0 V	1.0 V	1.2 V
# of Levels	15-level	256-level	Signal-Dependent	8-level
Implementation	Differential	Single-ended	Single-ended	Single-ended
SFDR	56 dB ($f_{in} = 19$ MHz)	~ 60 dB ($f_{in} = 0.2$ kHz)	53 dB ($f_{in} = 290$ kHz)	23.5 dB (1-tap) 31.5 dB (6-tap) ($f_{in} = 1$ GHz)
SNDR	59.9 dB ($f_{in} = 19$ MHz) (BW = 20 MHz)	47 dB ($f_{in} = 0.2$ kHz) 62 dB ($f_{in} = 4$ kHz) (BW = 10 kHz)	49 dB ($f_{in} = 290$ kHz) (BW = 300 kHz)	20.3 dB (1-tap) 25.3 dB (6-tap) ($f_{in} = 1$ GHz) (BW = 2.4 GHz)
Power ^a	30 mW	1.23 mW	14 μ W	5 mW

^aPower dissipation on the digital signal processing is excluded.

^bBecause of alias-free sampling, SFDR is calculated from the entire spectrum without applying post-filtering on the spline-interpolated output. The alias-free filtering assumes the finite resolution of time quantizer is much smaller than the period of input signal, which introduces a negligible aliasing effect.

^cIt is an ADC/DSP/DAC system where non-uniform samples at ADC output are interpolated by ZOH.

^dNon-uniform samples at ADC output are interpolated by iterative algorithm [4].

^eIt is an ADC/DSP/DAC system where non-uniform samples at ADC output are interpolated by ZOH. Post-filtering is applied on the interpolated output and SFDR/SNDR are calculated from 0.8 GHz to 3.2 GHz excluding the half-harmonic ($f_{in}/2$).

signal; the EVM shows -28 dB evaluated at the output of the digital AA filter.

The peak power of 30 mW including reference generator (1.1 mW), comparators (12 mW), pulse genera-

tors (1.7 mW), pulse combiner/level encoder (1.2 mW), fine/coarse time quantizer (4.8 mW/3.2 mW), and clock buffer (1.6 mW) is measured when a full-scale 19-MHz signal and 4-GHz external clock are injected. Table I compares this

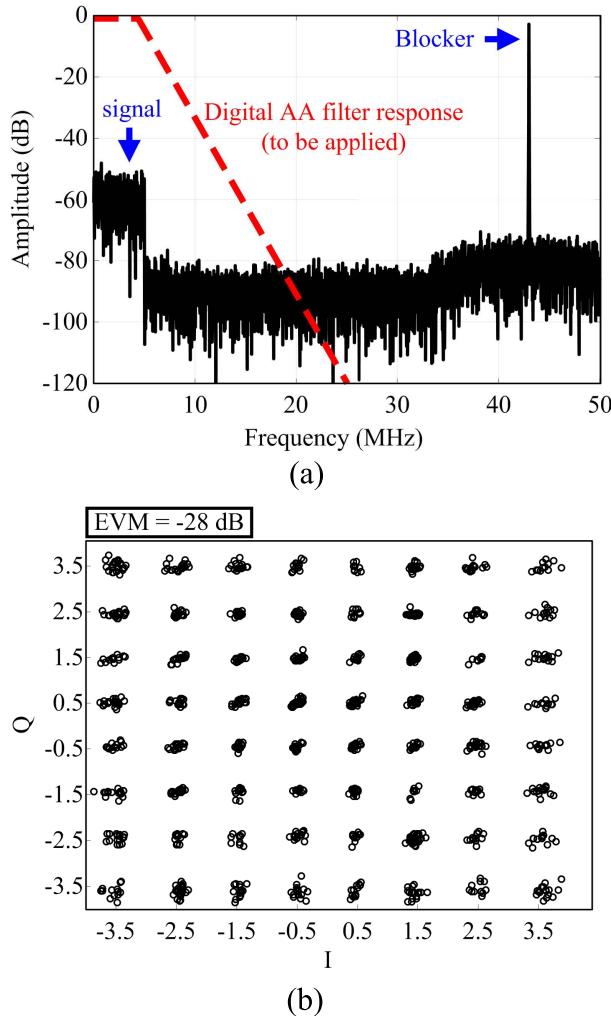


Fig. 28. Measured 64-QAM signal with 30-dB higher blocker presented at 43 MHz. (a) Before digital AA filter. (b) Constellation after digital AA filter.

proof-of-concept prototype with various ADCs utilizing non-uniform samples. The proposed ADC architecture achieves alias-free NUS, digital AA filtering, and uniform digital output at the same time, which is compatible with the existing synchronous DSP.

VII. CONCLUSION

A flash-based NUS ADC architecture using hybrid quantization in both the voltage and time domain is proposed to perform AA filtering in the non-uniform digital domain. Considering applications where the signal frequency, bandwidth, or activity may vary over time or operation conditions, the proposed ADC architecture can provide high agility, such as reconfigurable digital AA filter response and adaptable sampling rate. It relaxes the analog AA filter because of the analog-equivalent frequency response and reconfigurability of the proposed digital filter, which can benefit from technology scaling. Essentially, it provides a flexible way of performing analog-to-digital conversion and filtering, and enables different ways of designing an ADC.

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REFERENCES

- [1] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.
- [2] A. Bourdoux, J. Craninckx, A. Dejonghe, and L. V. der Perre, "Receiver architectures for software-defined radios in mobile terminals: The path to cognitive radios," in *Proc. IEEE Radio Wireless Symp.*, Jan. 2007, pp. 535–538.
- [3] C. T. C. Nguyen, "MEMS-based RF channel selection for true software-defined cognitive radio and low-power sensor communications," *IEEE Commun. Mag.*, vol. 51, no. 4, pp. 110–119, Apr. 2013.
- [4] F. Marvasti, *Nonuniform Sampling: Theory and Practice*. New York, NY, USA: Springer, 2001.
- [5] I. Bilinskis, *Digital Alias-Free Signal Processing*. West Sussex, U.K.: Wiley, 2007.
- [6] N. Sayiner, H. V. Sorensen, and T. R. Viswanathan, "A level-crossing sampling scheme for A/D conversion," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 43, no. 4, pp. 335–339, Apr. 1996.
- [7] C. Vezyrtzis and Y. Tsividis, "Processing of signals using level-crossing sampling," in *Proc. IEEE Int. Symp. Circuits Syst.*, Sep. 2009, pp. 2293–2296.
- [8] E. Allier, G. Sicard, L. Fesquet, and M. Renaudin, "A new class of asynchronous A/D converters based on time quantization," in *Proc. 9th IEEE Int. Symp. Asynchronous Circuits Syst.*, Vancouver, Canada, May 2003, pp. 196–205.
- [9] B. Schell and Y. Tsividis, "A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2472–2481, Nov. 2008.
- [10] S. Naraghi, M. Courcy, and M. P. Flynn, "A 9-bit, 14 μ W and 0.06 mm² pulse position modulation ADC in 90 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1870–1880, Sep. 2010.
- [11] T. Wang, D. Wang, P. J. Hurst, B. C. Levy, and S. H. Lewis, "A level-crossing analog-to-digital converter with triangular dither," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 2089–2099, Sep. 2009.
- [12] M. Kurchuk, C. W. Wu, D. Morche, and Y. Tsividis, "Event-driven GHz-range continuous-time digital signal processor with activity-dependent power dissipation," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2164–2173, Sep. 2012.
- [13] C. Weltin-Wu and Y. Tsividis, "An event-driven clockless level-crossing ADC with signal-dependent adaptive resolution," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2180–2190, Sep. 2013.
- [14] S. Patil, A. Ratiu, D. Morche, and Y. Tsividis, "A 3–10 fJ/conv-step error-shaping alias-free continuous-time ADC," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 908–918, Apr. 2016.
- [15] T. F. Wu, C. R. Ho, and M. Chen, "A flash-based non-uniform sampling ADC enabling digital anti-aliasing filter in 65nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2015, pp. 1–4.
- [16] Y. Tsividis, "Digital signal processing in continuous time: A possibility for avoiding aliasing and reducing quantization error," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process.*, vol. 2. Montreal, Canada, Sep. 2004, pp. 589–592.
- [17] M. Z. Win and R. A. Scholtz, "Impulse radio: How it works," *IEEE Commun. Lett.*, vol. 2, no. 2, pp. 36–38, Feb. 1998.
- [18] C. Duan, P. Orlík, Z. Sahinoglu, and A. Molisch, "A non-coherent 80.15.4a UWB impulse radio," in *Proc. IEEE Int. Conf. Ultra-WideBand*, Sep. 2007, pp. 146–151.
- [19] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 μ W wake-up receiver with –72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.
- [20] W. Tang *et al.*, "Continuous time level crossing sampling ADC for bio-potential recording systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 6, pp. 1407–1418, Jun. 2013.
- [21] D. Hand and M. Chen, "A non-uniform sampling ADC architecture with embedded alias-free asynchronous filter," in *Proc. IEEE GLOBECOM*, Sep. 2012, pp. 3707–3712.
- [22] T. F. Wu, S. Dey, and M. Chen, "A nonuniform sampling ADC architecture with reconfigurable digital anti-aliasing filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 10, pp. 1639–1651, Oct. 2016.
- [23] K. Kozmin, J. Johansson, and J. Delsing, "Level-crossing ADC performance evaluation toward ultrasound application," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1708–1719, Aug. 2009.

- [24] R. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed. Norwell, MA, USA: Kluwer, 2003.
- [25] K. Kozmin, J. Johansson, and J. Kostamovaara, "A low propagation delay dispersion comparator for a level-crossing AD converter," in *Proc. Analog Integr. Circuits Signal Process.*, vol. 62, Jan. 2010, pp. 51–61.
- [26] P. Palojarvi, T. Ruotsalainen, and J. Kostamovaara, "A 250-MHz BiCMOS receiver channel with leading edge timing discriminator for a pulsed time-of-flight laser rangefinder," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1341–1349, Jun. 2005.
- [27] J. Doernberg, P. R. Gray, and D. Hodges, "A 10-bit 5-Msample/s CMOS two-step flash ADC," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 241–249, Apr. 1989.
- [28] J.-P. Jansson, A. Mäntyniemi, and J. Kostamovaara, "A CMOS time-to-digital converter with better than 10 ps single-shot precision," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, Jun. 2006.
- [29] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, Feb. 1990.
- [30] Y. Wang *et al.*, "A 1.1 GHz 12 μ A/Mb-leakage SRAM design in 65 nm ultra-low-power CMOS with integrated leakage reduction for mobile applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 324–325.
- [31] C. R. Ho and M. Chen, "A fractional-N DLL with adaptive spur cancellation and calibration-free injection-locked TDC in 65 nm CMOS," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, Sep. 2014, pp. 97–100.
- [32] D. Koscielnik and M. Miskowicz, "Designing time-to-digital converter for asynchronous ADCs," in *Proc. IEEE Design Diag. Electron. Circuits Syst.*, Apr. 2007, pp. 1–6.
- [33] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1666–1676, Jul. 2008.
- [34] P. K. Sharma and M. Chen, "A 6 b 800 MS/s 3.62 mW Nyquist AC-coupled VCO-based ADC in 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Apr. 2013, pp. 1–4.
- [35] M. Matsui *et al.*, "A 200 MHz 13 mm² 2-D DCT macrocell using sense-amplifying pipeline flip-flop scheme," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1482–1490, Dec. 1994.
- [36] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.
- [37] N. Le Dortzetal, "A 1.62 GS/s time-interleaved SAR ADC with fully digital background mismatch calibration achieving interleaving spurs below 70 dBFS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 386–388.



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