A Nonuniform Sampling ADC Architecture With Reconfigurable Digital Anti-Aliasing Filter

Tzu-Fan Wu, Sourya Dey, and Mike Shuo-Wei Chen, *Member, IEEE*

***Abstract*—This work proposes a nonuniform sampling analog-to-digital converter (ADC) architecture that incorporates a reconfigurable digital anti-aliasing (AA) filter in the asynchronous digital domain. Considering applications where the signal frequency, bandwidth, or activity may significantly vary over time and operating conditions, it provides high flexibility, relaxes analog AA filter requirements, adapts its sampling rate according to the incoming signal, and interfaces seamlessly with synchronous digital processers. In addition, the proposed ADC architecture relaxes voltage quantization by introducing time quantization, which favors future technology scaling. Furthermore, approximated analytical noise models are derived to study the underlying quantization effects on the proposed digital AA filter. It explores the theoretical bounds of achievable signal-to-noise ratio (SNR) given different ADC and filter design parameters. Finally, some hardware design considerations and limitations are discussed.**

***Index Terms*—Analog-to-digital converter, anti-aliasing filter, level-crossing, nonuniform sampling, quantization noise.**

I. Introduction

CONVENTIONALLY, analog-to-digital converters (ADCs) sample an analog signal uniformly in time, leading to spectral replicas of the input signal at every integer multiple of the sampling frequency. Therefore, an analog anti-aliasing (AA) filter is typically required prior to sampling in order to prevent unwanted out-of-band noise or interference from folding back to the baseband and degrading the signal quality, a process referred to as aliasing. On the other hand, the trend of wireless communications is moving towards multi-standard and multi-band operation, which often leads to increasing AA filtering requirements and agility over different frequency bands and operation bandwidths. These types of systems [1]–[3] can demand tunable analog filters or switched filter banks to provide sufficient AA filtering prior to a uniformly sampled ADC to attenuate unwanted out-of-band blockers. There also exist some sampling techniques [4]–[7] that utilize analog integration to provide flexible AA filtering during uniform sampling.

Manuscript received February 14, 2016; revised May 3, 2016 and June 4, 2016; accepted June 20, 2016. Date of publication September 19, 2016; date of current version September 27, 2016. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under Grant 004897-00001 and by the National Science Foundation (NSF) under Grant ECCS-1351956. This paper was recommended by Associate Editor P. Rombouts.

The authors are with the Department of Electrical Engineering, University of Southern California, Los Angeles, CA 90089 USA (e-mail: tzufanwu@usc.edu; souryade@usc.edu; swchen@usc.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2016.2586523

Additionally, in some applications such as ultra-wideband impulse radio [8], [9], sensor networks [10], and biomedical electronics [11], signals are often sparse in time, i.e., duty cycle is low. Rather than sampling such signals at a constant rate, one can allow the sampling rate to adapt autonomously based on the input (assuming its amplitude is above the noise floor), i.e., generate samples whenever necessary, and avoid redundant samples when input signal is inactive. Motivated by these observations, the goal of this work is to explore a new ADC architecture that results in a flexible AA filtering strategy and adaptive sampling rate depending on input signal activity, instead of optimizing for fixed sampling rate applications. Finally, the ADC architecture should favor technology scaling and output synchronous digital bit stream in order to interface with existing digital processors seamlessly.

From a signal processing perspective, for a band-limited signal (deterministic or random), it is known that nonuniform sampling (NUS) can avoid signal aliasing, i.e., spectral replicas, and achieve error-free signal reconstruction if the average sampling rate satisfies the Nyquist rate [12]. As an example, unlike uniform sampling, level-crossing quantization [13], [14] adapts the average sampling rate to the input signal frequency content. While a nonband-limited signal can also be reconstructed without aliasing with a finite degree of freedom [12], [15], it will not be considered in the context of this paper as we intend to apply NUS in practical electronic systems with finite bandwidth. Some prior studies [16], [17] adopting NUS used continuous-time signal processing, which requires maintaining the temporal spacing of input samples to perform filtering while imposing strict timing requirements on the continuous-time processing circuits to preserve timing information. Another study [18] used a clock to record the time difference between two adjacent samples digitally, which is then used to perform digital filtering. The filter response used is equivalent to a finite impulse response (FIR) filter as the tap delays are fixed, and therefore the output spectrum contains aliases at a rate proportional to the tap delay. This prevents their use as AA filters.

To perform AA filtering in the digital domain, we propose an alias-free and reconfigurable asynchronous filter algorithm, referred to as a digital AA filter, within the NUS ADC architecture. Aliasing is prevented in the proposed filter by directly processing the nonuniform samples and dynamically adapting the filter response coefficients according to these irregular time intervals. This digital AA filter simultaneously resamples the filtered output at a constant rate, allowing direct interfacing with synchronous digital signal processing.

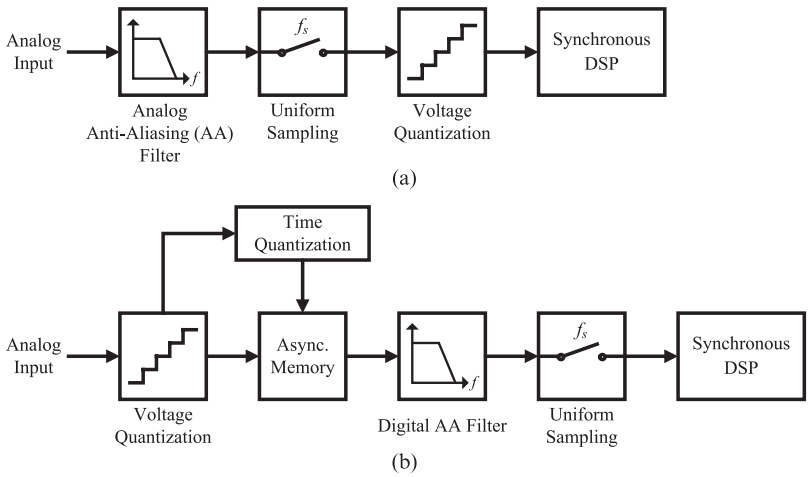


Fig. 1. (a) Uniform sampling ADC and (b) proposed nonuniform sampling ADC architecture.

Additionally, signal-to-noise ratio (SNR) is improved compared to conventional ADCs by using the digital AA filter to remove quantization and incoming noise.

Section II details the proposed NUS ADC architecture. Section III shows a theoretical analysis of voltage and time quantization noise to determine bounds for the SNR in the proposed digital AA filter. In Section IV, the filter algorithm is derived and numerical simulation results are shown to prove the concept. Finally, Section V suggests how the filter may be implemented in hardware.

II. Proposed Nonuniform Sampling ADC Architecture

The conventional ADC, shown in Fig. 1(a), utilizes an analog AA filter prior to the uniform sampling stage to band-limit the input signal, preventing unwanted high-frequency noise from folding back during sampling. The filtered input signal is sampled and quantized at a constant rate, and the resulting synchronous output can be interfaced with synchronous digital circuits. The key idea of our proposed NUS ADC architecture, shown in Fig. 1(b), is to move the AA filter after the quantizer into the asynchronous digital domain, followed by a synchronous digital sampler. The analog input signal is quantized via both voltage and time quantizers, which are used to record the amplitude and sampling time instants respectively. The time-stamped samples provide information for the proposed digital AA filter algorithm, which also converts the nonuniform samples into uniform samples. The AA filter algorithm can be reconfigured in the digital domain for arbitrary responses, which will be described in Section IV-E. In other words, the proposed NUS ADC transforms the conventional voltage quantization problem into a hybrid quantization mode, i.e., both voltage and time. Although time quantization causes aliasing of quantization noise [19], which will be discussed in Section III-D, this design constraint will be alleviated by technology scaling [20]. For example, state-of-the-art time quantizers achieve 1-ps accuracy [21], which is equivalent to a uniform sampling rate of 1 THz in order to maintain the same anti-aliasing bandwidth. In this case, for a conventional digital FIR filter and the proposed digital AA filter to have same filter response, the conventional digital FIR filter should be clocked at 1 THz. However, the proposed digital AA filter only needs to buffer the nonuniform samples and operate at the Nyquist rate, which will be elaborated in Section IV-B. In general, the proposed NUS ADC favors technological trends as time accuracy continues to improve while voltage accuracy becomes more limited due to the demand for lower supply voltages.

III. Quantization Noise Modeling

The voltage quantizer can be implemented with an n-bit level-crossing quantizer, where $2^n - 1$ comparator thresholds or detection levels divide the full-scale input range from $-A$ to $+A$ into 2^n equally spaced intervals. Whenever a band-limited input signal crosses any of these predefined thresholds, nonuniform samples are generated and its amplitude information is recorded, i.e., sampling and voltage quantization is performed at the same time. On the other hand, if the average sampling rate of a NUS satisfies the Nyquist rate, it can prevent aliasing and allow perfect reconstruction [12], [22]. In a practical case, we may always find a level density that guarantees this average sampling rate for signals with a sufficient level-crossing rate. A relation between level density and the average sampling rate has been discussed in [23]. However, such an error-free reconstruction algorithm involves high computation complexity; therefore, in the context of this paper, we will analyze the NUS ADC performance (Section III) and propose the underlying signal processing (Section IV) with the simplest reconstruction algorithm, i.e., zero-order-hold (ZOH), for ease of implementation. This provides a lower bound for performance and allows better understanding of the limitations of this ADC architecture.

To model the errors in the proposed architecture shown in Fig. 2, we separate them into an additive voltage quantization noise (VQ) given this simple signal reconstruction algorithm, and time quantization noise (TQ). Thus, the quality of the reconstructed NUS ADC outputs can be characterized by both voltage and time quantization noise to better understand the SNR bounds of the proposed NUS ADC architecture. We first discuss modeling of voltage quantization noise due to ZOH interpolator being used in the proposed digital filter and

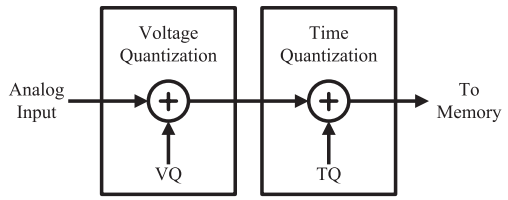


Fig. 2. Model of additive voltage and time quantization noise in proposed ADC.

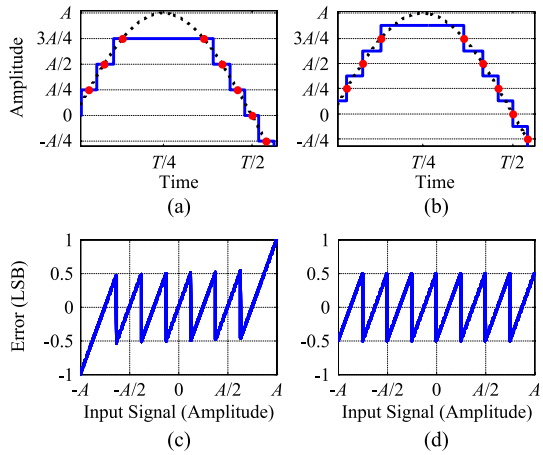


Fig. 3. Input sinusoid of time period T (dotted line) and its reconstruction (solid line) from points generated by the level-crossing quantizer, along (a) comparator thresholds versus (b) half LSB shifted from comparator thresholds. Quantization error versus input signal using (c) comparator thresholds versus (d) half LSB shifted from comparator thresholds.

derive its SNR in approximated forms, and later examine time quantization effects.

A. Voltage Quantization Noise Characteristics

In terms of signal reconstruction, ZOH uses horizontal reconstruction levels and can be done using two different methods. The difference between them is a half least significant bit (LSB) shift in the reconstruction levels. Prior works [24]–[26] have used the actual $2^n - 1$ detection levels as the reconstruction levels [Fig. 3(a)], resulting in larger quantization error [Fig. 3(c)]. Therefore, the proposed digital AA filter uses reconstruction levels shifted a half LSB up and down from the detection levels [Fig. 3(b)] so that there are 2^n reconstruction levels. This limits the quantization error to half LSB for the entire input signal range [Fig. 3(d)]. It should be noted that the implementation requirement is the same for both cases as both use n bits and $2^n - 1$ comparators.

We define voltage quantization noise $vq(x)$ as the amplitude difference between input signal x and ZOH reconstructed signal. The value of LSB is assumed to be normalized to one, such that full-scale amplitude $A = 2^{n-1}$. From the sawtooth profile of Fig. 3(d), quantization noise can be decomposed into a Fourier series of x. Analyzing the sinusoidal input case where $x(t) = A\sin(\omega_0 t)$, $vq(x)$ becomes [27], [28]

$$vq\left(x(t)\right) \equiv vq(t) = -\sum_{k=1}^{\infty} \frac{\sin\left(2\pi k x(t)\right)}{\pi k} = -\sum_{m=1}^{\infty} A_m \sin\left((2m-1)\omega_o t\right) \quad (1)$$

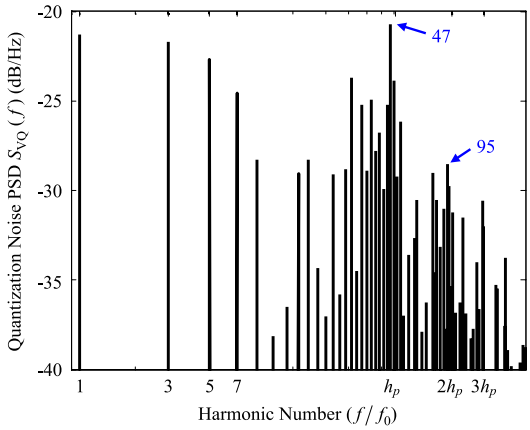


Fig. 4. Quantization noise PSD for sinusoidal input passed through a 4-bit level-crossing quantizer, shown on a logarithmic frequency scale.

where

$$A_m = \sum_{k=1}^{\infty} \frac{2}{\pi k} J_{2m-1}(2\pi k A) \quad (2)$$

and $J_{2m-1}(.)$ is the Bessel function of the first kind of order $2m-1$ resulting from doing the Jacobi-Anger expansion in (1). Equation (1) shows that quantization noise is the sum of all odd harmonics of the input signal frequency, including the fundamental. Therefore, $vq(t)$ is periodic with period equal to that of the input sinusoid, which is $1/f_0$ or $2\pi/\omega_0$. We now express $vq(t)$ as a Fourier series in time in order to analyze the spectral distribution of energy

$$vq(t) = \sum_{u=-\infty}^{\infty} C_u e^{ju\omega_0 t} \quad (3)$$

where

$$C_u = \frac{|u|}{u}\frac{j}{\pi}\sum_{k=1}^{\infty}\frac{J_{|u|}(2\pi kA)}{k}, \quad \text{when } u \text{ is odd}$$
$$= 0, \quad \text{when } u \text{ is even.} \quad (4)$$

We can now use this value of C_u and the fact that $|C_u| = |C_{-u}|$ to obtain the single-sided power spectral density (PSD) of voltage quantization noise as

$$S_{\mathrm{VQ}}(f) = \frac{2}{\pi^2}\sum_{u=1,3,5,\ldots}^{\infty}\left(\sum_{k=1}^{\infty}\frac{J_u(2\pi kA)}{k}\right)^2 \delta(f - uf_0) \quad (5)$$

where δ is the Dirac delta function. The value $2\pi A = 2^n\pi$ is of considerable interest; we shall refer to it as h_p and to its corresponding frequency $2\pi A f_0$ as f_p. Fig. 4 shows the plot of $S_{\mathrm{VQ}}(f)$ vs. harmonic number f/f_0 for a 4-bit quantizer $(h_p = 50)$, obtained by setting upper limits of 100 and $100h_p$ (i.e., 5000) for the summations over k and u, respectively. The terms beyond those values in (5) are negligible in comparison with other terms. The following inferences can be made from (5) and Fig. 4. Firstly, the Dirac delta function confirms that voltage quantization noise $vq(t)$ consists of discrete tones at the input frequency f_0 and its odd harmonics only, as predicted

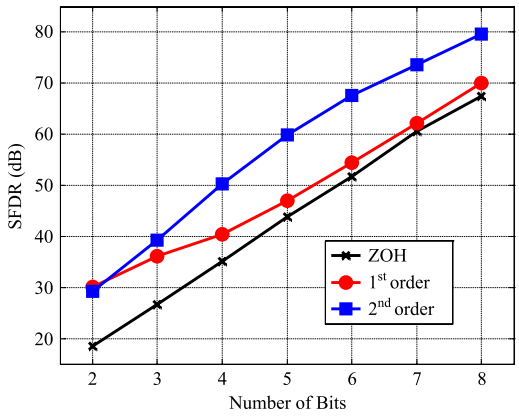


Fig. 5. SFDR versus number of bits using different interpolation techniques.

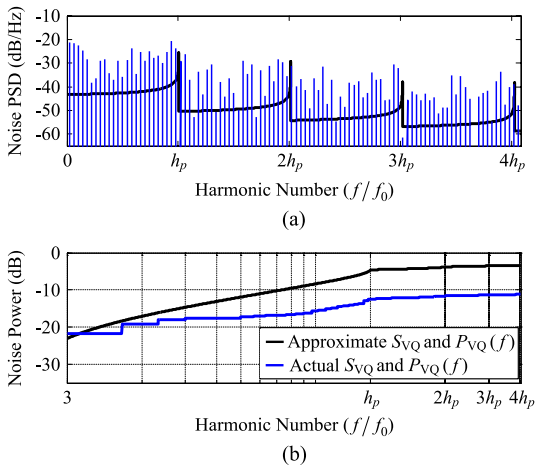


Fig. 6. Comparison of (a) $\hat{S}_{\mathrm{VQ}}(f)$ with $S_{\mathrm{VQ}}(f)$, using a linear frequency scale and (b) $\hat{P}_{\mathrm{VQ}}(f)$ with $P_{\mathrm{VQ}}(f)$ using a logarithmic frequency scale.

by the time-domain expression in (1). It should be noted that the noise tone at f_0 will only cause slight changes in signal amplitude and phase. It will not be considered as noise in the context of SNR in this paper. Therefore, our analysis will consider noise content at frequencies starting from $3f_0$. Secondly, $J_u(x)$ reaches its global maximum (which is the first local maximum) for $u \approx 0.95x$ [29]. This explains the notable characteristic of "high-frequency energy maxima" occurring at harmonic numbers close to integer multiples of h_p, as shown in Fig. 4. We conclude that maximum noise energy is present at the kth harmonic, where k is the closest odd integer to $0.95h_p$, and this determines the spurious free dynamic range (SFDR) of the ADC.

Apart from ZOH, other advanced techniques such as first-order (linear) and second-order polynomial interpolation can be used to reconstruct a signal from its nonuniform samples. These techniques can be theoretically analyzed using approaches analogous to the ZOH case, which will be the scope of our future work. Numerical simulations of the SFDR using higher order interpolators were performed with different numbers of voltage quantizer bits, as shown in Fig. 5. As expected, SFDR improves with increasing order, inspiring us to explore higher-order interpolators combined with the proposed digital AA filter algorithm, which is elaborated in Section IV-D.

B. Approximated Voltage Quantization Noise Model

It is observed from (1) that the quantization noise waveform $vq(t)$ is essentially phase-modulated by the input $x(t)$. In general, the PSD $S_C(\omega)$ of a signal $c(t)$ being phase-modulated by $p(t)$, i.e., $c(t) = A_c \sin[\omega_c t + \alpha p(t)]$, can be approximated as [30]

$$S_C(\omega) = \frac{A_c^2 \pi}{2\alpha}\left[\dot{g}\left(\frac{\omega-\omega_c}{\alpha}\right) + \dot{g}\left(\frac{-\omega-\omega_c}{\alpha}\right)\right] \quad (6)$$

where α is a constant, and $\dot{g}(.)$ is the derivative of the distribution function of $p(t)$. If $p(t)$ is a sinusoid with amplitude A_p and frequency ω_p, $\dot{g}$ becomes [24]

$$\dot{g}(z) = \frac{1}{\omega_p A_p \pi \sqrt{1-\left(\frac{z}{\omega_p A_p}\right)^2}}. \quad (7)$$

Based on (1), we can now derive an approximate simplified formula, $\hat{S}_{\mathrm{VQ}}(f)$, for $S_{\mathrm{VQ}}(f)$ by making these replacements above $c(t)$ with $vq(t)$, $p(t)$ with $x(t) = A\sin(\omega_0 t)$, A_c with $-1/(\pi k)$, α with $2\pi k$, and ω_c with zero. Then we get

$$\hat{S}_{\mathrm{VQ}}(f) = \frac{1}{2\pi^3 A f_0}\sum_{k=1}^{\infty}\frac{1}{k^3}\left(\sqrt{1-\left(\frac{f}{2\pi A f_0 k}\right)^2}\right)^{-1}. \quad (8)$$

Equation (8) presents a simplified function for the quantization noise with double side band, consisting of a series of decaying segments, where the kth segment is defined as the frequency range from $(k-1)f_p$ to kf_p. Fig. 6 compares $\hat{S}_{\mathrm{VQ}}(f)$ with $S_{\mathrm{VQ}}(f)$ in part (a), and part (b) shows the corresponding noise power profiles $P_{\mathrm{VQ}}(f)$ and $\hat{P}_{\mathrm{VQ}}(f)$ obtained by integrating $S_{\mathrm{VQ}}(f)$ and $\hat{S}_{\mathrm{VQ}}(f)$ respectively, from 0 to f. We see that (8) is continuous in frequency over every segment, as opposed to the discrete tones of (5). Also, the singularities of (8) at values of $f = kf_p$ overestimate the high-frequency energy maxima of (5). These effects combine to make $\hat{P}_{\mathrm{VQ}}(f)$ larger than $P_{\mathrm{VQ}}(f)$, and the error between them reaches a maximum of around 7 dB at h_p, after which it remains constant as the noise tones beyond the first segment are decaying and, compared to the first segment, contribute little to the overall noise power. Note that in the case of applying a low-pass digital AA filter, we are mainly interested in quantization noise in the low-frequency region, where we see that $\hat{P}_{\mathrm{VQ}}(f)$ is a fairly accurate model of $P_{\mathrm{VQ}}(f)$.

Equation (6) was derived by approximating a Taylor series using its first term. A more accurate approximation is possible by involving the 4th derivatives of $\dot{g}$ with respect to ω [30]. However, the increment in accuracy is small and the resulting expression is quite complex. Hence, it is more practical to use (8) as the approximation of voltage quantization noise PSD.

C. SNR Due to Voltage Quantization

In this section, we will derive the SNR of the NUS ADC based on the voltage quantization noise models derived thus far.

Time quantization effects will be ignored for now and addressed in Section III-D. It is known that in uniform sampling ADCs, the sampling frequency f_s is typically chosen to be greater than $2f_0$ to satisfy the Nyquist rate, and the frequency band of interest is from DC to $f_s/2$. As the high-frequency voltage quantization noise aliases back to the band of interest and makes the noise appear white, the well-known formula SNR $= 6.02n + 1.76$ can be derived. Due to the absence of aliasing in the NUS ADC, we consider voltage quantization noise PSD exactly as derived in (5), starting from the tone at $3f_0$. The PSD must be integrated within the band of interest, i.e., from DC to f_c, which is the low-pass digital AA filter cutoff frequency. Defining normalized filter bandwidth $c = f_c/f_0$ and using $A = 2^{n-1}$ as before, total noise power P_{VQ} in the passband is

$$P_{\mathrm{VQ}} = \int_0^{f_c} S_{\mathrm{VQ}}(f)df = \frac{2}{\pi^2} \sum_{u=3,5,7,\ldots}^{c} \left(\sum_{k=1}^{\infty} \frac{J_u(2^n \pi k)}{k} \right)^2. \quad (9)$$

Signal power P_{SIG} is given as $A^2/2 = 2^{2n-3}$. Then, the exact value of the NUS ADC SNR (in dB) due to voltage quantization can be numerically computed as a function of n and c

$$\mathrm{SNR}_{\mathrm{VQ}} = 10 \log_{10} \left(\frac{2^{2n-3}}{P_{\mathrm{VQ}}} \right). \quad (10)$$

Note that, since we consider noise energy starting from $3f_0$, $\mathrm{SNR}_{\mathrm{VQ}}$ is infinite when $c < 3$. This is a direct consequence of the alias-free property of the proposed ADC, assuming a zero time quantization step.

Although (10) gives the exact value of $\mathrm{SNR}_{\mathrm{VQ}}$, a simpler formula is desirable. This can be done by replacing P_{VQ} with $\hat{P}_{\mathrm{VQ}}$ in (10), where $\hat{P}_{\mathrm{VQ}}$ is the total passband noise power obtained by integrating the approximated PSD, $\hat{S}_{\mathrm{VQ}}(f)$, of (8). We first establish a relationship between the discrete tones of $S_{\mathrm{VQ}}(f)$ and the continuous form of $\hat{S}_{\mathrm{VQ}}(f)$. As the tones in $S_{\mathrm{VQ}}(f)$ are spaced $2f_0$ apart, each tone can be considered to represent the frequency band from $-f_0$ to $+f_0$ in its tone frequency. In other words, the tone at f_0 in $S_{\mathrm{VQ}}(f)$ represents the range from DC to $2f_0$ in $\hat{S}_{\mathrm{VQ}}(f)$, the tone at $3f_0$ in $S_{\mathrm{VQ}}(f)$ represents the range from $2f_0$ to $4f_0$ in $\hat{S}_{\mathrm{VQ}}(f)$, and so on. Since we do not consider the first noise tone of $S_{\mathrm{VQ}}(f)$ at f_0, the integration of $\hat{S}_{\mathrm{VQ}}(f)$ should start from $2f_0$, and is given as follows:

$$\begin{aligned} \hat{P}_{\mathrm{VQ}} &= 2 \int_{2f_0}^{f_c} \hat{S}_{\mathrm{VQ}}(f)df \\ &= \frac{1}{\pi^3 A f_0} \sum_{k=1}^{\infty} \frac{1}{k^3} \left(\int_{2f_0}^{f_c} \frac{df}{\sqrt{1 - \left(\frac{f}{2\pi A f_0 k} \right)^2}} \right). \end{aligned} \quad (11)$$

Then $\widehat{\mathrm{SNR}}_{\mathrm{VQ}}$ can be calculated as $10 \log_{10}(2^{2n-3}/\hat{P}_{\mathrm{VQ}})$. However, as shown in Fig. 6(b), $\hat{P}_{\mathrm{VQ}}$ overestimates P_{VQ} and so $\widehat{\mathrm{SNR}}_{\mathrm{VQ}}$ is lower than the real $\mathrm{SNR}_{\mathrm{VQ}}$ obtained from (10). An empirical correction factor will be introduced later to account for this approximation error. Due to the low-pass digital AA filter, the limiting value of the summation over k is k_s, such that $2\pi A(k_s - 1) < c < 2\pi A k_s$. The $k = k_s$ term can be expressed as

$$\begin{aligned} \hat{P}_{\mathrm{VQ}_{ks}} &= \frac{1}{\pi^3 A f_0 k_s^3} \int_{2f_0}^{f_c} \left[\sqrt{1 - \left(\frac{f}{2\pi A f_0 k_s} \right)^2} \right]^{-1} df \\ &= \frac{2}{\pi^2 k_s^2} \left[\arcsin \left(\frac{f}{2\pi A f_0 k_s} \right) \right]_{2f_0}^{f_c} \\ &= \frac{2}{\pi^2 k_s^2} \left[\arcsin \left(\frac{c}{2\pi A k_s} \right) - \arcsin \left(\frac{2}{2\pi A k_s} \right) \right]. \end{aligned} \quad (12)$$

While performing the integration for values of $k < k_s$, the frequency band under consideration is to the kth segment, which ends at $kf_p = 2\pi k A f_0$. Thus, for the terms where $k < k_s$

$$\begin{aligned} \hat{P}_{\mathrm{VQ}_k} &= \frac{2}{\pi^2 k^2} \left[\arcsin \left(\frac{f}{2\pi A f_0 k} \right) \right]_{2f_0}^{kf_p} \\ &= \frac{1}{\pi k^2} - \frac{2}{\pi^2 k^2} \arcsin \left(\frac{2}{2\pi A k} \right). \end{aligned} \quad (13)$$

We can now compute total noise power $\hat{P}_{\mathrm{VQ}}$ from (12) and (13)

$$\begin{aligned} \hat{P}_{\mathrm{VQ}} = \sum_{k=1}^{k_s} \hat{P}_{\mathrm{VQ}_k} &= \frac{1}{\pi} \left(\sum_{k=1}^{k_s - 1} \frac{1}{k^2} \right) + \frac{2}{\pi^2 k_s^2} \arcsin \left(\frac{c}{2\pi A k_s} \right) \\ &\quad - \frac{2}{\pi^2} \left(\sum_{k=1}^{k_s} \frac{1}{k^2} \arcsin \left(\frac{2}{2\pi A k} \right) \right). \end{aligned} \quad (14)$$

For most practical applications, the filter bandwidth of interest is small, i.e., $c \ll h_p$, which implies that $k_s = 1$. Writing $A = 2^{n-1}$, (14) reduces to

$$\hat{P}_{\mathrm{VQ}} = \frac{2}{\pi^2} \left[\arcsin \left(\frac{c}{2^n \pi} \right) - \arcsin \left(\frac{2}{2^n \pi} \right) \right]. \quad (15)$$

$\widehat{\mathrm{SNR}}_{\mathrm{VQ}}$ can now be computed as $10 \log_{10}(2^{2n-3}/\hat{P}_{\mathrm{VQ}})$. Since both c and 2 are much smaller than h_p, the $\arcsin(.)$ and $\log_{10}(.)$ functions can be approximated by their Taylor series

$$\arcsin(x) \approx x \left(1 + \frac{1}{6} x^2 \right) \quad (16a)$$

$$\log_{10}(1 + x) \approx x \log_{10} e \approx 0.43x. \quad (16b)$$

The final expression for $\widehat{\mathrm{SNR}}_{\mathrm{VQ}}$ then becomes

$$\widehat{\mathrm{SNR}}_{\mathrm{VQ}} = 9.03n + 2.87 - 10\log(c-2) - \frac{0.07}{4^n}(c^2 + 2c + 4). \quad (17)$$

It should be noted that (17) is only valid for $c > 3$, as explained earlier. Numerical simulations show that (17) closely models (10) when c is smaller; however, the error between them, defined as $\mathrm{SNR}_{\mathrm{VQ}} - \widehat{\mathrm{SNR}}_{\mathrm{VQ}}$, increases as c increases because the approximations of (16a) and (16b) are less accurate. In fact, the error reaches a maximum at $c = h_p$ because $\hat{P}_{\mathrm{VQ}}(f)$ is larger than $P_{\mathrm{VQ}}(f)$, as explained in Section III-B. Since

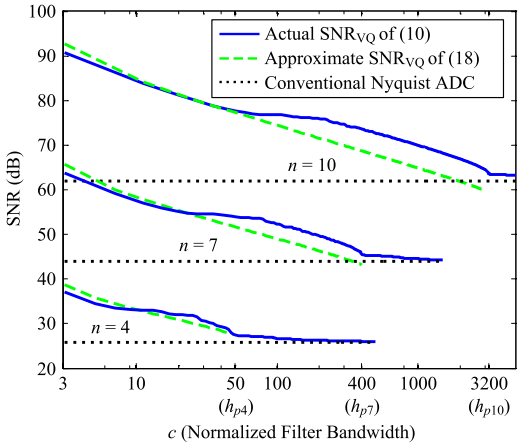


Fig. 7. Comparison of NUS ADC SNR$_{VQ}$ with corrected $\widehat{\text{SNR}}_{VQ}$ and conventional ADC SNR as c varies, for 4-, 6-, and 10-bit quantizers, whose h_p values are denoted as h_{p4}, h_{p6}, and h_{p10} respectively.

h_p increases as n increases, the rate of increase of error with c slows for larger values of n. Based on these observations, we incorporate an empirical correction factor to adjust the coefficient of the $-\log(c-2)$ term in (17) based on numerical simulations. The coefficient is lower than 10 for low values of n, and asymptotically approaches 10 as n increases, showing exponential behavior. Our objective is to achieve an accurate approximation of $\widehat{\text{SNR}}_{VQ}$ that is good for the entire range $3 \leqq c \leqq h_p$. Using curve-fitting techniques, the adjusted coefficient for $-\log(c-2)$ is incorporated in (18) to give

$$\widehat{\text{SNR}}_{VQ} = 9.03n + 2.87 - \left[10 - 12\cdot(1.35)^{-n}\right]\log(c-2) - \frac{0.07}{4^n}(c^2+2c+4). \quad (18)$$

The curve-fitting techniques used were optimized for the more practical cases where low-pass filter bandwidth is smaller, i.e., c is lower, and n is smaller for lower complexity implementation. Therefore, SNR approximation in those regimes is better, as shown in Fig. 7. The figure also shows that NUS ADC SNR presents significant improvement over the SNR of conventional uniform sampling Nyquist ADCs. Further comparison with uniform sampling ADCs will be provided in Section III-E.

D. Time Quantization Noise Modeling

The quantization noise models discussed so far arise only from voltage quantization; consequently, the derived equations for SNR$_{VQ}$ assume that the time information of a sample can be known with infinite precision. In reality, the time quantizer has a resolution t_{tq} which causes voltage quantization noise to fold in the frequency spectrum in the form of time quantization noise. The single-sided PSD of time quantization noise is

$$S_{TQ}(f) = \sum_{m=1}^{\infty} S_{VQ}(f + mf_{tq}) \quad (19)$$

where $f_{tq} = 1/t_{tq}$. The double-sided filter passband is from frequencies $-f_c$ to $+f_c$. The noise power folding back into this passband from the mth shifted copy of noise is given by integrating $S_{VQ}(f)$ from $(mf_{tq} - f_c)$ to $(mf_{tq} + f_c)$. Then the total noise power P_Q becomes

$$P_Q = P_{VQ} + P_{TQ} = P_{VQ} + \sum_{m=1}^{\infty} \int_{mf_{tq}-f_c}^{mf_{tq}+f_c} S_{VQ}(f)df \quad (20)$$

from which the final value of SNR can be calculated as

$$\text{SNR} = 10\log_{10}\left(\frac{P_{SIG}}{P_Q}\right) = 10\log_{10}\left(\frac{2^{2n-3}}{P_Q}\right). \quad (21)$$

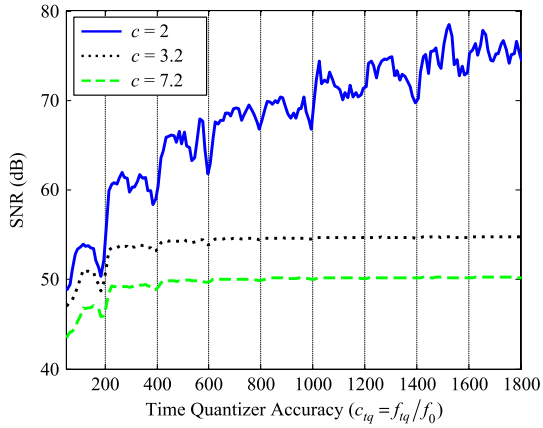


Fig. 8. Variation of SNR of a 6-bit quantizer with c_{tq} for different values of c.

Fig. 8 shows the variation of SNR with $c_{tq} = f_{tq}/f_0$ under different normalized filter bandwidths c, which better shows the time quantization effects. When $c < 3$, P_{VQ} is zero and only P_{TQ} is present, which consistently decreases as c_{tq} increases due to the decrease in noise folding. This leads to a continuous increase in SNR. When $c > 3$, P_{VQ} is not zero and dominates over P_{TQ} for large values of c_{tq}, where negligible noise folds back. This leads to saturation of the SNR, as shown in Fig. 8 for the 6-bit case. The limit for the summation over m in (20) is set to 10, beyond which changes are negligible.

When $c_{tq} \approx kh_p$, where k is an integer, shifted copies of the high-frequency noise maxima close to integer multiples of h_p will fall inside the filter passband. The effect is more pronounced for low values of k such as 1, 2, and 3. A similar phenomenon exists when $h_p \approx kc_{tq}$ as a shifted copy of the first noise maximum at h_p will fold back to the passband. These effects will degrade the SNR, as shown by the downward spikes at kh_p and h_p/k in Fig. 8 and later in Fig. 9.

Equation (20) is not suitable for hand calculations, even if we replace P_{VQ} and $S_{VQ}(f)$ with their approximations, $\hat{P}_{VQ}$ and $\hat{S}_{VQ}(f)$. A practical way to compute the summed integral of (20) is by modeling $\hat{S}_{VQ}(f)$ as a decreasing exponential of the form af^{-b}, as it comprises infinitely many decaying segments. To achieve this, we found the area under the curve for each segment and then modeled it by a constant value equal to its area divided by f_p. This approach preserves the noise power of each segment. Since the initial segments contribute more passband noise, a and b were calculated by taking the first two segments and finding the points of intersection of the constant

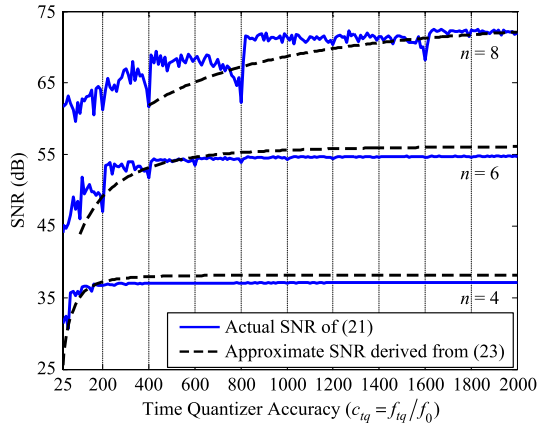


Fig. 9. Comparison of $\widehat{\text{SNR}}$ with real SNR for 4-, 6-, and 8-bit quantizers, as time quantizer accuracy c_{tq} varies, with c fixed at 3.2.

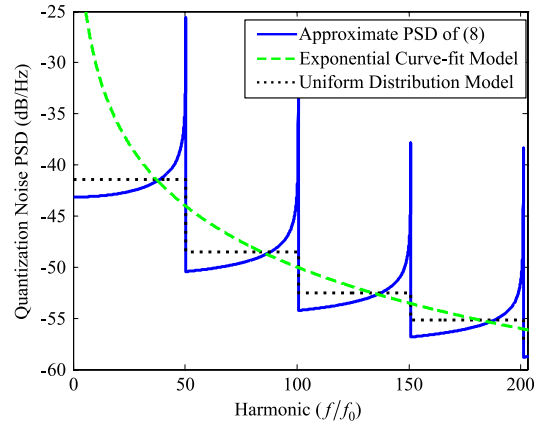


Fig. 10. Modeling $\hat{S}_{\text{VQ}}(f)$ of (8) as a decreasing exponential.

value with the actual $\hat{S}_{\text{VQ}}(f)$ curve. Suitable approximations were made, as $f_c \ll f_{tq}$, to finally obtain $b \approx 2$ and $a \approx 0.1 f_p$. The entire process is shown in Fig. 10 and results in

$$\hat{\hat{S}}_{\text{VQ}}(f) = \frac{0.1 f_p}{f^2} = \frac{0.63 A f_0}{f^2}. \tag{22}$$

It should be noted here that the correction to ignore the noise tone at f_0 has not been applied as it caused little difference in this approximation. Replacing $S_{\text{VQ}}(f)$ and P_{VQ} in (20) with their approximations from (22) and (14) respectively, we get

$$\hat{P}_Q = \hat{P}_{\text{VQ}} + \frac{1.26 Ac}{c_{tq}^2} \sum_{m=1}^{\infty} \frac{1}{m^2} \tag{23}$$

where $\hat{P}_{\text{VQ}}$ can be easily calculated from (15) instead of (14) for the typical case of $f_c \ll f_p$. Finally, the approximated $\widehat{\text{SNR}}$ can be computed as $\widehat{\text{SNR}} = 10 \log_{10}(2^{2n-3}/\hat{P}_Q)$.

Fig. 9 compares $\widehat{\text{SNR}}$ with real SNR of (21) as c_{tq} varies, for several typical values of n and $c = 3.2$. It shows generally good agreement between approximated $\widehat{\text{SNR}}$ and real SNR for typical values of c_{tq}. However, when c_{tq} is sufficiently smaller than h_p (empirically estimated as $c_{tq} < h_p/2$), a large portion of the first noise PSD segment ($\leq h_p$) is aliased back to itself and results in SNR approximation inaccuracy. This is because for higher values of n, more nonuniformly sampled points will be generated and the time intervals between them will be reduced. In such cases, SNR should be determined from numerical simulations of (21) instead of the analytical equation for $\widehat{\text{SNR}}$. This is why the plots for $\widehat{\text{SNR}}$ start from $h_p/2$ in Fig. 9.

E. Comparison With Uniform Sampling Scheme

As the proposed NUS ADC architecture nonuniformly samples the analog input based on level-crossing events, its instantaneous sampling rate varies with the characteristics of the input signal, e.g., amplitude and frequency, and the number of levels in the quantizer. For example, the average sampling rate of a full-swing sinusoidal input with 3-bit voltage quantizer is seven times the Nyquist sampling rate. We define this ratio as average oversampling ratio (OSR_{avg}) in the context of this paper. We then compare SNR of the NUS ADC with that of the conventional uniform sampling ADCs that generate the same average sampling rate. To provide a more comprehensive comparison, we consider the conventional oversampling ADCs with and without noise shaping. A numerical simulation with a range of voltage quantizer bits and fixed time quantization accuracy is performed on the NUS ADC using ZOH interpolation. The SNR improvement, computed from DC to the 2nd Nyquist zone (twice the input frequency), over different uniform oversampling ADCs is plotted in Fig. 11. It shows more improvement for the lower number of voltage quantizer bits. When compared to higher-order delta-sigma ADCs, the SNR improvement diminishes for higher number of voltage quantizer bits. Note that there is underlying implementation overhead for both NUS ADC and delta-sigma ADCs in the regime of higher bit-number voltage quantizers. For example, higher average sampling rate requires higher asynchronous data capture for the NUS ADC, while in delta-sigma ADCs it demands operational amplifiers with a few times higher gain-bandwidth product compared to the sampling rate for proper output settling. As a result, for a more practical hardware implementation of NUS ADC, the region of interest lies in the lower bit-number voltage quantizer regime, e.g., the silicon prototype in [31] uses only a 4-bit voltage quantizer.

In addition, a uniform sampling ADC should constantly sample at the maximal rate regardless of the input characteristics, thereby providing less flexibility, while the NUS ADC can automatically adjust its instantaneous sampling rate according to input signal. It is challenging to vary the sampling clock frequency based on input signal in real time for a uniform sampling ADC.

F. Design Considerations and Limitations

While the focus of this paper is to explore theoretical bounds of the proposed NUS ADC architecture, some practical design considerations and examples as discussed in [31] and [32] are summarized here for completeness. First of all, in a representative embodiment, the number of comparators increases exponentially with the number of voltage quantizer bits (similar to the conventional flash ADC architectures) and the accuracy

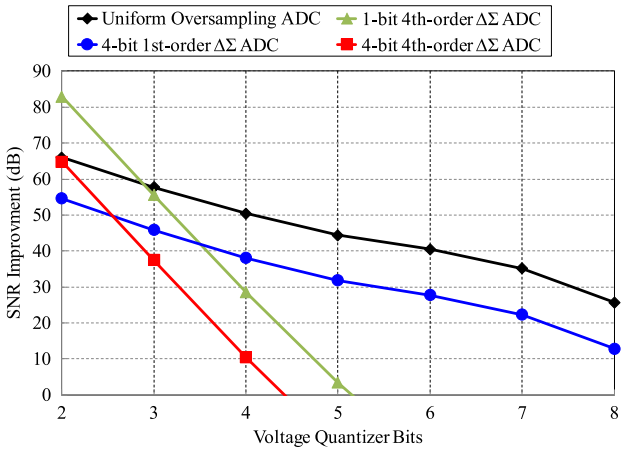


Fig. 11. SNR improvement between the NUS ADC with time quantizer accuracy of $c_{tq} \sim 9\,900$ and different uniform oversampling ADCs given the same average sampling rate.

of voltage quantization levels can be limited by manufacture variability. Therefore, in applications requiring high dynamic range, a comparator offset calibration technique can be applied [31]. Additionally, the increased voltage quantization levels shorten the time between nonuniform samples, i.e., it increases the maximum instantaneous sampling rate. Parallel processing on these nonuniform samples for each voltage level can be utilized to achieve high throughput [17], in this case, instantaneous sampling rate can be up to 45 GS/s. Nevertheless, these factors impose an upper limit of the voltage quantizer resolution in practical implementation. On the other hand, the time quantization resolution should scale with maximum input frequency for a given reconstruction fidelity. For a given time quantization accuracy, this imposes an upper limit on the signal bandwidth. In addition, aside from the quantization noise which is defined by the time quantizer resolution, the time-measurement precision depends on several other factors such as clock jitter and the differential nonlinearity (DNL) of the quantizer. Note that technology scaling generally improves time accuracy. In current state-of-the-art hardware, 1-ps time quantization [21] has already been demonstrated. The achievable signal bandwidth and resolution is expected to further improve as technology advances thanks to increasing device intrinsic speed.

IV. Proposed Digital Anti-Aliasing Filter

One unique feature of the proposed NUS ADC architecture is the ability to perform AA filtering in the digital domain due to alias-free sampling. Also, the same digital AA filter can be used to remove quantization noise and yield SNR improvement over conventional uniform sampling ADCs, as shown by the NUS ADC SNR plots in Fig. 11. A reconfigurable digital AA filter algorithm using nonuniform samples is thus proposed that emulates an analog filter response by computing the filter output using the integral of an ideal analog impulse response [33]. In this section, the filter algorithm is derived assuming ZOH interpolation for the input signal and is then extended to higher order interpolations and different filter responses.

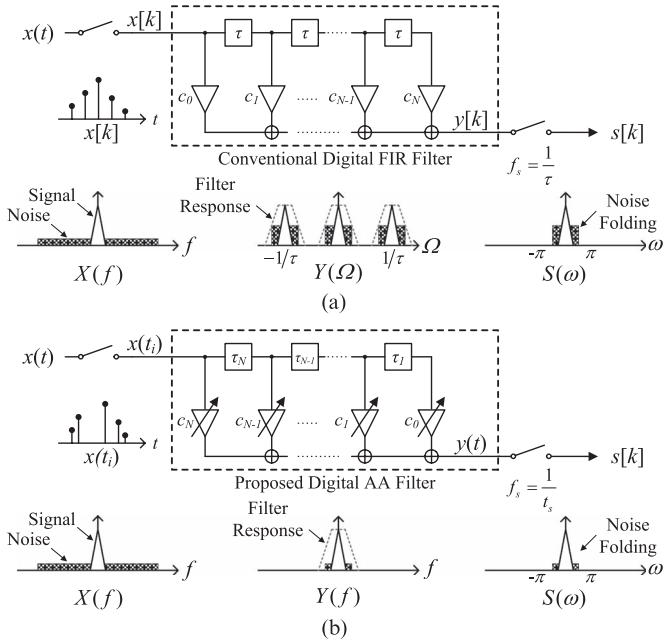


Fig. 12. (a) Conventional digital FIR filter. (b) Proposed digital AA filter.

A. High-Level Concept

Fig. 12 illustrates the proposed filter algorithm for digital AA filtering. We examine the case where the analog input is composed of the desired signal component (white triangle) and the band-limited noise (shaded box) and observe the output SNR. In the case of a conventional digital FIR filter, the spectrum aliasing due to fixed tap delay causes noise folding.

Our proposed digital filter algorithm constructs a time-varying, signal-dependent FIR filter whose tap delay matches the time gap of nonuniform samples. The filter response does not repeat at integer multiples of 2π, i.e., it is equivalent to an analog filter. Together with the alias-free property of nonuniform sampling, the output SNR matches that of analog AA filters. Real-time computation of filter coefficients can be implemented via memory-based DSP to minimize cost. Moreover, filter computation occurs only at the signal Nyquist rate instead of the nonuniform sampling rate, which leads, along with ease of reconfigurability of the filter in the digital domain, to a more flexible platform compared to conventional analog AA filters.

B. Proposed Filter Algorithm

In this section, the following annotations are used for filter algorithm derivations: the analog input signal to be filtered is given in the time domain and denoted by $x(t)$. The desired filter transfer function is $H(\omega)$ in the frequency domain, and its impulse response is $h(t)$. A continuous-time analog filtering process can be represented mathematically as the convolution of $x(t)$ with $h(t)$, as shown

$$y(t) = \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau \tag{24}$$

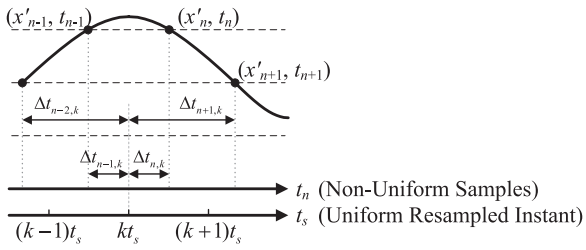


Fig. 13. Time-domain view of nonuniform output samples.

where

$$h(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} H(\omega) e^{j\omega t} d\omega. \tag{25}$$

While $h(t)$ can be any arbitrary impulse response designed to achieve any desired attenuation profile, an ideal brick-wall low-pass filter with corner frequency $\omega_c = 2\pi f_c$ will be considered here as a representative case. Therefore, the time domain impulse response is the normalized sinc function

$$h(t) = \frac{\omega_c}{\pi} \text{sinc}\left(\frac{\omega_c}{\pi} t\right). \tag{26}$$

The convolution in (24) can be rewritten as the sum of integral sections from t_n to t_{n+1} as

$$y(t) = \sum_{n=1}^{\infty} \int_{t_n}^{t_{n+1}} x(\tau) \frac{\omega_c}{\pi} \text{sinc}\left(\frac{\omega_c}{\pi}(t-\tau)\right) d\tau \tag{27}$$

where t_n is the time instant of the nth level-crossing point as shown in Fig. 13.

Using ZOH reconstruction, the voltage quantizer output has discrete amplitudes and remains constant between level-crossing points. Therefore, the amplitude of $x(\tau)$ in each t_n to t_{n+1} interval is a constant value, x_n, which is with half LSB shifted from x'_n and can be separated from the convolution integral. A change of variable is performed to reference all t_n values to t by setting $t' = \tau - t$, $\Delta t_n = t_n - t$, and $\Delta t_{n+1} = t_{n+1} - t$, resulting in

$$y(t) = \sum_{n=1}^{\infty} x_n \int_{\Delta t_n}^{\Delta t_{n+1}} \frac{\omega_c}{\pi} \text{sinc}\left(\frac{\omega_c}{\pi} t'\right) dt'. \tag{28}$$

In the real implementation, the filter duration should be finite in time to avoid using an infinite number of nonuniform samples, i.e., restricted to the set of $t_n \forall\, n : |\Delta t_n| \le t_d$. Thus, the time duration of the filter is $2t_d$. To achieve sharper rolloff and better stopband attenuation, the impulse response $h(t)$ is multiplied by a nonrectangular windowing function $w(t)$. Using the Hann window centered at $t = 0$, we get

$$w(t) = \frac{1}{2}\left[1 + \cos\left(\frac{\pi t}{t_d}\right)\right]. \tag{29}$$

On including $w(t)$ in the convolution integral, (28) can be rewritten as

$$y(t) = \sum_n x_n \int_{\Delta t_n}^{\Delta t_{n+1}} \frac{\omega_c}{2\pi} \text{sinc}\left(\frac{\omega_c}{\pi} t'\right) \left[1 + \cos\left(\frac{\pi t'}{t_d}\right)\right] dt'$$
$$\forall\, n : |\Delta t_n| \le t_d. \tag{30}$$

According to (30), the sinc and cosine functions are completely decoupled from the input and the integral can be evaluated and represented using the sine-integral function, $\text{Si}(x)$, defined by

$$\text{Si}(x) = \int_0^x \frac{\sin t}{t} dt. \tag{31}$$

On performing the integration of (30) and applying limits, we get

$$\begin{aligned} y(t) = \sum_n \frac{x_n}{4\pi} & \times \Bigg\{ 2\left[\text{Si}(\omega_c \Delta t_{n+1}) - \text{Si}(\omega_c \Delta t_n)\right] \\ & + \left[\text{Si}\left(\left(\omega_c + \frac{\pi}{t_d}\right)\Delta t_{n+1}\right) - \text{Si}\left(\left(\omega_c + \frac{\pi}{t_d}\right)\Delta t_n\right)\right] \\ & + \left[\text{Si}\left(\left(\omega_c - \frac{\pi}{t_d}\right)\Delta t_{n+1}\right) - \text{Si}\left(\left(\omega_c - \frac{\pi}{t_d}\right)\Delta t_n\right)\right] \Bigg\} \\ & \forall\, n : |\Delta t_n| \le t_d. \end{aligned} \tag{32}$$

Although the computations utilize nonuniform samples, the proposed filter algorithm is only evaluated at the uniformly resampled time instants in order to be processed by a synchronous digital signal processor. The resampled output after filtering can be computed by

$$s[k] = y(kt_s) = \sum_n x_n \cdot g_n \quad \forall\, n : |\Delta t_{n,k}| \le t_d \tag{33}$$

where

$$\Delta t_{n,k} = t_n - kt_s \tag{34}$$

g_n is the term inside the curly brackets of (32) divided by 4π, k is a positive integer, and t_s is the inverse of the resampling frequency f_s. Equation (33) can be viewed as a time-varying, signal-dependent FIR filter, where the tap delays and weights are dynamically changing as a function of nonuniform time instants relative to the resampling time, kt_s. This is key to the alias-free operation. With infinite time quantization accuracy and time duration of the filter, (28) is equivalent to (24) except that $x(\tau)$ is replaced with a ZOH representation of the input. Therefore, the filter output $s[k]$ is equivalent to the sampled output of the continuous-time convolution between the input signal and the analog filter response.

To validate the frequency response of the proposed AA filter, band-limited white noise with frequency up to $2f_s$ and peak less than full-scale is used as a test input signal, and an 8-bit ideal nonuniform sampling ADC is simulated with a very fine time quantization step, such that $t_{tq} \ll t_s$. The corner frequency of

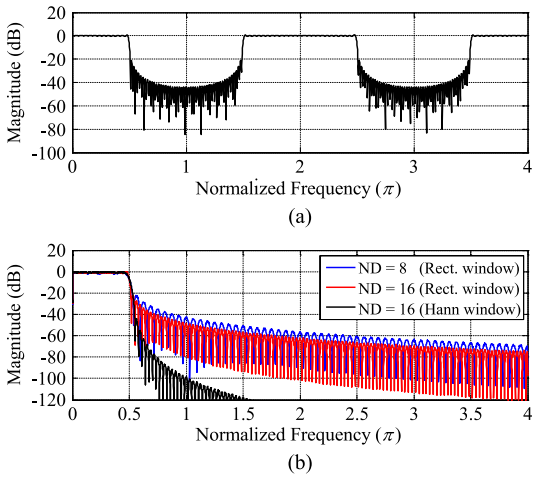


Fig. 14. Filter response of (a) conventional digital FIR filter and (b) proposed digital AA filter with an input of band-limited white noise up to $2f_s$ and filter corner at $0.25f_s$.

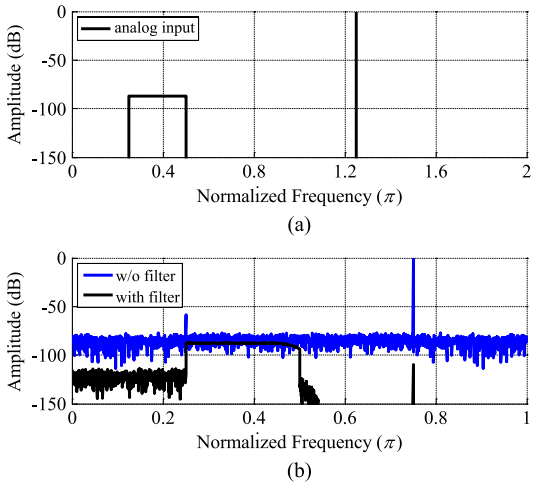


Fig. 15. Power spectrum of (a) analog input and (b) resampled output with and without the proposed digital AA filter.

the low-pass filter is set to $0.25f_s$ and simulation results are shown in Fig. 14. To illustrate the effect of finite time duration of the filter, t_d is normalized to π/ω_c and quantified as

$$ND = \frac{t_d}{\left(\frac{\pi}{\omega_c}\right)} = 2f_c t_d. \tag{35}$$

The term ND is the number of zero crossings of the sinc impulse response and is a measure of the sharpness of the filter. Higher values of ND lead to narrower transition bands. The windowed filter responses utilizing a Hann window are shown in Fig. 14 as representative examples, where the input is band-limited white noise up to $0.5f_s$ and the filter corner is at $0.25f_s$ with ND set to 16. Depending on the specifications, proper time duration of the filter and window function can be chosen to create a desired filter response. This proves the flexibility of the proposed filter algorithm.

C. Alias-Free Property Validation

A unique property of the proposed filter algorithm is that it attenuates any out-of-band signal before it folds into the Nyquist band due to uniform resampling, i.e., AA filtering takes place. To validate this alias-free property, we perform a blocker test in the simulation, i.e., a modulated input signal along with an unwanted blocker. The filter response is configured with a large t_d and Hann window to minimize the effect of finite time duration and a fine time accuracy is set to reduce time quantization noise. The simulation setup is the same as in Fig. 14, except the band-limited white noise is now located in the first Nyquist zone along with a 60-dB higher blocker at $0.625f_s$. The overall signal amplitude is adjusted to be within the full scale of the NUS ADC to avoid any amplitude clipping, i.e., ideal automatic gain control (AGC) is assumed. The final resampled outputs with and without the proposed AA filter are compared and their power spectra are plotted in Fig. 15. We observe that both the blocker and voltage quantization noise can be attenuated significantly via the proposed filter algorithm before being aliased.

D. Reconfigurable Signal Reconstruction

Thus far, we have assumed ZOH interpolation for the signal reconstruction. The voltage quantization noise due to deviation of the term $x(\tau)$ in (24) generate harmonic tones, as discussed in Section III-A. In the case of a relaxed signal reconstruction requirement, ZOH is a reasonable choice to minimize the computation; in addition, the voltage quantizer can be reconfigured into fewer levels to not only minimize the implementation cost but also reduce nonuniform samples for less digital signal post-processing.

In the case of more stringent signal reconstruction requirements, it is possible to reduce the voltage quantization noise by using higher-order interpolations combined with the proposed filter algorithm to achieve a higher quality of the reconstructed signal, as illustrated in Fig. 5. As shown in Fig. 12, interpolation is conceptually done before the filtering. In the real implementation, we propose embedding the interpolation as part of the filter algorithm without calculating additional interpolated points between the adjacent level-crossing samples. As a result, the memory and computation costs can be reduced. The only overhead is calculating the coefficients of the interpolation function of each section when a new level-crossing sample is generated. The output is evaluated at the resampled instants using the existing nonuniform samples. In the following derivations, a generic second-order piecewise polynomial is used as an example to approximate the input signal between adjacent nonuniform samples, so the input signal can be written as

$$x(t) = \sum_n x_n(t) \tag{36}$$

and each function $x_n(t)$ is a piecewise polynomial defined on $[t_n, t_{n+1}]$, where $n = 0, 1, 2, \ldots$. For a second-order polynomial, we have

$$x_n(t) = a_n t^2 + b_n t + c_n \tag{37}$$

where a_n, b_n, and c_n are the coefficients defined on $[t_n, t_{n+1}]$ and can be calculated via existing numerical approaches such

as Lagrange interpolation. Therefore, (30) can be modified as

$$y(t) = \sum_n \int_{\Delta t_n}^{\Delta t_{n+1}} \left\{ \left(a_n(t'+t)^2 + b_n(t'+t) + c_n\right) \times \frac{\omega_c}{\pi} \mathrm{sinc}\left(\frac{\omega_c}{\pi} t'\right) \left[1 + \cos\left(\frac{\pi t'}{t_d}\right)\right] \right\} dt' \quad \forall n : |\Delta t_n| \le t_d. \tag{38}$$

After some algebraic manipulation, the resampled output $s[k]$ can be represented as

$$s[k] = y(kt_s) = A_k + B_k + C_k \quad \forall n : |\Delta t_{n,k}| \le t_d \tag{39}$$

which is the combination of three terms originating from integrating t'^2, t', and the constant term in (38), and involves sine and cosine functions in addition to Si. When $a_n = b_n = 0$, the equation reduces to the ZOH case, where $A_k = B_k = 0$ and C_k is equal to the right-hand side of (33). Similarly, first-order interpolation can be applied when $a_n = 0$. Different embedded interpolation options provide another degree of freedom to the proposed filter algorithm.

E. Filter Response Reconfigurability

Up to this point, the derivations have focused on the low-pass filter response. However, they can be extended to other responses, such as band-pass filtering, due to digital reconfigurability. This is particularly useful for subsampling applications [34], [35]. Conventionally, in order to perform subsampling, an ADC relies on an analog band-pass filter centered at the carrier frequency with sharp frequency response or samples at higher than Nyquist rate to avoid any undesirable out-of-band components from being aliased on top of desired signals. This design constraint limits the practicability of subsampling with uniform sampling. Benefiting from the alias-free property, the proposed digital AA filter is able to remove any out-of-band components before subsampling. In addition to undesired signals presented in front of the ADC, it can also relax the noise requirement of the quantizer using subsampling and yield an improved value of SNR. However, when a baseband signal of one-sided bandwidth B is located at a center frequency f_0, since the average sampling rate is proportional to $B + f_0$, an increased average sampling rate will increase design costs as described in Section III-F. Therefore, the upper limit of the passband signal frequency for subsampling should be bound, similar to signal bandwidth considerations.

Considering an ideal brick-wall band-pass filter with corner frequencies at ω_H and ω_L, the output $S_{\mathrm{BPF}}[k]$ can be given as

$$s_{\mathrm{BPF}}[k] = s_{\mathrm{LP}}[k]\big|_{\omega_C=\omega_H} - s_{\mathrm{LP}}[k]\big|_{\omega_C=\omega_L} \tag{40}$$

where $S_{\mathrm{LP}}[k]$ is the low-pass filter output obtained from (39) with the desired interpolation order. To validate the band-pass filter response, a NUS ADC with a band-limited signal along with two adjacent 60-dB higher blockers is simulated and the subsampled output spectrum is shown in Fig. 16. The proposed filter with ZOH and $ND = 16$ yields more than 60-dB attenuation on blockers which would otherwise require an 11th-order

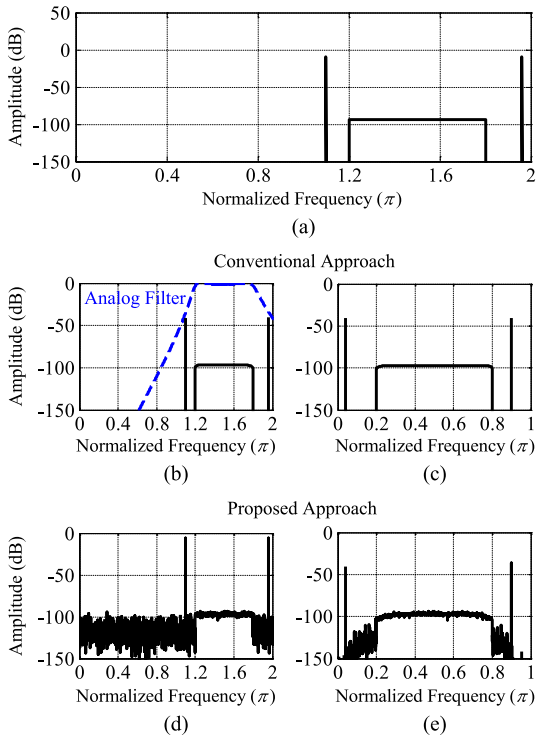


Fig. 16. (a) Spectrum of the analog input where two blockers located at $0.55f_s$ and $0.98f_s$, and band-limited signal between $0.6f_s$ and $0.9f_s$. (b) and (c) Blockers attenuated by an 11th-order Butterworth band-pass filter and subsampled by an ideal uniformly sampled ADC. (d) Reconstructed signal before proposed digital AA filter. (e) Subsampled and filtered output.

Butterworth bandpass filter when implemented using the conventional analog approach. ND values can be flexibly adjusted depending on the requirements, giving equivalent 3rd-order and 20th-order Butterworth band-pass filters for ND equal to 4 and 32, respectively.

As an illustration of relaxing the noise requirements for the quantizer, we examine a NUS ADC case using an 8-bit voltage quantizer to subsample a sinusoidal input at $0.75f_s$ without any amplitude clipping in the presence of additive white Gaussian noise (AWGN). This additive noise can be caused by the intrinsic circuit noise of the voltage quantizer implementation. With noise of standard deviation of 0.85 LSB referred at the input, the uniform sampling ADC achieves 40 dB SNR after subsampling due to aliasing of the out-of-band noise, as shown in Fig. 17(a). When the proposed NUS ADC architecture with digital AA band-pass filter is utilized (corners at $f_s/2$ and f_s), out-of-band noise can be filtered because of an average sampling rate higher than f_s resulting in SNR improvement of 29 dB as shown in Fig. 17(b).

F. One Embodiment of the Digital AA Filter

Fig. 18 shows a possible hardware implementation of the proposed digital AA filter algorithm using ZOH. A first-in-first-out (FIFO) buffer can be used to store the incoming nonuniform samples and the final filter output rate must only satisfy the Nyquist rate, i.e., twice the signal bandwidth. Furthermore, the desired filter responses evaluated at y, such as sine-integral, can be pre-calculated and stored in lookup tables to reduce

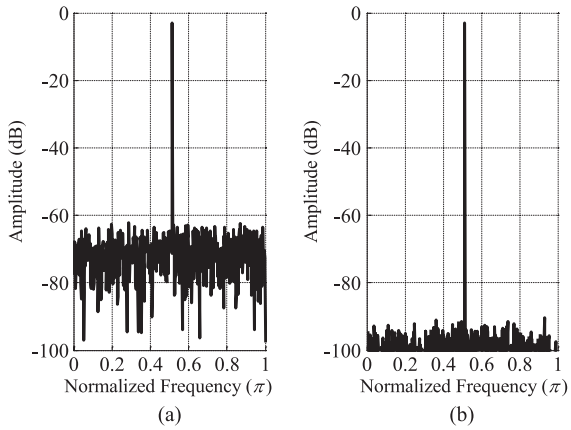


Fig. 17. Subsampling for a sinusoid input at $0.75f_s$. (a) Uniform sampling ADC. (b) Proposed NUS ADC architecture with ZOH interpolation, Hann windowed, and ND set to 32.

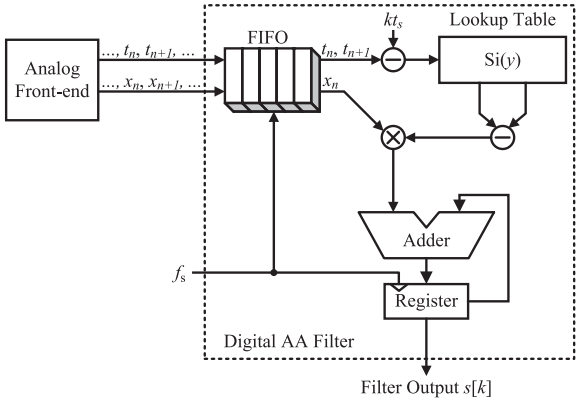


Fig. 18. Implementation of proposed digital AA filter.

computation cost in real time. Since y is bounded between 0 and t_d, lookup table size can be optimized for specific values of ω_c and ND. For each filter output time instant kt_s, Δt_n, and Δt_{n+1} are computed for all nonuniform samples within the filter duration from $kt_s - t_d$ to $kt_s + t_d$. These are plugged into the filter response values read from the lookup tables. The values are subtracted and multiplied with the incoming nonuniform samples x_n and a final accumulator computes the filter output at a rate of $f_s(= 1/t_s)$.

V. Conclusion

A NUS ADC architecture with embedded digital AA filter has been proposed to utilize both voltage and time quantization, which aims to relax analog AA filter requirements, and seamlessly interface with synchronous DSPs. Errors in this architecture are modeled as voltage and time quantization noise in order to analyze performance, understand the lower bound of the entire system and tradeoff with several design parameters. It has been found that the worst-case SFDR varies from $\sim$20 to 70 dB for a 2- to 8-bit voltage quantizer, given the simplest interpolator, i.e., ZOH. Moreover, SNR improves by 9 dB for every added bit in voltage quantization, given the same digital AA filter bandwidth and sufficiently fine time quantization resolution. The proposed ADC architecture features an adaptive sampling rate according to the incoming signal and provides reconfigurable alias-free anti-aliasing filtering in the digital domain. It provides a flexible way of performing analog-to-digital conversion and filtering instead of an optimized solution for a fixed sampling rate data conversion. Lastly, the proposed NUS ADC architecture is expected to benefit from technology scaling, as increasing device speeds will continue to improve time quantization resolution.

Acknowledgment

The authors would like to thank Dr. M. Rich for funding support and discussions.

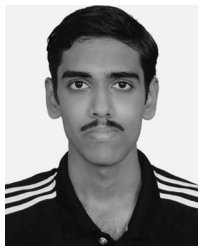
References

[1] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE J. Solid-State Circuits*, vol. 42, pp. 954–966, May 2007.
[2] A. Bourdoux, J. Craninckx, A. Dejonghe, and L. V. der Perre, "Receiver architectures for software-defined radios in mobile terminals: The path to cognitive radios," in *Proc. IEEE Radio Wireless Symp.*, Jan. 2007, pp. 535–538.
[3] C. T. C. Nguyen, "MEMS-based RF channel selection for true software-defined cognitive radio and low-power sensor communications," *IEEE Commun. Mag.*, vol. 51, no. 4, pp. 110–119, Apr. 2013.
[4] Y. S. Poberezhskiy and G. Y. Poberezhskiy, "Sampling and signal reconstruction structures performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 118–129, Jan. 2004.
[5] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. Abidi, "Analysis of first order anti-aliasing integration sampler," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 10, pp. 2994–3005, Nov. 2008.
[6] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. Abidi, "A second-order antialiasing prefilter for a software-defined radio receiver," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 7, pp. 1513–1524, Jul. 2009.
[7] Y. S. Poberezhskiy and G. Y. Poberezhskiy, "Impact of the sampling theorem interpretations on digitization and reconstruction in SDRs and CRs," in *Proc. IEEE Aerospace Conf.*, Big Sky MT, USA, Mar. 1–8, 2014, pp. 1–20.
[8] M. Z. Win and R. A. Scholtz, "Impulse radio: How it works," *IEEE Commun. Lett.*, vol. 2, no. 2, pp. 36–38, Feb. 1998.
[9] C. Duan, P. Orlik, Z. Sahinoglu, and A. Molisch, "A noncoherent 802.15.4a UWB impulse radio," in *Proc. IEEE Int. Conf. Ultra-Wide-Band*, Sep. 2007, pp. 146–151.
[10] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 μW wake-up receiver with−72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.
[11] W. Tang *et al.*, "Continuous time level crossing sampling ADC for bio-potential recording systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 6, pp. 1407–1418, Jun. 2013.
[12] F. Marvasti, Ed. *Nonuniform Sampling: Theory and Practice*. New York, NY, USA: Springer-Verlag, 2001.
[13] N. Sayiner, H. V. Sorensen, and T. R. Viswanathan, "A level-crossing sampling scheme for A/D conversion," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 43, pp. 335–339, Apr. 1996.
[14] C. Vezyrtzis and Y. Tsividis, "Processing of signals using level-crossing sampling," in *Proc. IEEE Int. Symp., Circuits Syst.*, 2009, pp. 2293–2296.
[15] K. Guan and A. C. Singer, "A level-crossing sampling scheme for non-bandlimited signals," in *Proc. IEEE Int. Conf., Acoust, Speech Signal Process.*, vol. 3, 2006, pp. 381–383.
[16] Y. Tsividis, "Digital signal processing in continuous time: A possibility for avoiding aliasing and reducing quantization error," in *Proc. IEEE Int. Conf., Acoust., Speech Signal Process.*, vol. 2, 2004, pp. 589–592.
[17] M. Kurchuk, C. Weltin-Wu, D. Morche, and Y. Tsividis, "GHz-range continuous-time programmable digital FIR with power dissipation that automatically adapts to signal activity," in *Proc. ISSCC Dig. Tech. Papers*, 2011, pp. 232–234.

[18] E. Allier, G. Sicard, L. Fesquet, and M. Renaudin, "A new class of asynchronous A/D converters based on time quantization," in *Proc. 9th Int. Symp. Asynchronous Circuits Syst.*, 2003, pp. 196–205.
[19] F. Aeschlimann, E. Allier, L. Fesquet, and M. Renaudin, "Asynchronous FIR filters: Towards a new digital processing chain," in *Proc. 10th Int. Symp. Asynchronous Circuits Syst.*, 2004, pp. 198–206.
[20] R. B. Staszewski *et al.*, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2278–2291, Dec. 2004.
[21] P. Keranen, "Wide-range time-to-digital converter with 1-ps single-shot precision," *IEEE Trans. Instrum. Measur.*, vol. 60, pp. 3162–3172, Sep. 2011.
[22] J. L. Yen, "On nonuniform sampling of bandwidth-limited signals," *IRE Trans. Circuit Theory*, pp. 251–257, Dec. 1956.
[23] M. Malmirchegini and Marvasti, "Performance improvement of level-crossing sampling," in *Proc. IEEE Int. Conf. Telecommun. Malaysia Int. Conf. Commun.*, May 2007, pp. 438–441.
[24] T. Claasen and A. Jongepier, "Model for the power spectral density of quantization noise," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 29, pp. 914–917, Apr. 1981.
[25] A. G. Clavier, P. F. Panter, and D. D. Grieg, "Distortion in a pulse count modulation system," *AIEE Trans.*, vol. 66, pp. 989–1005, Jan. 1947.
[26] W. R. Bennett, "Spectra of quantized signals," *Bell Syst. Tech. J.*, vol. 27, pp. 446–472, Jul. 1948.
[27] N. M. Blachman, "The intermodulation and distortion due to quantization of sinusoids," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. ASSP-33, pp. 1417–1426, Dec. 1985.
[28] M. Alink *et al.*, "Spurious-free dynamic range of a uniform quantizer," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 6, pp. 434–438, Jun. 2009.
[29] G. W. Morgenthaler and H. Reismann, "Zeros of first derivatives of Bessel functions of the first kind, $J_n'(\mathrm{x})$, $21 \leq n \leq 51$, $0 \leq x \leq 100$," *J. Res. National Bureau Standards-B. Mathematics Mathematical Physics*, vol. 67B, pp. 181–183, Jul.–Sep. 1963.
[30] P. Z. Peebles, Jr., "Angle modulation," in *Communication System Principles*. Reading, MA, USA: Addison-Wesley, 1976.
[31] T.-F. Wu, C.-R. Ho, and M. Chen, "A flash-based nonuniform sampling ADC enabling digital anti-aliasing filter in 65 nm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2015, pp. 1–4.
[32] K. Kozmin, J. Johansson, and J. Delsing, "Level-crossing ADC performance evaluation toward ultrasound application," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 8, pp. 1708–1719, Aug. 2009.
[33] D. Hand and S.-W. M. Chen, "A nonuniform sampling ADC architecture with embedded alias-free asynchronous filter," in *Proc. IEEE GLOBECOM*, Anaheim, CA, USA, Dec. 2012, pp. 3707–3712.
[34] S.-W. M. Chen and R. W. Brodersen, "A subsampling radio architecture for ultrawideband communications," *IEEE Trans. Signal Process.*, vol. 55, pp. 5018–5031, Dec. 2007.
[35] A. M. A. Ali *et al.*, "A 16 b 250 MS/s IF-sampling pipelined A/D converter with background calibration," in *Proc. IEEE ISSCC Dig. 2010*, pp. 292–293.
[36] I. Bilinskis, *Digital Alias-Free Signal Processing*. West Sussex, U.K.: Wiley, 2007.

Tzu-Fan Wu received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 2004 and the M.S. degree from University of California, Los Angeles, in 2008, all in electrical engineering. He is currently pursuing the Ph.D. degree in electrical engineering at University of Southern California.

From 2009 to 2013, he was with Metanoia Communications, Hsinchu, Taiwan, working on mixed-signal circuits for various wireline communication systems. His research interests include the development of high-speed and asynchronous data converters for low-power and wireless applications.



Sourya Dey received the B.Tech degree in instrumentation engineering from the Indian Institute of Technology, Kharagpur, India, in 2014. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Southern California, where he is a Viterbi Graduate School Fellow.

His research interests include neural networks and asynchronous circuit design.

Mike Shuo-Wei Chen (M'06) received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1998 and the M.S. and Ph.D. degrees from the University of California (UC), Berkeley, in 2002 and 2006, all in electrical engineering.

He is currently an Assistant Professor in the Electrical Engineering Department, University of Southern California, and holds the Colleen and Roberto Padovani Early Career Chair position. From 2001 to 2006, he was a Graduate Research Assistant at Berkeley Wireless Research Center, working on mixed-signal circuits, ultra-wideband, digital baseband and ASIC implementation. During that time, he proposed and demonstrated the asynchronous SAR ADC architecture, which has been adopted for low-power high-speed analog-to-digital conversion in industry. Since 2006, he has been a member of Analog IC Group at Atheros Communications (now Qualcomm-Atheros), working on mixed-signal and RF circuits for various wireless communication products. After joining the University of Southern California, he leads an analog mixed-signal circuit group, focusing on high-speed low-power data converters, bio-inspired electronics, RF frequency synthesizers, and DSP-enabled analog circuits and systems.

Dr. Chen was the recipient of a National Science Foundation (NSF) Faculty Early Career Development (CAREER) Award and DARPA Young Faculty Award (YFA) in 2014, Analog Devices Outstanding Student Award for recognition in IC design in 2006, and UC Regents' Fellowship at Berkeley in 2000. He also achieved an honorable mention in the Asian Pacific Mathematics Olympiad 1994.