JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

Homework 3

Assigned: June 1, 2021

Due: June 8, 2021, 2:00pm.

Submit a PDF file on Canvas

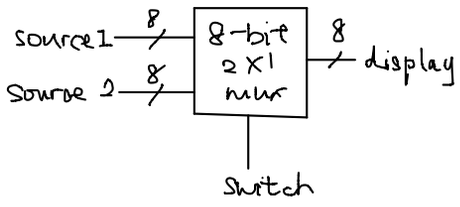
1. Problem 2.65 (5 points)

2.65 Simplify the following equation by using XOR wherever possible: `F = a'b + ab' + cd' + c'd + ac.`

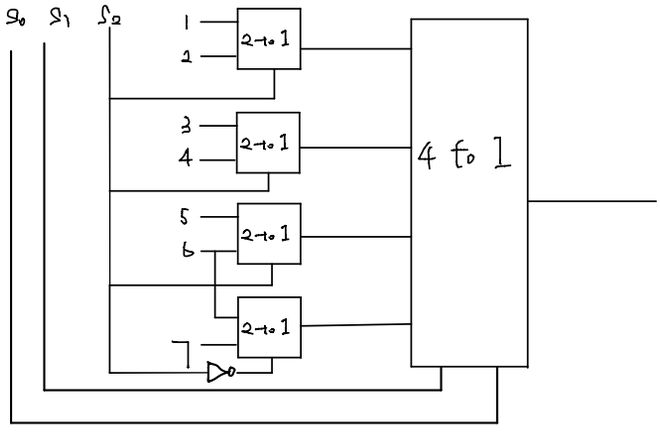
$F = a \oplus b + c \oplus d + ac$

2. Problem 2.75 (20 points)

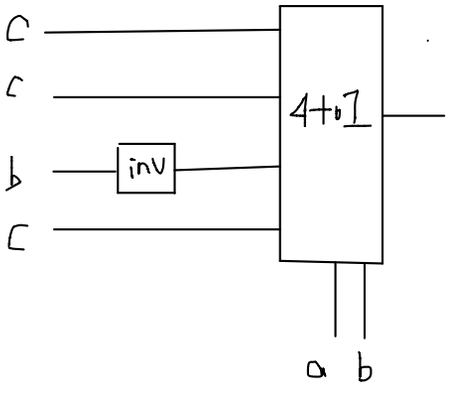
2.75 A video system can accept video from one of two video sources, but can only display one source at a given time. Each source outputs a stream of digitized video on its own 8-bit output. A switch with a single-bit output chooses which of the two 8-bit streams will be passed on a display's single 8-bit input. Create a circuit to connect the two video sources, the switch, and the display. Use at least one mux (a single mux or an *N*-bit mux) or decoder. Use block symbols, each with a clearly defined function, such as "2x1 mux," "8-bit 2x1 mux," or "3x8 decoder"; do not show the internal design of a mux or decoder.



3. Design a 7-to-1 MUX with four 2-to-1 and one 4-to-1 MUXs. Make sure the control signals are clearly connected and labeled. (10 points)

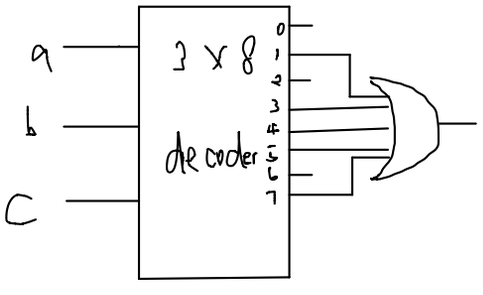


4. Use one 4-to-1 MUX and one inverter to implement a digital circuit for following truth table. (10 points)

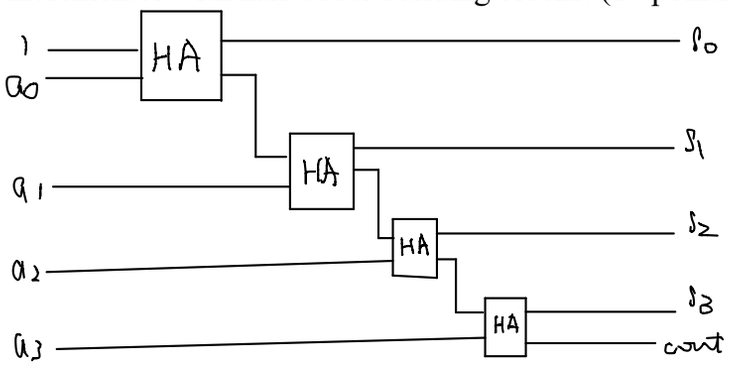


a	b	c	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

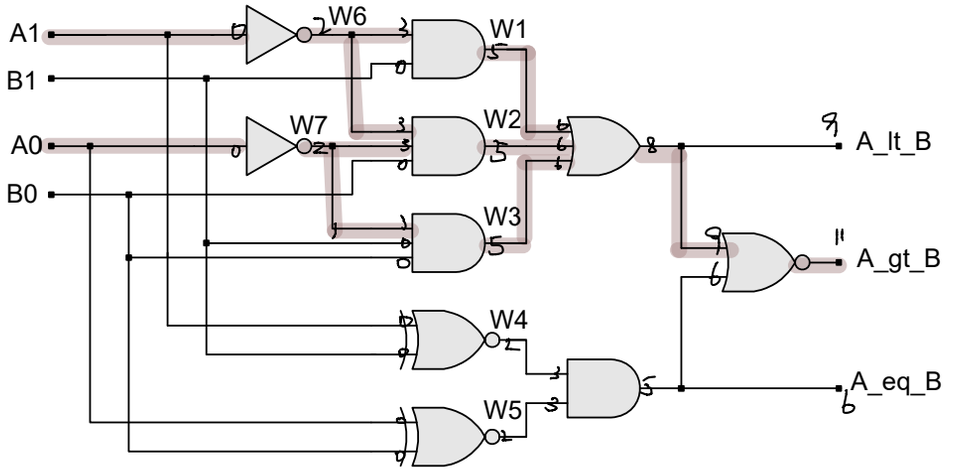
5. Use one 3-by-8 decoder and other components to implement a digital circuit for above truth table. (5 points)



6. An incrementor is a combinational circuit that always adds "1" to the input. Design a 4-bit incrementor with half-adder building blocks. (15 points)

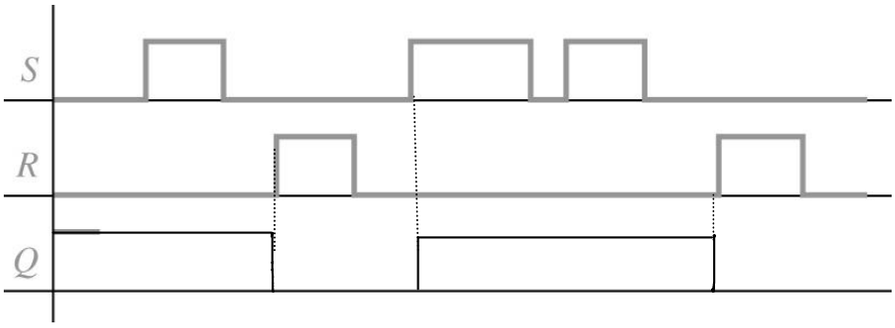


7. Highlight the critical paths of the following circuit. Assume that each gate (including the individual inverters, NOR, and XNOR gates) has a delay of 2 ns and each wire has a delay of 1 ns. (5 points)

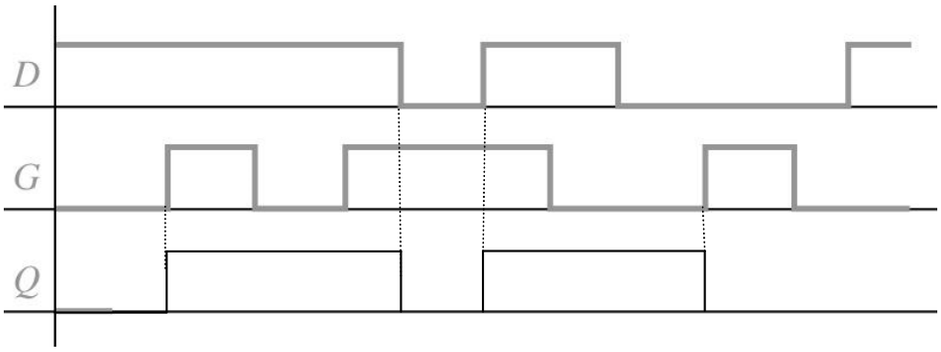


***Note**: For following problems, you may ignore the gate delays when drawing a timing diagram.*

8. Complete the following timing diagram for an SR latch. Assume Q begins at 1. (10 points)



9. Complete the following timing diagrams for a gated D latch. Assume Q begins at 0. (10 points)



10. Complete the following diagrams for the rising-edge triggered D flip-flop. Assume Q begins at 1. (10 points)