

EE 319K Lab1

Deliverables

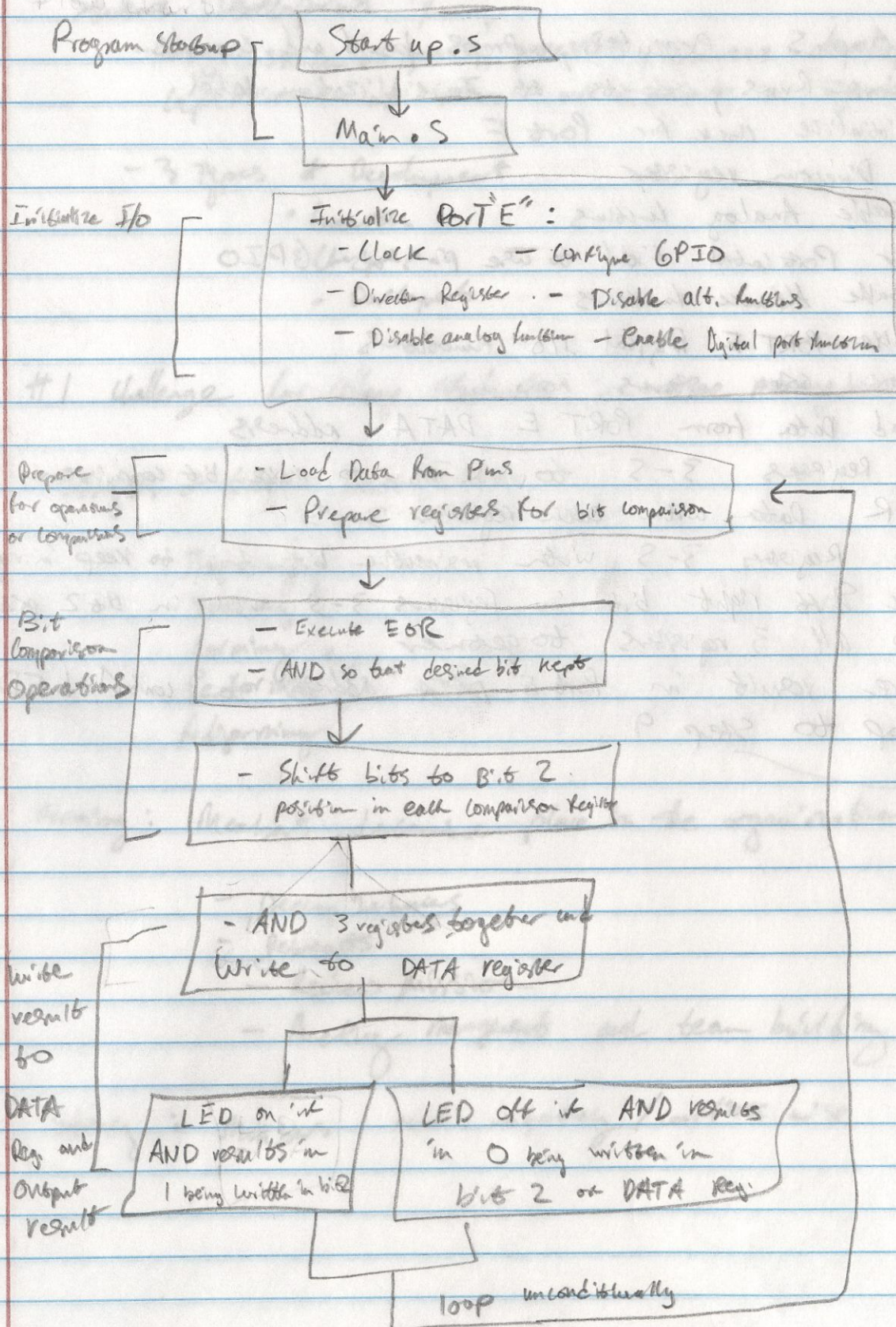
HYDER SHAH

HS25796

2/3/16

Prof. VJ

Flow Chart, Lab 1



Pseudo Code, Lab 1

- 1 Startup.S executed, preps board and commands
- 2 Mains Runs, starts at Initialization label
- 3 Initialize clock for Port E
- 4 Set Direction register
- 5 Disable Analog functions
- 6 Clear Port control field to use pins as GPIO
- 7 Disable Alternate functions
- 8 Enable PORT E Digital I/O Functions.
↓ actual code starts now
- 9 Load Data from PORT E DATA address
- 10 Set Registers 3-5 to x38 to make bit comparison
- 11 EOR Data with each register 3-5
- 12 AND Registers 3-5 with respective bit trying to keep in register
- 13 Logic Shift right bit in Registers 3-5 until in Bit 2 position
- 14 AND all 3 registers together
- 15 Store result in Port E DATA address to control LED
- 16 Loop to Step 9

C:\Keil\EE319KwareSpring2016\Lab1_EE319K_asm\Lab1.uvproj - μVision4

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Logic Analyzer

Registers

Register	Value
Core	
R0	0x400243FC
R1	0x00000004
R2	0x00000000
R3	0x00000004
R4	0x00000004
R5	0x00000020
R6	0x00000000
R7	0x00000000
R8	0x00000000
R9	0x00000000
R10	0x00000000
R11	0x00000000
R12	0x00000000
R13 (SP)	0x20000400
R14 (LR)	0x000002C3
R15 (PC)	0x000002F2
xPSR	0x01000000
Banked	
System	
Internal	
Mode	Thread
Privilege	Privileged
Stack	MSP
States	10639100
Sec	0.66494375
FPU	

main.s Startup.s

```
68 STR R1, [R0]
69 BX LR
70
71 Start
72 BL INIT ; [R1] = R0
73
74
75 LDR R0, =GPIO_PORTE_DATA_R
76 loop LDR R1, [R0] ; LOAD DATA FROM PORT E PINS
77 MOV R3, #0X38 ; STORE X38 VALUE TO PERFORM EXCLUSIVE OR OPERATION TO TURN LED ON OR OFF
78 MOV R4, #0X38
79 MOV R5, #0X38
80 EOR R3, R1, R3
81 AND R3, #0X08 ; KEEP JUST BIT 3
82 EOR R4, R1, R4
83 AND R4, #0X10 ; KEEP JUST BIT 4
84 EOR R5, R1, R5
85 AND R5, #0X20 ; KEEP JUST BIT 5
86 LSR R3, #1 ; LEFT SHIFT EACH OF THE BITS INTO THE BIT 2
87 LSR R4, #2
88 LSR R5, #3
89 AND R3, R4, R3 ; IF EOR RESULTED IN 1 IN EACH BIT POSITION, EACH SWITCH WAS PRESSED, THEREFORE IF ALL SWITCHES PRESSED,
90 ;THREE BITS ANDED TOGETHER AND STORED IN DATA REGISTER TO WRITE LED HIGH (BIT 2 HIGH) AND TURN IT ON
91 AND R3, R5, R3
92 STR R3, [R0]
93 B loop ;REPEAT CHECK FOR SWITCHES
94
95
96 ALIGN ; make sure the end of this section is aligned
97 END ; end of file
```

TEaS Lab 1

Port E Hardware

SW1 SW2 SW3

TM4C123

PE3 PE4 PE5

16 MHz

LED

Port E Registers

DATA: 0x04 PUR: 0x00 LOCK: 0x01

DIR: 0x04 PDR: 0x00 CR: 0xFF

DEN: 0x3C RCGCGPIO: 0x00000010 Clock enabled

Grading Controls

Number from Ed% Grade Score: 100

Copy this to Ed% DIBmeChm

Command

6) All three switches pressed
Pass: All switches pressed has LED on
Done grading. Score is 100

Memory 1

Address: 0x0

0x00000000: 00 04 00 20 6D 02 00 00 71 02 00 00 73 02 00 00 75 02 00 00 77 02 00 00 79 02 00
0x0000001B: 00 00 00 00 00 00 00 00 00 00 00 00 7B 02 00 00 7D 02 00 00 7F 02 00 00 81 02
0x00000036: 00 00 7F 02 00 00 81 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00
0x00000051: 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00
0x0000006C: 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00 00 83 02 00

ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE DEFINE DIR

Simulation tt: 0.66494375 sec L:88 C:1 CAP NUM SCRL OVR RAW

Search the web and Windows 11:12 PM 2/3/2016

```

1  ;***** main.s *****
2  ; Program written by: HYDER SHAD
3  ; Date Created: 1/22/2016
4  ; Last Modified: 2/2/2016 6:38 PM
5  ; Section: THURSDAY 2-3 PM
6  ; Instructor: V. JANAPA
7  ; Lab number: 1
8  ; Brief description of the program
9  ; The overall objective of this system is a digital lock
10 ; Hardware connections
11 ; PE3 is switch input (1 means switch is not pressed, 0 means switch is pressed)
12 ; PE4 is switch input (1 means switch is not pressed, 0 means switch is pressed)
13 ; PE5 is switch input (1 means switch is not pressed, 0 means switch is pressed)
14 ; PE2 is LED output (0 means door is locked, 1 means door is unlocked)
15 ; The specific operation of this system is to
16 ;   unlock if all three switches are pressed
17
18 GPIO_PORTE_DATA_R      EQU    0x400243FC
19 GPIO_PORTE_DIR_R       EQU    0x40024400
20 GPIO_PORTE_AFSEL_R     EQU    0x40024420
21 GPIO_PORTE_DEN_R       EQU    0x4002451C
22 GPIO_PORTE_AMSEL_R     EQU    0x40024528
23 GPIO_PORTE_PCTL_R      EQU    0x4002452C
24 SYSCCTL_RCGCGPIO_R     EQU    0x400FE608
25
26     AREA    |.text|, CODE, READONLY, ALIGN=2
27     THUMB
28     EXPORT  Start
29
30 INIT    ; 1) activate clock for Port E
31     LDR R0, =SYSCCTL_RCGCGPIO_R
32     LDR R1, [R0]
33     MOV R1, #0X10                ;SET BIT 4 HIGH TO ENABLE PORT E CLOCK
34     STR R1, [R0]
35     NOP
36     NOP                ; allow time to finish activating
37     NOP
38
39     ; 2) set direction register
40
41     LDR R0, =GPIO_PORTE_DIR_R    ;SET BIT 2 HIGH FOR PE2 TO BE OUTPUT
42     MOV R1, #0X04
43     STR R1, [R0]
44
45     ; 3) disable analog functionality
46
47     LDR R0, =GPIO_PORTE_AMSEL_R    ; DISABLE ANALOG CAPABILITIES, SOLEY DIGITAL I/O
48     MOV R1, #0x0
49     STR R1, [R0]
50
51     ; 4) configure as GPIO
52
53     LDR R0, =GPIO_PORTE_PCTL_R
54
55     MOV R2, #0x0                ; CLEAR PORT CONTROL FIELD TO SET UP PINS FOR GPIO
56     STR R2, [R0]
57
58     ;5) regular port function
59
60     LDR R0, =GPIO_PORTE_AFSEL_R    ; DISABLE ALT FUNCTIONS FOR BIN BY SETTING BITS TO ZERO
61     MOV R1, #0
62     STR R1, [R0]
63
64     ;6) enable digital port
65
66     LDR R0, =GPIO_PORTE_DEN_R      ; R1 = &GPIO_PORTD_DEN_R
67     MOV R1, #0x3C                ;ENABLE DIGITAL I/O ON PINS 5-2
68     STR R1, [R0]
69     BX LR
70
71 Start
72     BL INIT                ; [R1] = R0

```

```
73
74
75     LDR R0, =GPIO_PORTA_DATA_R
76 loop  LDR R1, [R0] ; LOAD DATA FROM PORT A PINS
77       MOV R3, #0X38 ; STORE 38 VALUE TO PERFORM EXCLUSIVE OR OPERATION TO TURN LED ON OR OFF
78       MOV R4, #0X38
79       MOV R5, #0X38
80       EOR R3, R1, R3
81       AND R3, #0X08 ; KEEP JUST BIT 3
82       EOR R4, R1, R4
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