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EE 460M
TH 2-5 Lab Section

Lab 0 Questions:

1. ModelSim is a Verilog compiler, debugger, and simulator that can show the functionality and operation of hardware designs. The main text window at the bottom of the ModelSim simulator is where the commands to run the simulation, toggle signals, and set values for inputs are entered.
2. Delta cycles are a sort of simulation for a time step without moving forward in actual time. This enable a signal change to propagate out to other logic components that may cause additional signals to change, and these cycles the simulation goes through to propagate the signal are delta cycles. The physical time is not changed during this process. This is done in many cases to guarantee old values are disposed of when new changes in inputs that affect the output are made.
3. A .do file is a plain text file that has a series of commands written in the order they are to be executed. A .do file is useful for quickly running a simulation process automatically without having to re-enter the commands one by one every time. A .do file can be created by simply opening up a plain text file (.txt) and saving the file extension as a .do file. The transcript window can also be saved as a list or text file which can be edited and turned into a .do file later by selecting file->save transcript as…
4. The flow window in Vivado is a main options list where the user can select from editing simulation settings, running a simulation, adding source files, and viewing the synthesized design of the Verilog/HDL code, generating the bitstream to download to a FPGA board and more. The RTL schematic viewer allows the user to see how the Verilog/HDL code has been compiled into the structure of signals and logic components that will produce the outputs as desired. It also shows which signals/components are tied to which particular blocks or lines of code.
5. The XDC file is the Xillinx Design Constraints file which is used to map the signals written in the HDL code to the actual Artix-7 pins and components on the particular FPGA board the user is going to program, in this case the Basys3 FPGA. The bitstream file is created after the HDL design is synthesized and all the signals in the code are mapped to the pins on the FPGA to be programmed. The bit file describes the entire FPGA design and how all the components are wired and set up.
6. It is possible if the two digits happen to be the same digit, but otherwise to display multiple different digits only one digit can be “active” at any instant. The anode and cathodes for the 4 seven segment displays are tied together so to display multiple digits, each one is turned on for a very short period such as 20ms and then off an then the next one is triggered immediately after so

to the human eye it appears as if they are on simultaneously when in reality only one 7-segment is on at a time.

7. Button debounce should be used to ensure when a button is pressed or released the snap shell of the button doesn't cause the signal to oscillate between high and low while the button comes to a rest. This helps to prevent an incorrect input signal from being latched at a clock edge and create incorrect output values. This can be done in the Verilog code by using a counter in conjunction with the clock and a D-flip-flop to make sure the button signal is held constant after changing for a minimum amount of time before the signal is latched or used.