Lab Assignment #0

This lab is a tutorial lab. You don't have to design anything in this lab, just install the required tools on your laptop/PC, go through the tutorials and perform them on your systems individually. In this course, in almost all the labs we will be doing the following steps:

Step 1: Writing Verilog code of the circuit we want to implement
Step 2: Simulating the Verilog code using a simulator (ModelSim) to check if the intended functionality has been achieved
Step 3: Synthesizing the Verilog code using a tool from Xilinx called Vivado so that it can be programmed onto an FPGA
Step 4: Programming the FPGA (an Artix 7 series FPGA from Xilinx) on the lab board (called Basys3 board), also by using Vivado
Step 5: Applying inputs to and observing outputs from our circuit using the peripherals (like switches, buttons, LEDs, etc.) on the Basys3 board

To be able to do all this, we need to learn how to use ModelSim and Vivado, and we also need to understand the capabilities of the Basys3 board and how can we program the Xilinx Artix 7 FPGA on it using Vivado. The following activities will help you go through all the steps so you can learn and use the concepts in the upcoming labs.

Activity 1: Downloading Software Tools

The first step will be to download ModelSim and Vivado, both of which are available online for free. Instructions for downloading and installing them can be found in the Required Software Download Instructions document in the Lab Documentation and Starter Files tab on the EE 460M Canvas home page.

For Mac users:
ModelSim and Vivado only support Linux/Windows and Mac users will have to first install Windows to be able to use them. Instructions for the same can be found at: https://support.apple.com/en-us/HT201468

Though we may have the tools required for this lab on ECE linux servers, installation of these softwares on your systems are necessary for you to be able to program the Basys board through Vivado by connecting it to your systems via USB.

Activity 2: ModelSim tutorial

Mentor Graphic's Modelsim tool will be used to perform the functional simulation of our Verilog code for the course. Go through the "**Modelsim Tutorial**" posted on Canvas under the lab documentation page. This tutorial goes through the basic steps in compiling and simulating within the Modelsim environment using a simple D-flipflop as an example.

Activity 3: Vivado tutorial

The Vivado tool is used to synthesize circuits and place & route them for a particular Xilinx FPGA. Then, a BIT file needs to be generated which can be programmed onto the FPGA so that the FPGA now contains the circuit you designed. Go through the "**Vivado Tutorial**" posted on Canvas under the lab documentation page. You may also visit www.xilinx.com and browse the Artix-7 manuals for help.

Activity 4: Basys3 board tutorial

Read through the **Basys3 Reference Manual** on Canvas under the lab documentation page to understand the features and capabilities of the board to be used in all the labs.

Questions

You should be able to answer (almost all of) the following questions after going through these tutorials:

1. What is ModelSim? What is the role of the transcript window which appears on the bottom of the main ModelSim window?
2. What is a delta cycle in a Verilog simulator like ModelSim?
3. What is a do-file w.r.t. ModelSim? How do you create a do-file of commands entered in the transcript window in ModelSim? Notice how selecting a particular option that is provided by the ModelSim GUI translates into a corresponding ModelSim specific command in the transcript window.
4. Describe the roles and functionality of the following tools in the Vivado suite: Flow Navigator, RTL schematic viewer.
5. What is the Vivado XDC file? What is the purpose of the bitstream file and how is it used to program the FPGA?
6. Is it possible to display two digits using the 7SEG LEDs at the same time on the Basys3 boards? If yes, then how? Note that there are only 7 pins corresponding to a single 7-segment digit.
7. If we want to use the push buttons on the board reliably, what should we do first to the incoming signal into the FPGA? How do we implement this in Verilog? Hint: Refer textbook.

Submission and Grading Details:

Submit a text/doc/pdf file containing the answers to the questions given above on Canvas. Name the file "your_last_name.extension".

Grading for this lab is as follows:
Total points: 50
Canvas submission for answers to the questions above: 25
Lab checkout: 25

Lab checkout for this lab will require you to show us the installed softwares and the outputs of the ModelSim and Vivado tutorials i.e. the simulated waveforms for the D flip-flop on ModelSim, the XDC and bitstreamfiles for the 4-bit adder on Vivado as well as the adder programmed into the Basys board.

Please note that marks will NOT be deducted for Lab checkout(25) even if you are not able to entirely and correctly implement the ModelSim and Vivado tutorials. However, checkout is mandatory and no credit for checkout will be given if someone fails to do so.