



US 20170323899A1

(19) **United States**(12) **Patent Application Publication**
PARK et al.(10) **Pub. No.: US 2017/0323899 A1**(43) **Pub. Date: Nov. 9, 2017**(54) **3D SEMICONDUCTOR MEMORY DEVICE
AND MANUFACTURING METHOD
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Jeong CHEON**, Gyeonggi-do (KR)(21) Appl. No.: **15/279,099**(22) Filed: **Sep. 28, 2016**(30) **Foreign Application Priority Data**

May 4, 2016 (KR) 10-2016-0055548

Publication Classification(51) **Int. Cl.****H01L 27/11582** (2006.01)**H01L 21/28** (2006.01)**H01L 21/02** (2006.01)**H01L 21/02** (2006.01)**H01L 27/11568** (2006.01)**H01L 21/02** (2006.01)**H01L 21/02** (2006.01)(52) **U.S. Cl.**CPC .. **H01L 27/11582** (2013.01); **H01L 27/11568**
(2013.01); **H01L 21/28282** (2013.01); **H01L**
21/02362 (2013.01); **H01L 21/02359**
(2013.01); **H01L 21/0228** (2013.01); **H01L**
21/02164 (2013.01)

(57)

ABSTRACT

Provided herein is a semiconductor device including: a channel layer; a data storage layer surrounding the channel layer and extending along the channel layer; interlayer insulating layers surrounding the data storage layer and stacked along the channel layer, wherein the interlayer insulating layers are spaced apart from each other, wherein a conductive area is disposed between the interlayer insulating layers; a conductive pattern disposed in the conductive area and surrounding the data storage layer; buffer patterns disposed between the interlayer insulating layers and the data storage layer and surrounding the data storage layer, wherein each of the buffer patterns includes a densified area, wherein the buffer patterns are separated from each other by the conductive area; and a blocking insulating pattern disposed between the conductive pattern and the data storage layer and surrounding the data storage layer.

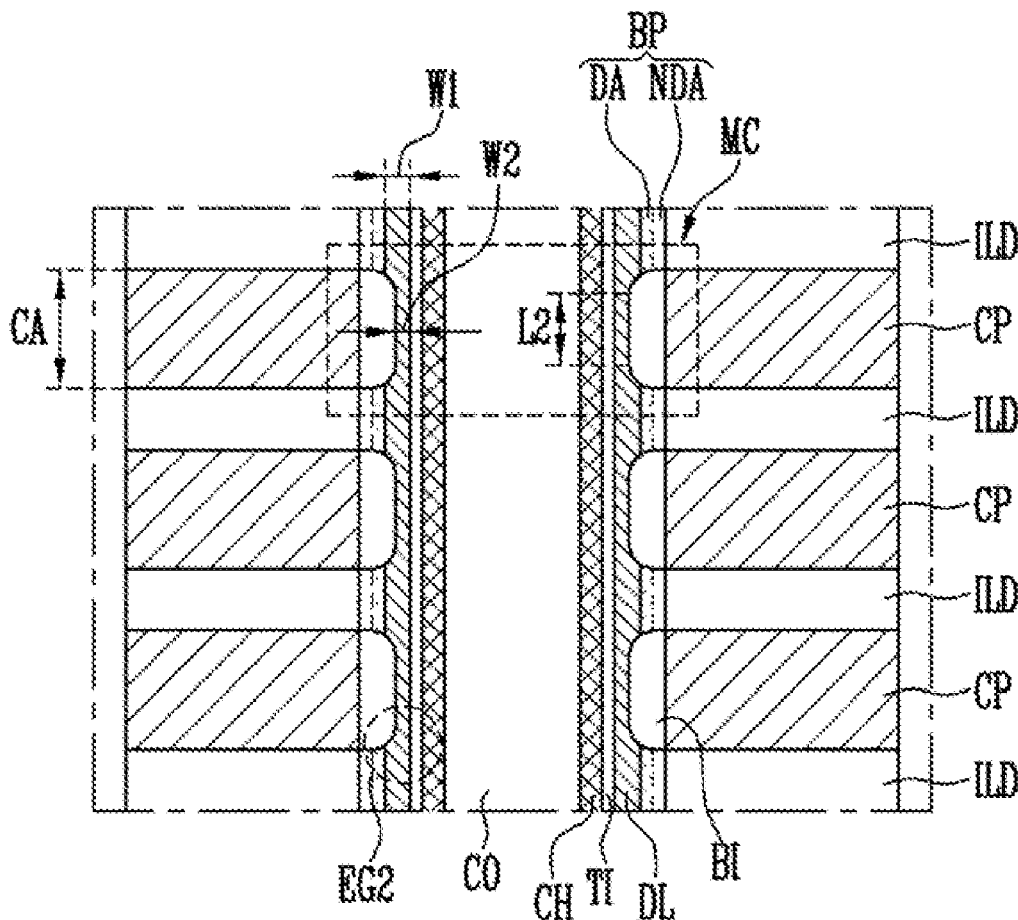


FIG. 1A

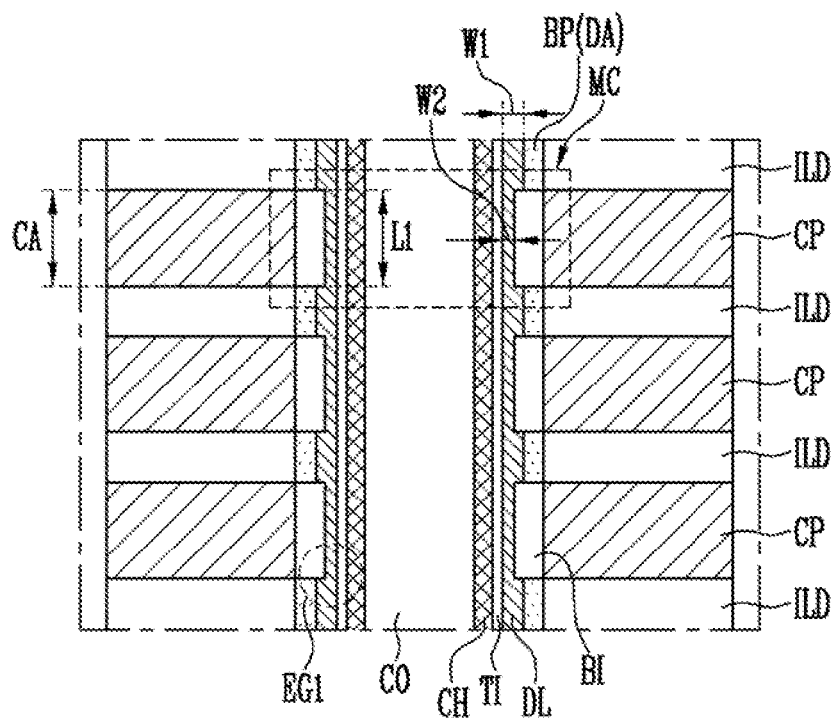


FIG. 1B

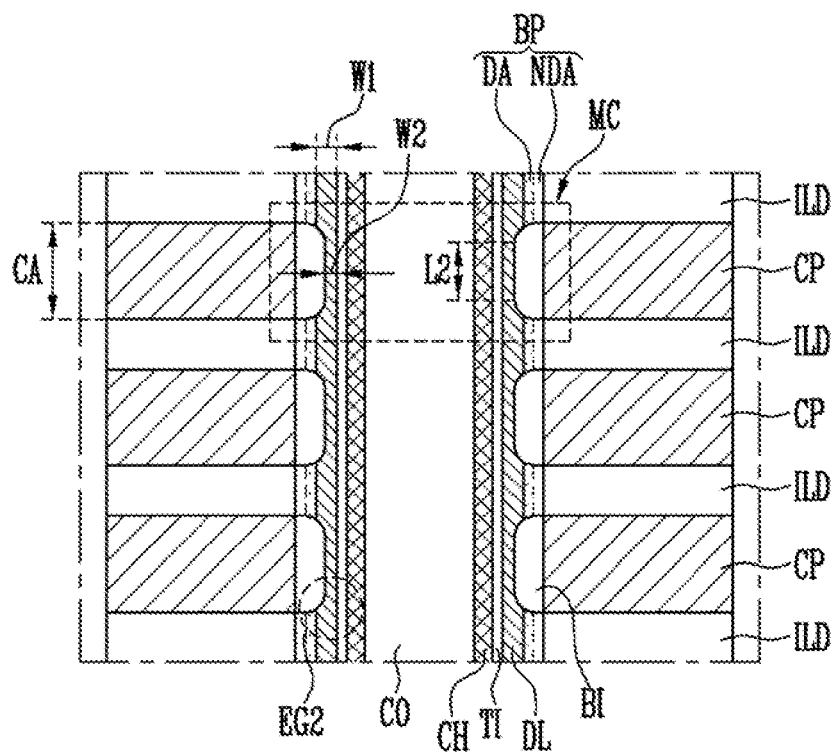


FIG. 1C

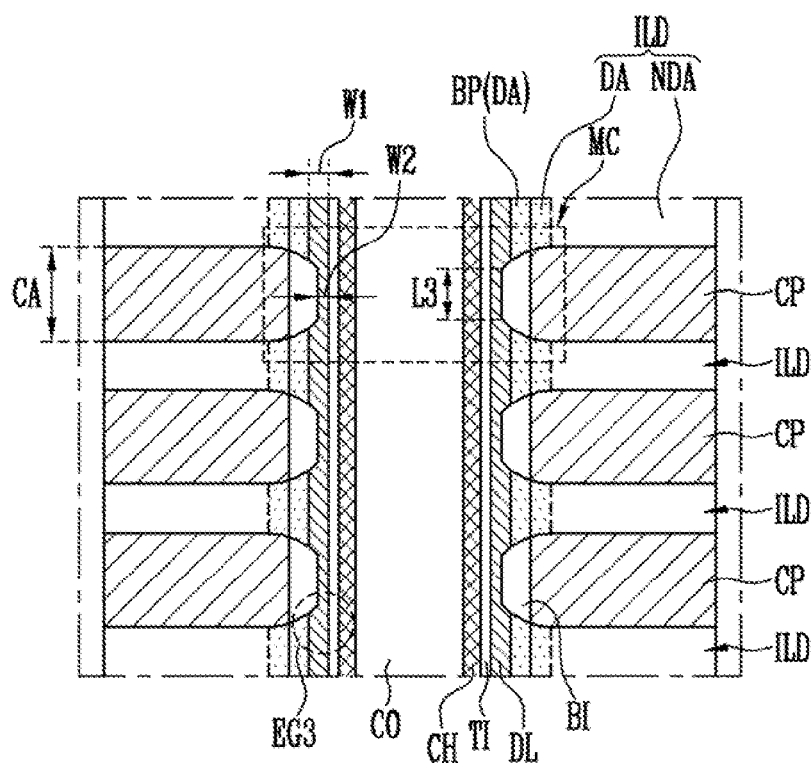


FIG. 1D

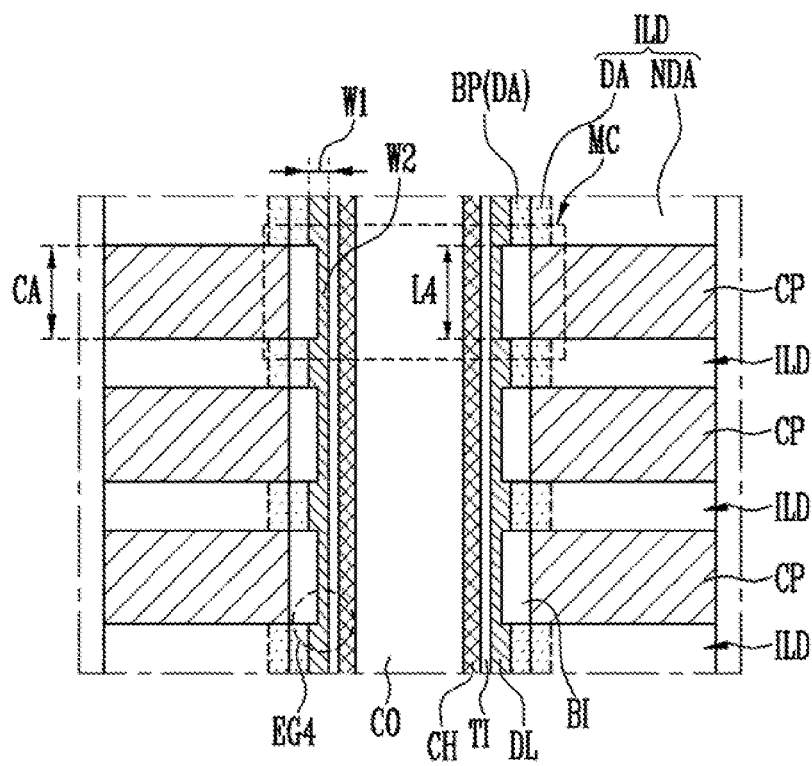


FIG. 2A

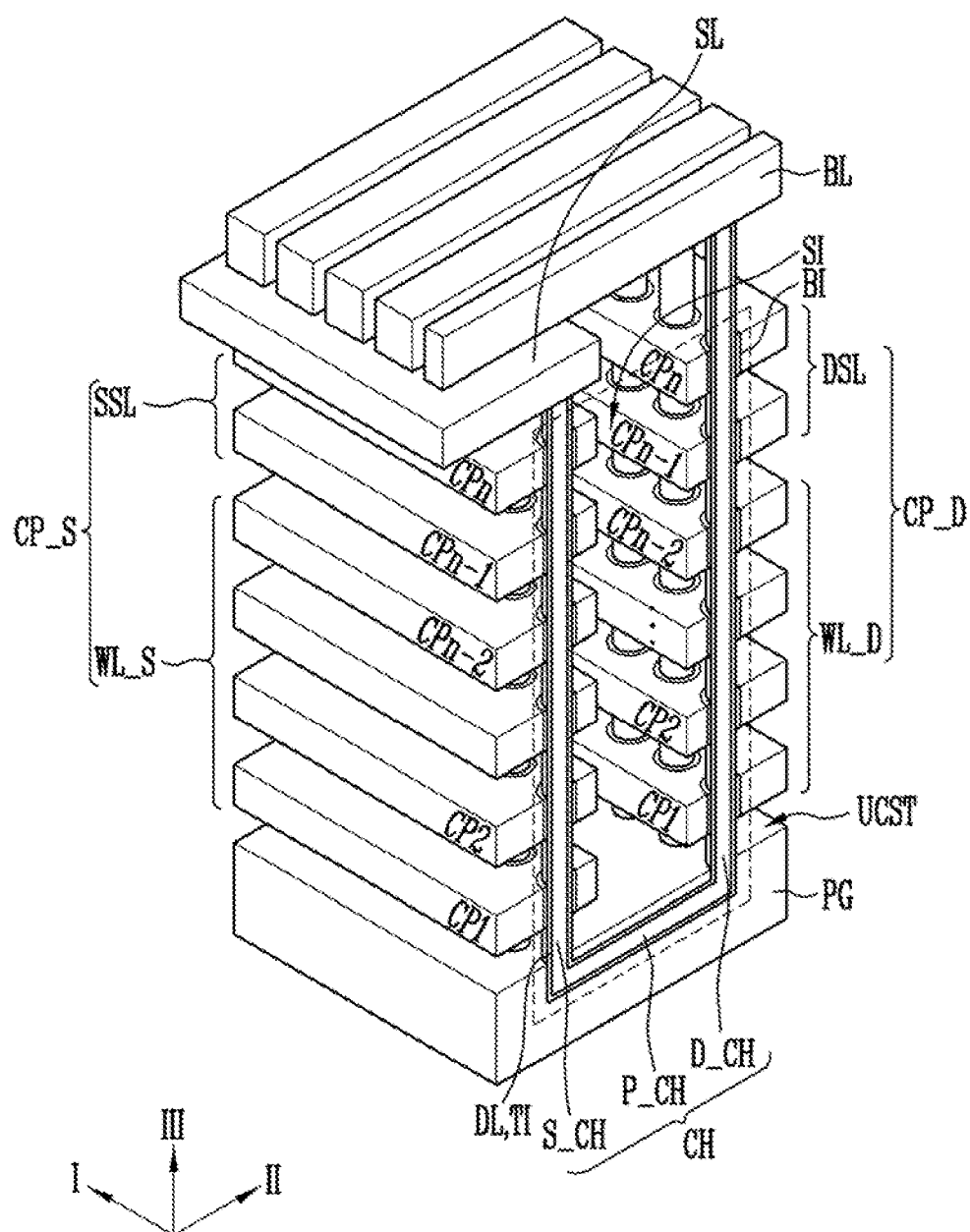
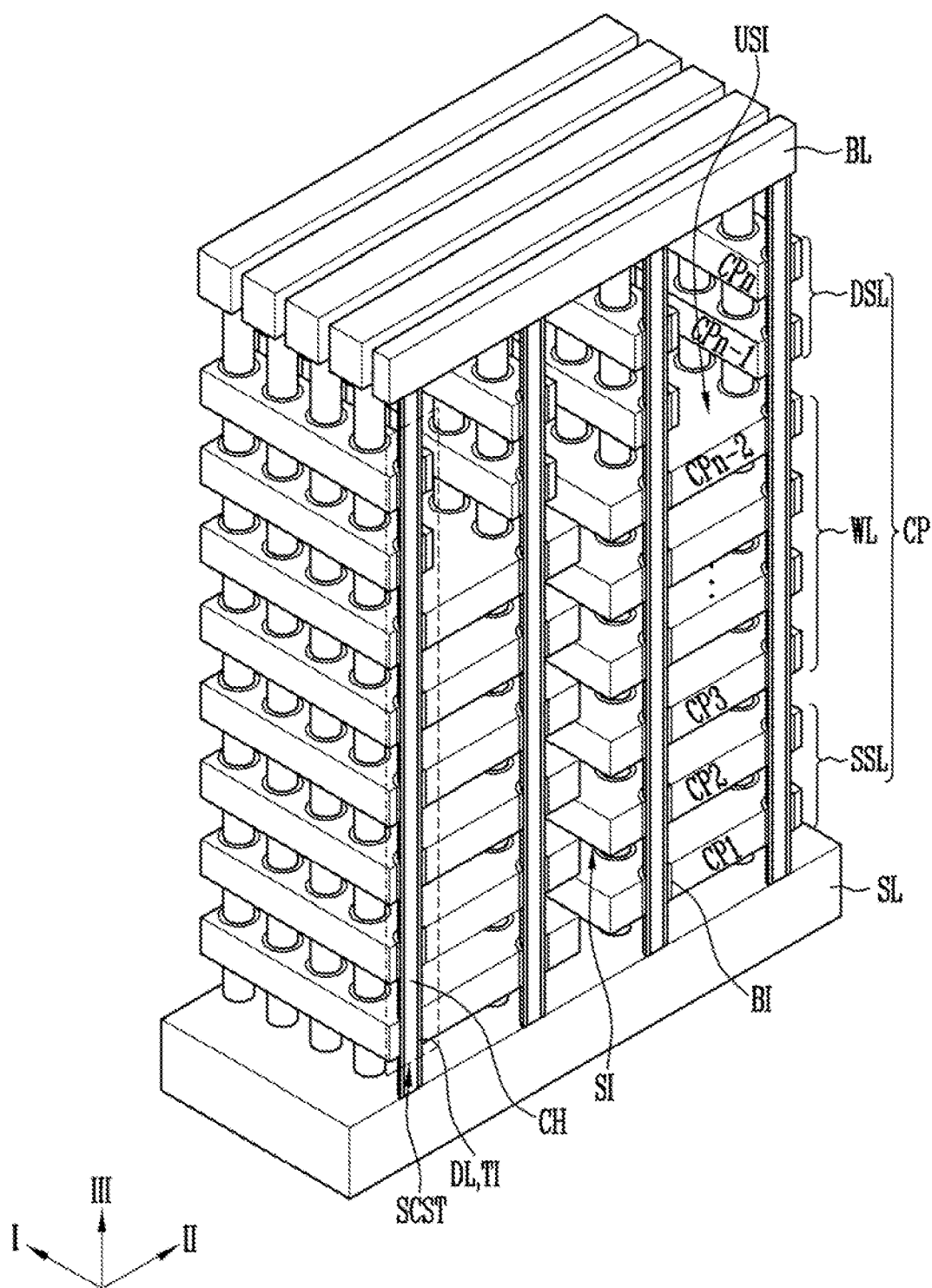


FIG. 2B



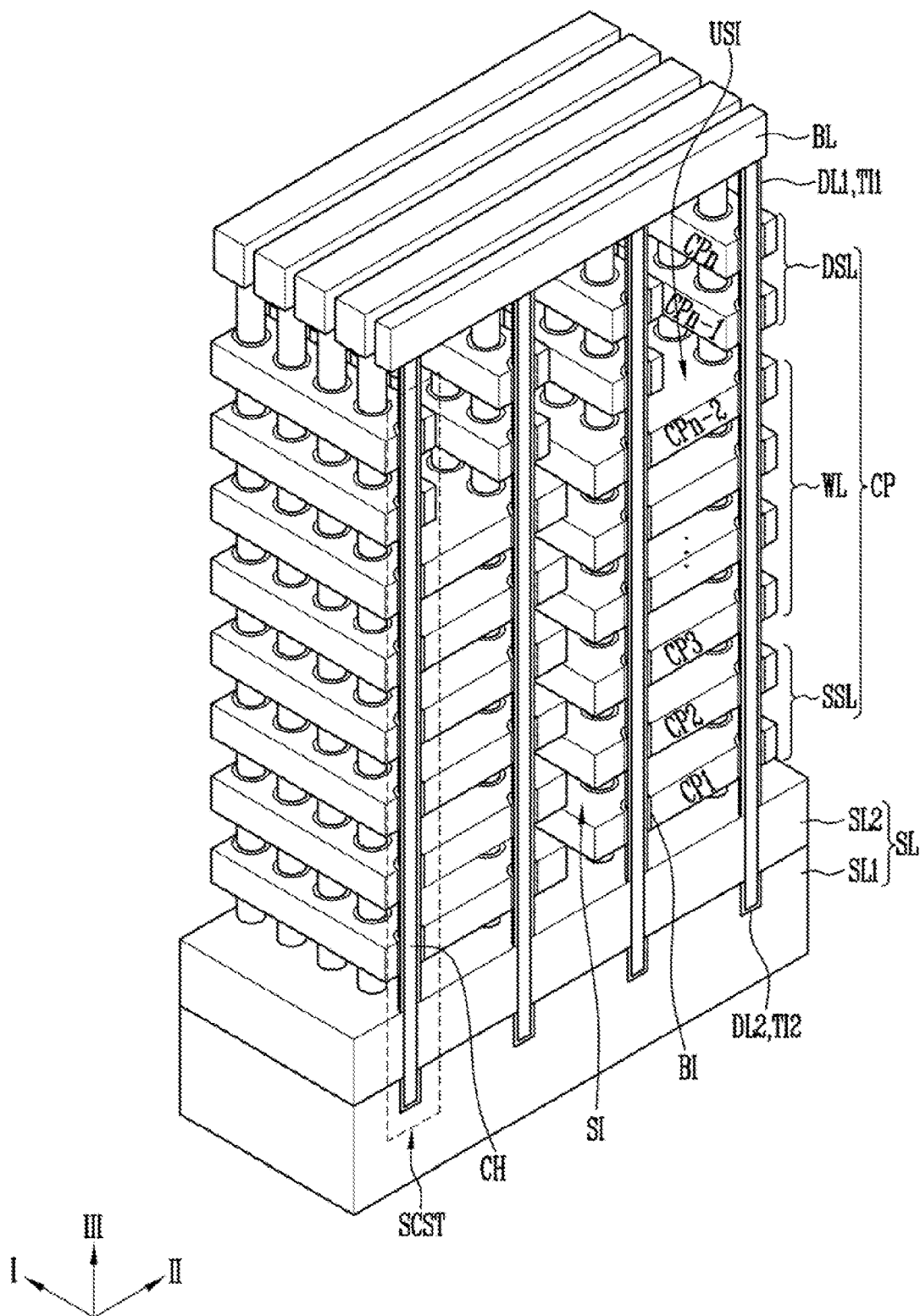


FIG. 3A

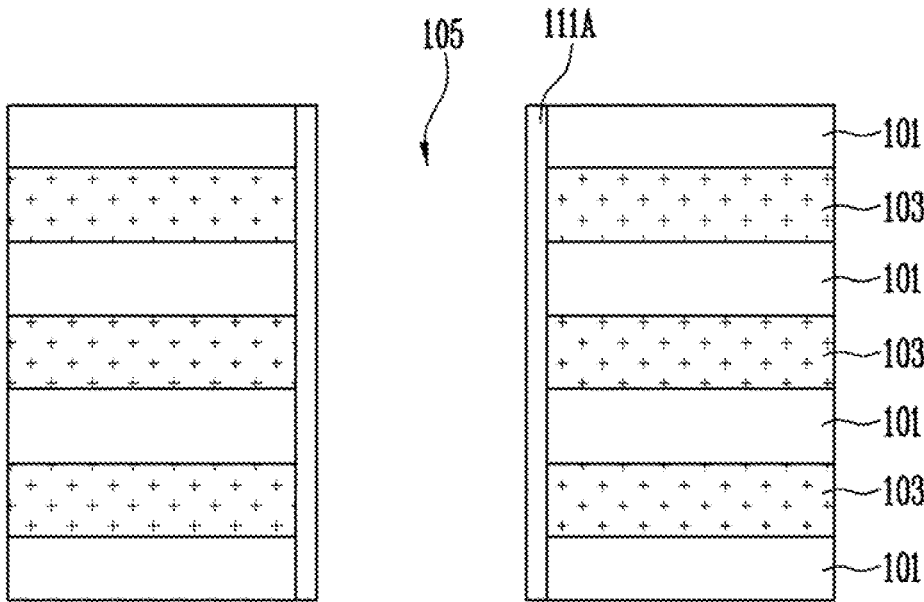


FIG. 3B

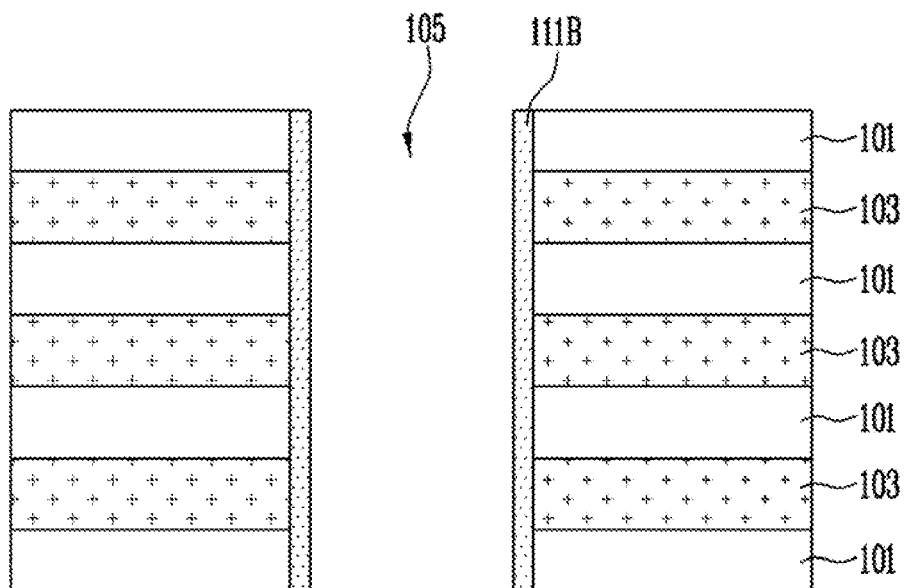


FIG. 3C

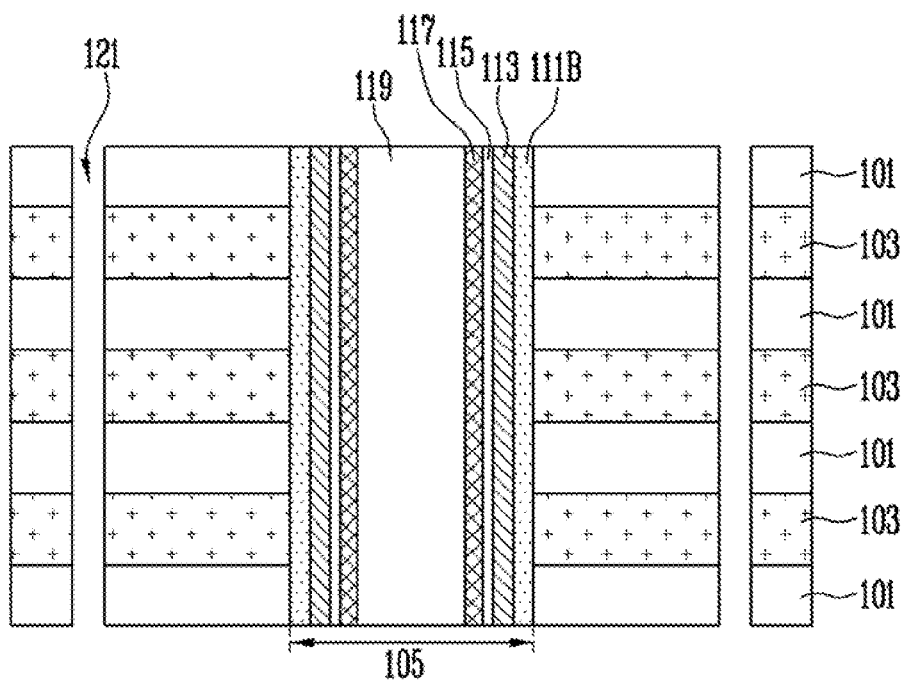


FIG. 3D

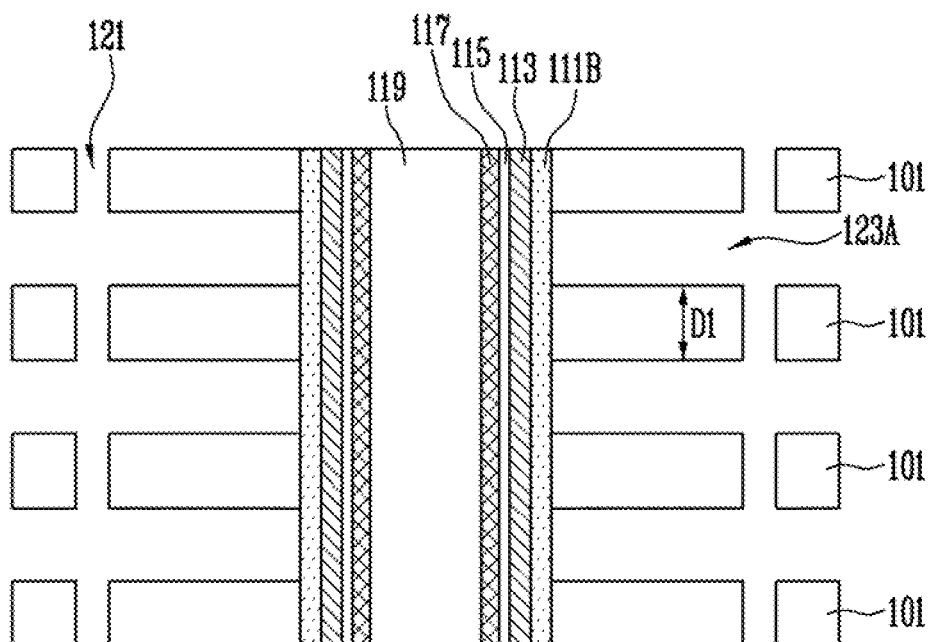


FIG. 3E

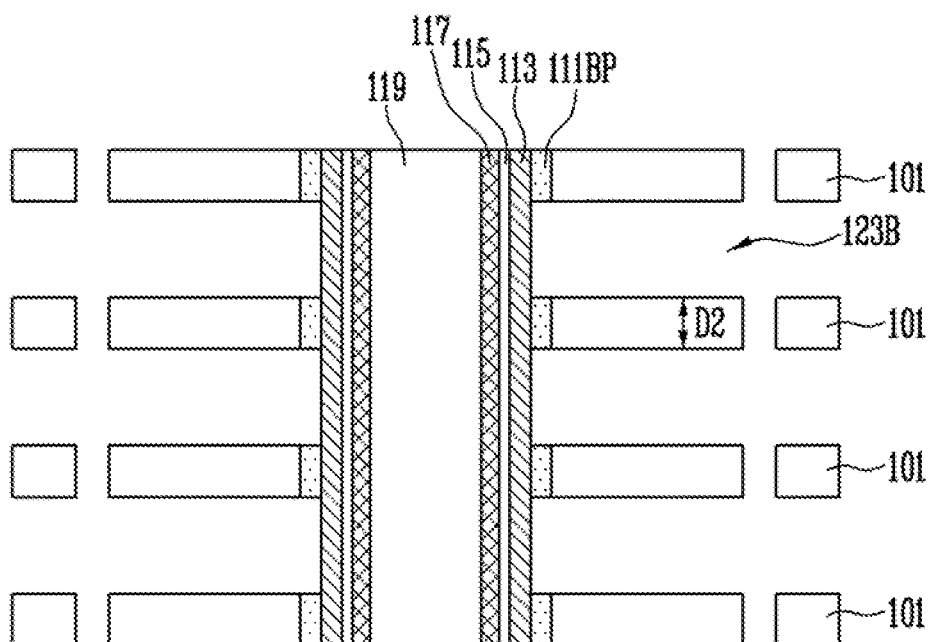


FIG. 3F

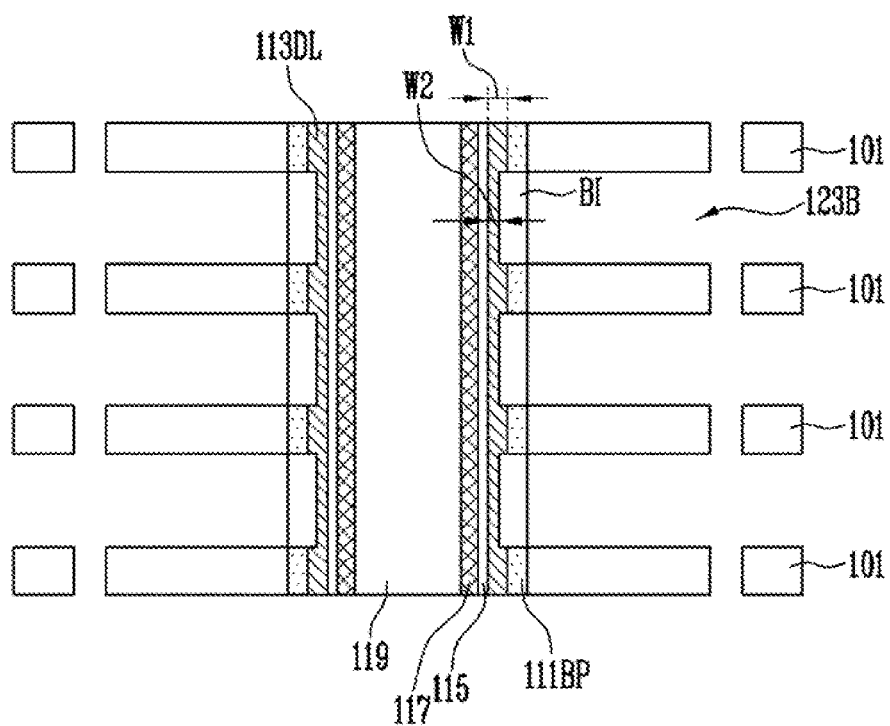


FIG. 3G

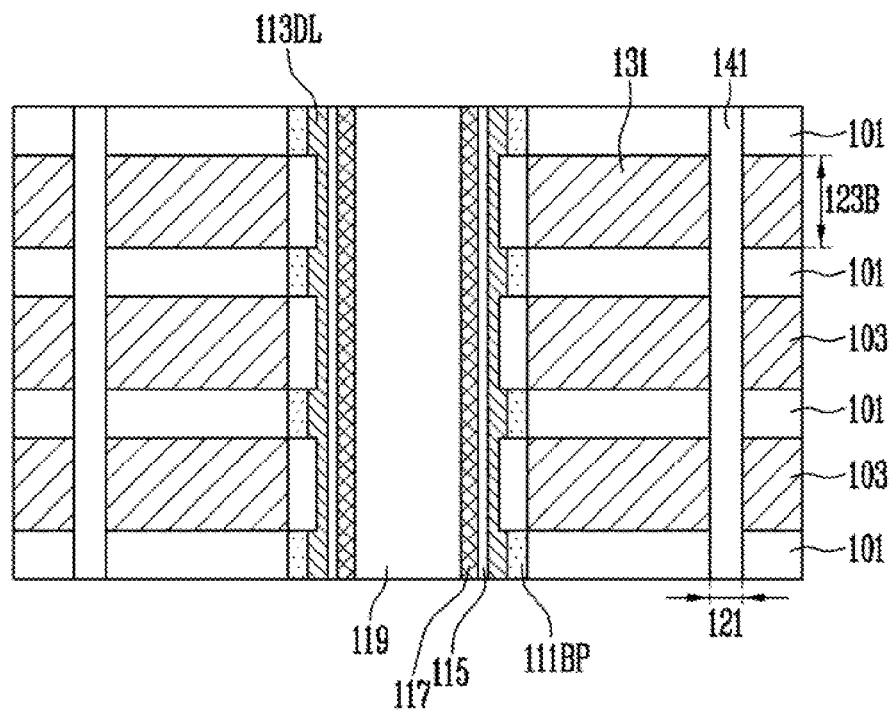


FIG. 5A

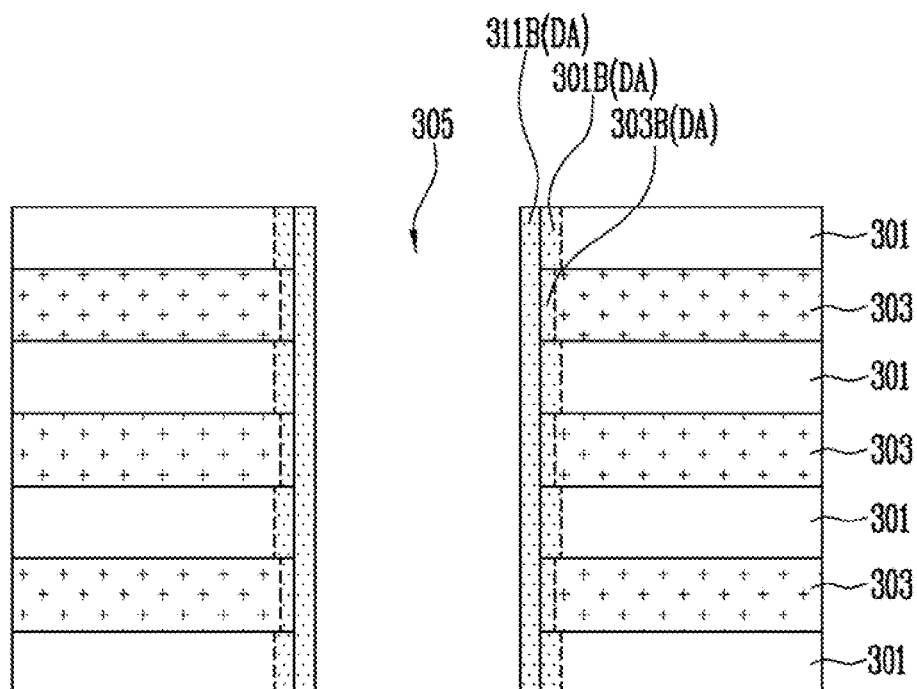


FIG. 5B

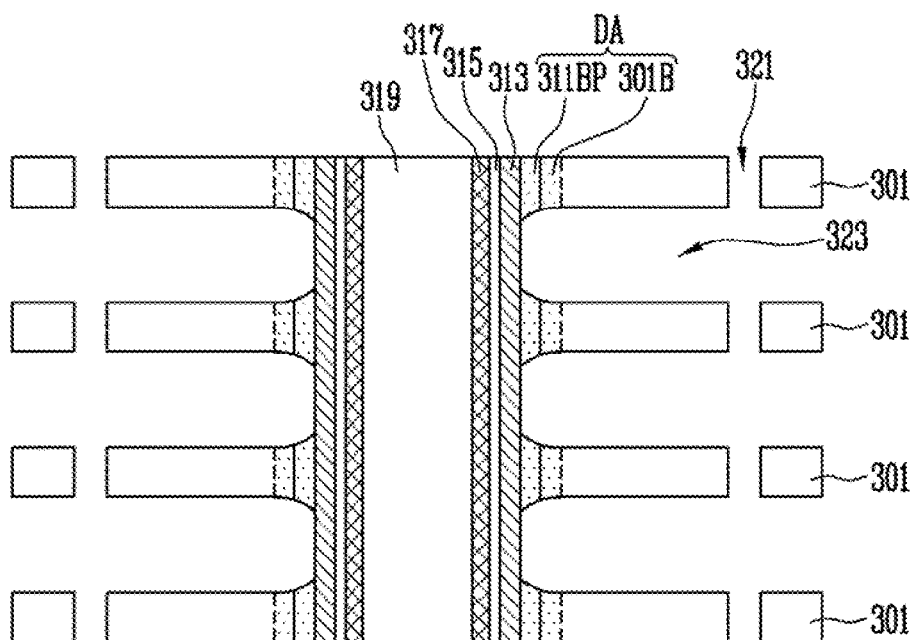


FIG. 6A

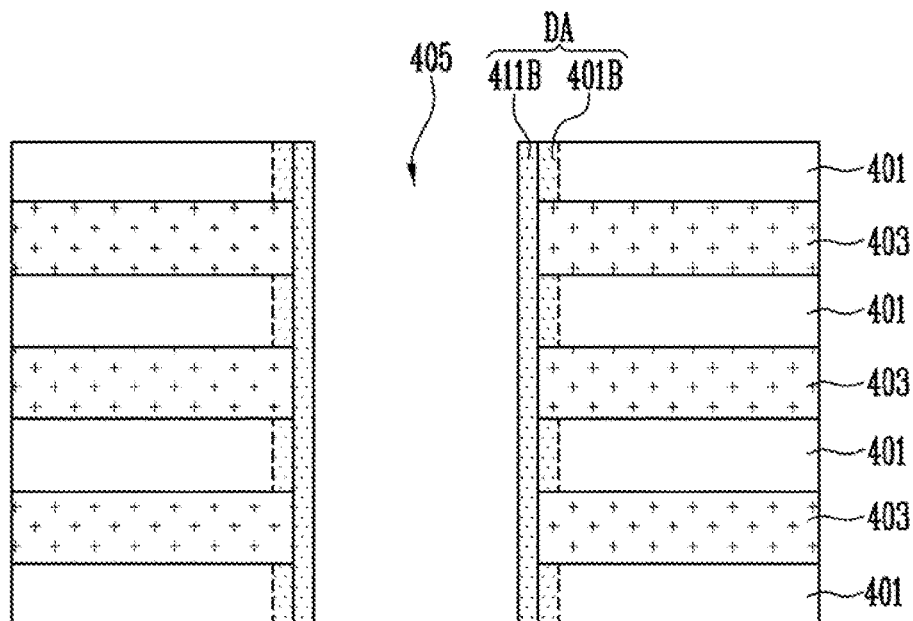


FIG. 6B

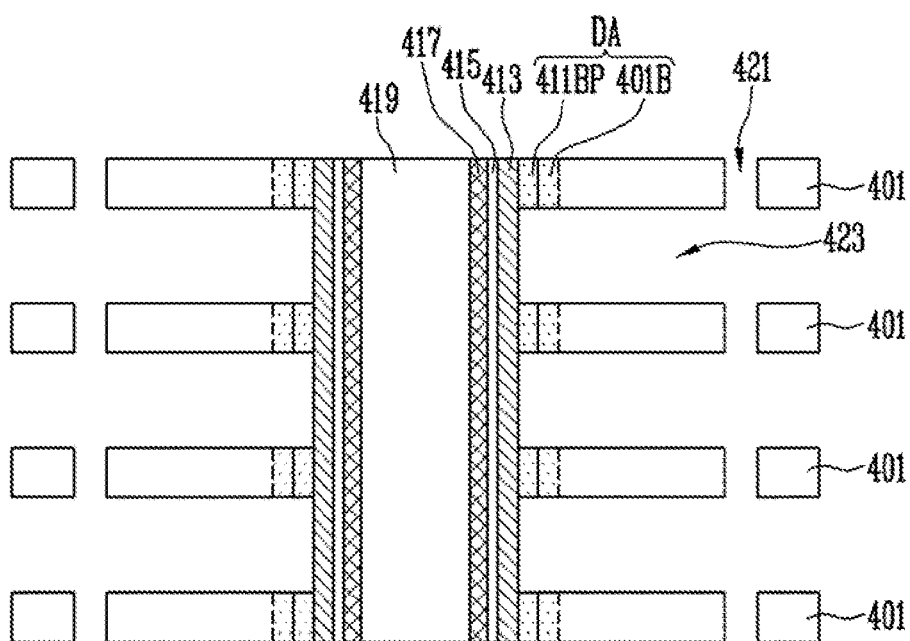


FIG. 7

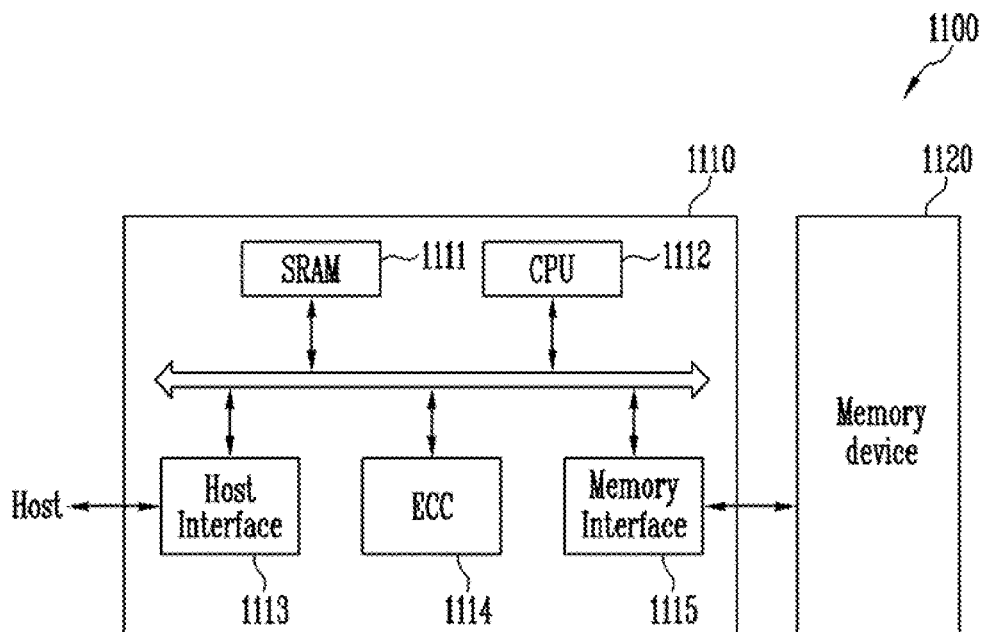
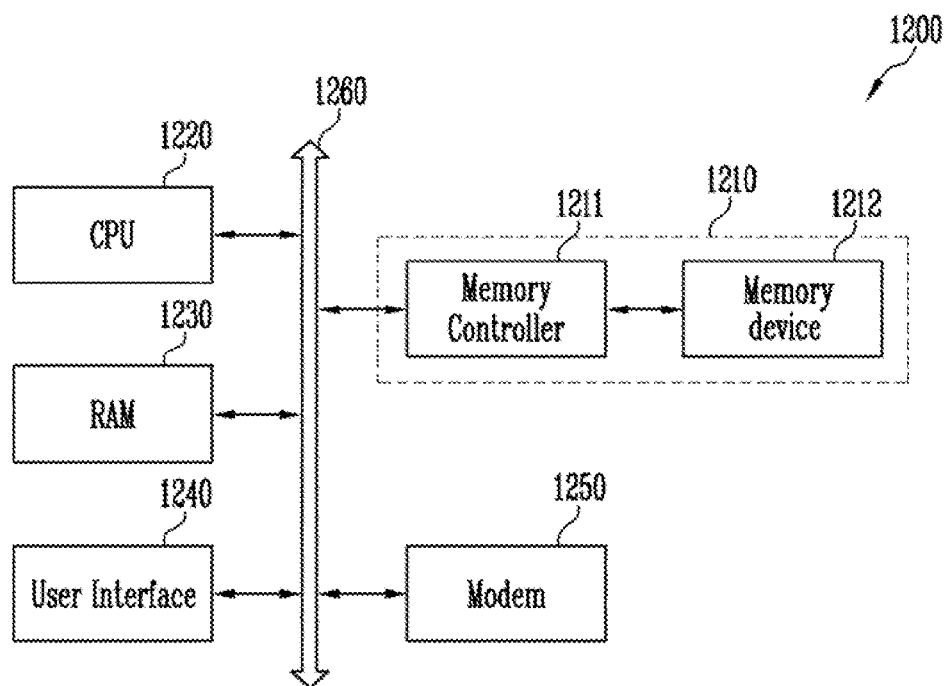


FIG. 8



3D SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. §119(a) to Korean patent application number 10-2016-0055548 filed on May 4, 2016, which is herein incorporated by reference in its entirety.

BACKGROUND

Field of Invention

[0002] Various embodiments of the present disclosure relate to a semiconductor device and a manufacturing method thereof, and more particularly, to a semiconductor device which includes a conductive pattern surrounding a channel layer, and a manufacturing method thereof.

Description of Related Art

[0003] A semiconductor device may include a memory device capable of storing data. The memory device may include memory cells. The memory cells may be arranged in three dimensions. To improve operational characteristics of such memory cells, various technical developments are required. In this case, the memory cells may be coupled to conductive patterns that surround a channel layer.

SUMMARY

[0004] An embodiment of the present disclosure provides a semiconductor device including: a channel layer; a data storage layer surrounding the channel layer and extending along the channel layer; interlayer insulating layers surrounding the data storage layer and stacked along the channel layer, wherein the interlayer insulating layers are spaced apart from each other, wherein a conductive area is disposed between the interlayer insulating layers; a conductive pattern disposed in the conductive area and surrounding the data storage layer; buffer patterns disposed between the interlayer insulating layers and the data storage layer and surrounding the data storage layer, wherein each of the buffer patterns includes a densified area, wherein the buffer patterns are separated from each other by the conductive area; and a blocking insulating pattern disposed between the conductive pattern and the data storage layer and surrounding the data storage layer.

[0005] An embodiment of the present disclosure provides a manufacturing method for a semiconductor device, including: alternately stacking first layers and second layers; forming a hole passing through the first layers and the second layers; forming a buffer layer over a sidewall of the hole; curing dangling bonds in the buffer layer to form a first densified area in the buffer layer; forming a data storage layer over the first densified area; and forming a channel layer over the data storage layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set

forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the example embodiments to those skilled in the art.

[0007] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being “between” two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

[0008] FIGS. 1A to 1D are sectional views illustrating a memory cell of a semiconductor device in accordance with embodiments of the present disclosure;

[0009] FIGS. 2A to 2C are perspective views illustrating memory strings having various structures including memory cells in accordance with embodiments of the present disclosure;

[0010] FIGS. 3A to 3G are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure;

[0011] FIGS. 4A and 4B are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure;

[0012] FIGS. 5A and 5B are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure;

[0013] FIGS. 6A and 6B are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure;

[0014] FIG. 7 is a block diagram illustrating a memory system in accordance with an embodiment of the present disclosure; and

[0015] FIG. 8 is a block diagram illustrating a computing system in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0016] Hereinafter, embodiments will be described in greater detail with reference to the accompanying drawings. Embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of embodiments and intermediate structures. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but may include deviations in shapes that result, for example, from manufacturing. In the drawings, lengths and sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

[0017] Terms such as ‘first’ and ‘second’ may be used to describe various components, but they should not limit the various components. Those terms are only used for the purpose of differentiating a component from other components. For example, a first component may be referred to as a second component, and a second component may be referred to as a first component and so forth without departing from the spirit and scope of the present disclosure. Furthermore, ‘and/or’ may include any one of or a combination of the components mentioned.

[0018] Furthermore, a singular form may include a plural form as long as it is not specifically identified as singular in

a sentence. Furthermore, “include/comprise” or “including/comprising” used in the specification represents that one or more components, steps, operations, and elements exist or are added.

[0019] Furthermore, unless defined otherwise, all the terms used in this specification including technical and scientific terms have the same meanings as would be generally understood by those skilled in the related art. The terms defined in generally used dictionaries should be construed as having the same meanings as would be construed in the context of the related art, and unless clearly defined otherwise in this specification, should not be construed as having idealistic or overly formal meanings.

[0020] It is also noted that in this specification, “connected/coupled” refers to one component not only directly coupling another component but also indirectly coupling another component through an intermediate component. On the other hand, “directly connected/directly coupled” refers to one component directly coupling another component without an intermediate component.

[0021] Embodiments of the present disclosure provide a semiconductor device which has improved operational reliability, and a manufacturing method thereof.

[0022] FIGS. 1A to 1D are sectional views illustrating a memory cell of a semiconductor device in accordance with embodiments of the present disclosure.

[0023] Referring to FIGS. 1A to 1D, a memory cell MC of a semiconductor device in accordance with an embodiment of the present disclosure may have a Gate All Around (GAA) structure. The GAA structure includes a conductive pattern CP which surrounds a channel layer CH. The memory cell MC may include a data storage layer DL which is disposed between the channel layer CH and the conductive pattern CP, a tunnel insulating layer TI which is disposed between the data storage layer DL and the channel layer CH, and a blocking insulating pattern BI which is disposed between the data storage layer DL and the conductive pattern CP. The data storage layer DL, the tunnel insulating layer TI, and the blocking insulating pattern BI surround the channel layer CH. The data storage layer DL and the tunnel insulating layer TI extend along the channel layer CH.

[0024] The conductive pattern CP may be disposed in a conductive area CA.

[0025] The conductive area CA may be formed between interlayer insulating layers ILD which are stacked along the channel layer CH.

[0026] The data storage layer DL and the tunnel insulating layer TI may extend along sidewalls of the interlayer insulating layers ILD. The data storage layer DL may extend on the sidewalls of the interlayer insulating layers ILD. Buffer patterns BP are interposed between the data storage layer DL and the interlayer insulating layers ILD. The buffer patterns BP may be separated from each other by the blocking insulating pattern BI interposed therebetween.

[0027] The channel layer CH may have a tube shape and surround a core insulating layer CO. The core insulating layer CO may not be formed. In this case, the channel layer CH may include a central region filled with a semiconductor layer. The cross-section of the channel layer CH may have various shapes, such as a circle, an ellipse, a rectangle, a square, and a polygon.

[0028] The data storage layer DI may be divided into first areas defined between the buffer patterns BP and the channel layer CH and a second area defined between the block

insulating pattern BI and the channel layer CH. The blocking insulating pattern BI may extend further into the data storage layer DL than the buffer patterns BP. In this case, a thickness W2 of the second area of the data storage layer DL may be less than a thickness W1 of each of the first areas. More particularly, the data storage layer DL may include a first sidewall which faces the channel layer CH and is planar, and a second sidewall which faces the interlayer insulating layers ILD and the conductive pattern CP and has an uneven surface structure. The second sidewall may have a depression into which the blocking insulating pattern BI extends, and protrusions which face the interlayer insulating layers ILD.

[0029] Each of the buffer patterns BP may include a densified area DA. The densified area DA may contact the data storage layer DL. As shown in FIGS. 1A and 1B, the densified area DA may be disposed only within the buffer patterns BP. Alternatively, as shown in FIGS. 1C and 1D, the densified area DA may extend into each of the interlayer insulating layers ILD that contact the buffer patterns BP. The densification degree of the densified area DA may gradually increase as it is closer to the channel layer CH. The densification degree of the densified area DA is in inverse proportion to a density of dangling bonds. That is, the less the dangling bonds, the higher the densification degree of the densified area DA is. The densified area DA may be defined as an area in which dangling bonds are cured. Hereinafter, various embodiments of the densified area DA will be described in more detail.

[0030] As shown in FIGS. 1A, 1C and 1D, the densified area DA may be distributed in the entire areas of the buffer patterns BP.

[0031] Referring to FIG. 1A, the densified area DA may be distributed on the entire areas of the buffer patterns BP and disposed only within the buffer patterns BP. In this case, an edge EG1 of the conductive area CA that is adjacent to the data storage layer DL may be formed at a right angle or a substantially right angle. The edge EG1 of the conductive area CA is defined by the buffer patterns BP and the data storage layer DL. The densified area DA may have an etching rate less than that of the interlayer insulating layers ILD because the density of the densified area DA is higher than that of the interlayer insulating layers ILD.

[0032] Referring to FIGS. 1C and 1D, the densified area DA may extend into each of the interlayer insulating layers ILD that contact the buffer patterns BP. In this case, each of the interlayer insulating layers ILD may include a densified area DA and a non-densified area NDA. The densified area DA of the interlayer insulating layer ILD may be disposed along the sidewall of the interlayer insulating layer ILD that comes into contact with the buffer pattern BP.

[0033] When the densified area DA extends into each of the interlayer insulating layers ILD, as shown in FIG. 1C, an edge EG3 of the conductive area CA that is adjacent to the data storage layer DL may have a round shape or a substantially round shape. That is, the conductive area CA may have a round edge EG3. Alternatively, as shown in FIG. 1D, an edge EG4 of the conductive area CA that is adjacent to the data storage layer DL may be formed at a right angle or a substantially right angle. That is, the conductive area CA may have a squared edge EG4. The shapes of the edges EG3 and EG4 of the conductive area CA shown in FIGS. 1C and

1D may be controlled depending on whether sacrificial layers (not shown) are cured during the manufacturing process.

[0034] As shown in FIG. 1B, each of the buffer patterns BP may include a densified area DA and a non-densified area NDA. The densified area DA may be disposed along one sidewall of the corresponding buffer pattern BP that is adjacent to the data storage layer DL. The non-densified area NDA may be disposed between the corresponding interlayer insulating layer ILD and the densified area DA. When each of the buffer patterns BP includes the densified area DA and the non-densified area NDA, an edge EG2 of the conductive area CA that is adjacent to the data storage layer DL may be formed in a round shape or a substantially round shape due to a difference in etching rate between the densified area DA and the non-densified area NDA. The edge EG2 of the conductive area CA is defined by the densified area DA, the non-densified area NDA and the data storage layer DL.

[0035] As described above with reference to FIGS. 1A to 1D, the densified area DA in accordance with the embodiment of the present disclosure may be in various structures, and the structure may be controlled in accordance with the embodiment of the present disclosure. In this way, the conductive area CA may be formed in a desired shape by controlling the structure of the densified area DA in accordance with the embodiment of the present disclosure.

[0036] In an embodiment of the present disclosure, according to a design of the memory cell MC, the width of the densified area DA is controlled, whereby the edges EG1 to EG4 of the conductive area CA that face the channel layer CH may be formed in desired shapes. Hence, in the embodiment of the present disclosure, an effective gate length or effective gate width of the memory cell MC may be controlled to a desired value.

[0037] For example, as shown in FIG. 1A, when a buffer layer is densified such that the entire area of the buffer pattern BP becomes the densified area DA, the buffer layer may be uniformly etched while a process of forming the buffer pattern BP by etching the buffer layer is performed. Thereby, the edge of the buffer pattern BP that faces the channel layer may be formed at a right angle or a substantially right angle. Therefore, the edge EG1 of the conductive area CA that faces the channel layer CH may be formed at a right angle or a substantially right angle. In this case, an effective gate length L1 of the memory cell MC may be the same as a vertical width of the conductive pattern CP, and an area through which a bias is applied to the conductive pattern CP may be increased. As a result, the speed of erase and program operations of the memory cell MC may be improved.

[0038] Alternatively, as shown in FIG. 1B, when a portion of the buffer layer is densified such that the buffer pattern BP includes a densified area DA and a non-densified area NDA, the densified area and the non-densified area NDA of the buffer layer that have different etching rates may be etched at different rates while a process of forming the buffer pattern BP by etching the buffer layer is performed. In more detail, the densified area DA may be etched at a rate less than that of the non-densified area NDA. Therefore, the edge EG2 of the conductive area CA that faces the channel layer CH may be formed in a round shape or a substantially round shape. In this case, an effective gate length L2 of the memory cell MC may be less than a vertical width of the conductive pattern CP. In addition, interference between

memory cells MC which are adjacent to each other with respect to the extension direction of the channel layer CH may be reduced.

[0039] As a further alternative, as shown in FIGS. 1C and 1D, when the densified area DA extends into the interlayer insulating layer ILD, the edge EG3 or EG4 of the conductive layer CA that faces the channel layer CH may have a round shape or a substantially round shape or be formed at a right angle or a substantially right angle depending on whether sacrificial layers (not shown) are densified during the manufacturing process. Each of the edge EG3 and EG4 is defined by the densified area DA of each of the buffer patterns BP, the densified area DA of each of the interlayer insulating layers ILD and the data storage layer DL.

[0040] Furthermore, when the densified area DA extends into the sacrificial layers (not shown) during the densification process, the edge EG3 of the conductive area CA that faces the channel layer CH may have a round shape or a substantially round shape, as shown in FIG. 1C. In this case, the effective gate length L3 of the memory cell MC may be less than the vertical width of the conductive pattern CP. In addition, interference between memory cells MC which are adjacent to each other with respect to the extension direction of the channel layer CH may be reduced.

[0041] When the densified area DA does not extend into the sacrificial layers (not shown) during the densification process, the edge EG4 of the conductive area CA that faces the channel layer CH may be formed at a right angle or a substantially right angle, as shown in FIG. 1D. In this case, the effective gate length L4 of the memory cell MC may be the same as the vertical width of the conductive pattern CP, and an area through which a bias is applied to the conductive pattern CP may be increased. As a result, the speed of the erase and program operations of the memory cell MC may be improved.

[0042] Referring to FIGS. 1A to 1D, memory cells MC in accordance with the embodiment of the present disclosure are stacked along the extension direction of the channel layer CH and thus form a memory string of a three-dimensional memory device. In this case, the interlayer insulating layers ILD and the conductive patterns CP may surround the channel layer CH and be alternately stacked.

[0043] Although FIGS. 1A to 1D illustrate an arrangement of the memory cells MC forming a memory string of a three-dimensional memory device, the embodiments of the present disclosure is not limited to them. Various modifications are possible for a semiconductor device including a memory cell MC that has a GAA structure and is disposed between interlayer insulating layers ILD.

[0044] FIGS. 2A to 2C are perspective views illustrating memory strings having various structures which include memory cells in accordance with embodiments of the present disclosure. Particularly, FIGS. 2A to 2C are perspective views illustrating three-dimensional memory strings. In FIGS. 2A to 2C, interlayer insulating layers are not shown for conciseness of description.

[0045] The memory string in accordance with the embodiments of the present disclosure may have a three-dimensional structure to embody high integration of a semiconductor device. For example, the memory string may be formed in a U type shape, as shown in FIG. 2A, or in a straight type shape, as shown in FIGS. 2B and 2C.

[0046] Referring to FIG. 2A, a U type memory string UCST may include memory cells and select transistors

which are arranged along a U type channel layer CH. Gates of the memory cells and gates of the select transistors may be coupled to conductive patterns CP1 to CPn.

[0047] The channel layer CH may include a pipe channel layer P_CH which is embedded in a pipe gate PG, and a source side channel layer S_CH and a drain side channel layer D_CH which extend from the pipe channel layer P_CH. The channel layer CH may be formed in the form of a tube which surrounds a core insulating layer in which a central region of a U-shaped hole is filled. Alternatively, the central region of the U-shaped hole is completely filled with the channel layer CH.

[0048] The channel layer CH may be electrically coupled between a source line SL and a bit line BL. The bit line BL and the source line SL are disposed at different layers from each other and spaced apart from each other. For example, the source line SL may be disposed below the bit line BL. The source line SL may be electrically coupled to an upper end of the source side channel layer S_CH. The source line SL may extend in a first direction I. A source contact plug may be formed between the source line SL and the source side channel layer S_CH. The bit line BL may be electrically coupled to an upper end of the drain side channel layer D_CH. The bit line BL may extend in a second direction II intersecting the first direction I. A drain contact plug may be formed between the bit line BL and the drain side channel layer D_CH.

[0049] The conductive patterns CP1 to CPn are disposed below the bit line BL and the source line SL, form an "n" number of multi-layer stacks, and are spaced apart from each other. The conductive patterns CP1 to CPn may include source side conductive patterns CP_S and drain side conductive pattern CP_D.

[0050] The source side conductive patterns CP_S may surround the source side channel layer S_CH and be stacked spaced apart from each other. The source side conductive patterns CP_S may include source side word lines WL_S and a source select line SSL. The source select line SSL may be disposed over the source word lines WL_S. The source select line SSL may have a single layered or two or more layered structure and be formed over the source side word lines WL_S. Although, in the drawing, for example, the source select line SSL is configured with an n_{th} pattern CPn that is disposed at an uppermost layer of the source side conductive patterns CP_S and with an $n-1_{th}$ pattern CPn-1 disposed below the n_{th} pattern CPn, the present disclosure is not limited to this.

[0051] The drain side conductive patterns CP_D may surround the drain side channel layer D_CH and be stacked spaced apart from each other. The drain side conductive patterns CP_D may include drain side word lines WL_D and a drain select line DSL. The drain select line DSL may be disposed over the drain side word lines WL_D. The drain select line DSL may have a single layered or two or more layered structure over the drain side word lines WL_D. Although, in the drawing, for example, the drain select line DSL is configured with an n_{th} pattern CPn that is disposed at an uppermost layer of the drain side conductive patterns CP_D and with an $n-1_{th}$ pattern CPn-1 disposed below the n_{th} pattern CPn, the present disclosure is not limited to this configuration.

[0052] The source side conductive patterns CP_S and the drain side conductive patterns CP_D may be separated from each other by a slit SI formed therebetween.

[0053] The pipe gate PG is disposed below the source side conductive patterns CP_S and the drain side conductive patterns CP_D and formed to surround the pipe channel layer P_CH. The pipe gate PG may be disposed below the conductive patterns CP1 to CPn.

[0054] An outer sidewall of the channel layer CH may be surrounded by a tunnel insulating layer TI and a data storage layer DL. The tunnel insulating layer TI and the data storage layer DL may have the same structures as those described with reference to FIG. 1A, 1B, 1C or 1D.

[0055] The data storage layer DL may be surrounded by the blocking insulating patterns BI. The blocking insulating patterns BI may be disposed between the data storage layer DL and the respective conductive patterns CP1 to CPn. Each blocking insulating pattern BI may have the same structure as that described with reference to FIG. 1A, 1B, 1C or 1D.

[0056] Source side memory cells are formed at intersections between the source side channel layer S_CH and the source side word lines WL_S, and drain side memory cells are formed at intersections between the drain side channel layer D_CH and the drain side word lines WL_D. A source select transistor is formed at an intersection between the source side channel layer S_CH and the source select line SSL, and a drain select transistor is formed at an intersection between the drain side channel layer D_CH and the drain select line DSL. A pipe transistor is formed at an intersection between the pipe channel layer P_CH and the pipe gate PG.

[0057] The source select transistor, the source side memory cells, the pipe transistor, the drain side memory cells, and the drain select transistor that are arranged along the single channel layer CH may be coupled to each other in series through the channel layer CH. The source select transistor, the source side memory cells, the pipe transistor, the drain side memory cells and the drain select transistor that are coupled to each other in series define a U type memory string UCST along the U type shape of the channel layer CH.

[0058] The source side word lines WL_S may transmit signals to gates of the source side memory cells. The drain side word lines WL_D may transmit signals to gates of the drain side memory cells. The source select line SSL may transmit a signal to a gate of the source select transistor. The drain select line DSL may transmit a signal to a gate of the drain select transistor. The pipe gate PG may transmit a signal to a gate of the pipe transistor. The pipe transistor may couple the source side memory cells and the drain side memory cells to each other, in response to a signal applied to the pipe gate PG.

[0059] The channel layer CH may have various shapes, for example, as the above-mentioned U type shape, as a W type shape, etc. The arrangement of the memory cells may be changed in various shapes depending on the structure of the channel layer CH. Thereby, the memory string structure may also have various shapes.

[0060] Each of the source side memory cells and drain side memory cells that form the memory string UCST described with reference to FIG. 2A may have the same structure as that of any one of the memory cells described with reference to FIGS. 1A to 1D.

[0061] Referring to FIGS. 2B and 2C, a straight type memory string SCST may include memory cells and select transistors which are stacked along a straight type channel

layer CH. Gates of the memory cells and gates of the select transistors may be coupled to conductive patterns CP1 to CPn.

[0062] The channel layer CH may be formed in the form of a tube which surrounds a core insulating layer. The core insulating layer may be located in a central region of a straight type hole. Alternatively, the central region of the straight type hole is completely filled with the channel layer CH.

[0063] An upper end of the channel layer CH may be electrically coupled to a bit line BL. The bit line BL may extend in a second direction II. A drain contact plug (not shown) may be further formed between the bit line BL and the channel layer CH.

[0064] The channel layer CH may be coupled to a source structure SL. The source structure SL may be formed to have various structures.

[0065] As shown in FIG. 2B, the source structure SL may contact the bottom of the channel layer CH. The source structure SL may be formed of a doped polysilicon layer. The channel layer CH may contact an upper surface of the source structure SL and extend in a third direction III toward the bit line BL.

[0066] A sidewall of the channel layer CH shown in FIG. 2B may be surrounded by a tunnel insulating layer TI and a data storage layer DL. The tunnel insulating layer TI and the data storage layer DL may have the same structures as those described with reference to FIG. 1A to 1D. The data storage layer DL may be surrounded by the blocking insulating patterns BI.

[0067] The blocking insulating patterns BI may be disposed between the data storage layer DL and the respective conductive patterns CP1 to CPn. Each blocking insulating pattern BI may have the same structure as that described with reference to FIGS. 1A to 1D.

[0068] As shown in FIG. 2C, a portion of the lower end of the channel layer CH may extend into the source structure SL. That is, the lower end of the channel layer CH may pass through a portion of the source structure SL.

[0069] Furthermore, the source structure SL may have a stacked structure including a first source layer SL1 and a second source layer SL2. The first source layer SL1 may surround the lower end of the channel layer CH. The second source layer SL2 may be disposed over the first source layer SL1 and contact an upper surface of the first source layer SL1 and the sidewall of the channel layer CH. The second source layer SL2 may surround a lower sidewall of the channel layer CH.

[0070] The outer sidewall of the channel layer CH shown in FIG. 2C may be surrounded by a first tunnel insulating pattern TI1 and a first data storage pattern DL1, or by a second tunnel insulating pattern TI2 and a second data storage pattern DL2. The first tunnel insulating pattern TI1 and the first data storage pattern DL1 may have the same structures as those of the tunnel insulating layer and the data storage layer that have been described with reference to FIGS. 1A to 1D. The second tunnel insulating pattern TI2 and the second data storage pattern DL2 are disposed between the first source layer SL1 and the channel layer CH.

[0071] The first tunnel insulating pattern TI1 and the second tunnel insulating pattern TI2 may be separated from each other by the second source layer SL2 disposed therebetween. The first data storage pattern DL1 and the second data storage pattern DL2 may be separated from each other

by the second source layer SL2 disposed therebetween. The first data storage pattern DL1 may be surrounded by the blocking insulating patterns BI. The blocking insulating patterns BI may be disposed between the first data storage pattern DL1 and the respective conductive patterns CP1 to CPn. Each blocking insulating pattern BI may have the same structure as that described with reference to FIGS. 1A to 1D.

[0072] Referring to FIGS. 2B and 2C, the conductive patterns CP1 to CPn may form an “n” number of layers, which are spaced apart from each other, between the bit line BL and the source structure SL. The conductive patterns CP1 to CPn may surround the channel layer CH and be stacked spaced apart from each other. The conductive patterns CP1 to CPn may include a source select line SSL, word lines WL, and a drain select line DSL. The source select line SSL may be disposed over the source structure SL. The word lines WL may be disposed over the source select line SSL. The drain select line DSL may be disposed over the word lines WL. A stack of the conductive patterns CP1 to CPn may be divided into multiple stacks by a slit SI.

[0073] The source select line SSL may be disposed to have a single layered or two or more layered structure below the word lines WL. Although, in the drawing, for example, the source select line SSL is configured by a first pattern CP1 that is disposed at a lowermost layer of the conductive patterns CP1 to CPn and a second pattern CP2 disposed over the first pattern CP1, the present disclosure is not limited to this.

[0074] The drain select line DSL may have a single layered or two or more layered structure and may be formed over the word lines WL. Although, in the drawing, for example, the drain select line DSL is configured by an n_m pattern CPn that is disposed at an uppermost layer of the conductive patterns CP1 to CPn and an $n-1_m$ pattern CPn-1 disposed below the n_m pattern CPn, the present disclosure is not limited to this.

[0075] The conductive patterns CP1 to CPn may be separated by the slit SI. Either the source select line SSL or the drain select line DSL may be divided into smaller units than that of the word lines WL. For example, each of the channel layers CH that are surrounded by each word line WL may be surrounded by drain select lines DSL. In this case, the drain select lines DSL may be separated from each other not only by the slit SI but also by an upper slit USI so that the width thereof is smaller than that of each of the word lines WL.

[0076] According to the configuration described with reference to FIGS. 2B and 2C, memory cells are formed at intersections between the channel layer CH and the word lines WL, a drain select transistor is formed at an intersection between the channel CH and the drain select line DSL, and a source select transistor is formed at an intersection between the channel layer CH and the source select line SSL. The source select transistor, the memory cells, and the drain select transistor that are arranged in a line along the single channel layer CH are coupled in series to each other through the channel layer CH and define a straight type memory string SCST. The word lines WL may transmit signals to gates of the memory cells. The source select line SSL may transmit a signal to a gate of the source select transistor. The drain select line DSL may transmit a signal to a gate of the drain select transistor.

[0077] Each of the memory cells of the memory string SCST described with reference to FIGS. 2B and 2C may

have the same structure as any one of the memory cells described with reference to FIGS. 1A to 1D.

[0078] FIGS. 3A to 3G are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure. Moreover, FIGS. 3A to 3G are sectional views illustrating a method for manufacturing the semiconductor device shown in FIG. 1A.

[0079] Referring to FIG. 3A, the interlayer insulating layers **101** and the sacrificial layers **103** are alternately stacked. The number by which the interlayer insulating layers **101** and the sacrificial layers **103** are stacked may be set to various values. The interlayer insulating layers **101** and the sacrificial layers **103** may be formed of different materials. Furthermore, the sacrificial layers **103** may be made of material having an etch selectivity with respect to the interlayer insulating layers **101**. For example, the interlayer insulating layers **101** may be made of oxide layers, and the sacrificial layers **103** may be made of nitride layers having an etch selectivity to the oxide layers.

[0080] Thereafter, the interlayer insulating layers **101** and the sacrificial layers **103** are etched to form a hole **105** passing through them. Subsequently, a buffer layer **111A** is formed on a sidewall of the hole **105**. The buffer layer **111A** may be made of material having an etch selectivity to the sacrificial layers **103**. For example, the buffer layer **111A** may be made of an oxide layer. Additionally, the buffer layer **111A** may be an oxide layer having p-type impurities. The buffer layer **111A** may be formed of a liner layer having a constant thickness. The buffer layer **111A** may be formed by depositing an oxide layer using an Atomic Layer Deposition (ALD) method. That is, the buffer layer **111A** may be formed using a deposition cycle including supplying a precursor and supplying an oxidizer. The deposition cycle may be repeated several times until the thickness of the buffer layer **111A** becomes a desired thickness. The precursor for forming the buffer layer **111A** may include silicon.

[0081] The buffer layer **111A** may function to prevent the interlayer insulating layers **101** from being densified when a following densification process is performed.

[0082] Referring to FIG. 3B, the buffer layer **111A** is densified, and thus a densified buffer layer **111B** in which a densified region is distributed is formed. The densification process is a process of curing dangling bonds in the buffer layer **111A** and may be embodied by a radical oxidation method, a heat treatment process, furnace annealing or laser annealing. When the curing process is performed at a high temperature, the dangling bonds in the buffer layer **111A** may be reduced by the curing. Process conditions of the curing process may be controlled such that the densified buffer layer **111B** has a density higher than that of the interlayer insulating layers **101**.

[0083] The densification process is targeted at the buffer layer **111A**. During the densification process, the interlayer insulating layers **101** are protected by the buffer layer **111A** so that the uniformity of the layer characteristics of the interlayer insulating layers **101** can be maintained. The densification process may be controlled such that the entirety of the buffer layer **111A** is densified. The degree to which the densified buffer layer **111B** is densified, that is, cured, may be increased toward the central region of the hole **105**. Due to this, the dangling bonds in the densified buffer layer **111B** may be decreased toward the central region of the hole **105**.

[0084] During the densification process, the interlayer insulating layers **101** and the sacrificial layers **103** may be protected by the buffer layer **111A**. When the interlayer insulating layers **101** and the sacrificial layers **103** are exposed to the curing process for densification, portions of sidewalls of the interlayer insulating layers **101** and the sacrificial layers **103** may be oxidized. In this case, since the interlayer insulating layers **101** and the sacrificial layers **103** are formed of different materials, they are oxidized to different thicknesses. As a result, an uneven surface structure may be formed on the sidewall of the hole **105**. According to the embodiment of the present disclosure, the interlayer insulating layers **101** and the sacrificial layers **103** can be prevented from being oxidized so that deformation of the sidewall of the hole **105** can be reduced.

[0085] Referring to FIG. 3C, a data storage layer **113** is formed on the densified buffer layer **111B**. The data storage layer **113** may be formed of a nitride layer capable of trapping charges. Thereafter, a tunnel insulating layer **115** is formed on the data storage layer **113**. The tunnel insulating layer **115** may be formed of a silicon oxide layer in which charge tunneling occurs. The data storage layer **113** and the tunnel insulating layer **115** may be formed in a liner shape along the sidewall of the hole **105**.

[0086] Subsequently, a channel layer **117** may be formed on the tunnel insulating layer **115**. The channel layer **117** may be formed of a semiconductor layer such as a silicon layer. The channel layer **117** may be formed in a hollow shape or formed in a pillar shape. When the channel layer **117** is formed in a hollow shape, a central region of the hollow channel layer **117** may be filled with a core insulating layer **119**.

[0087] Thereafter, the interlayer insulating layers **101** and the sacrificial layers **103** are etched to form a slit **121** passing through them.

[0088] Referring to FIG. 3D, the sacrificial layers **103** are removed through the slit **121**. When the sacrificial layers **103** are formed of nitride layers, phosphoric acid may be used to remove the sacrificial layers **103**.

[0089] As the sacrificial layers **103** are removed, first conductive areas **123A** that expose the densified buffer layer **111B** may be defined between the interlayer insulating layers **101** that are adjacent to each other with respect to the direction in which the channel layer **117** extends. In this case, each interlayer insulating layer **101** may remain with a first thickness **D1**.

[0090] When the sacrificial layers **103** are removed, the densified buffer layer **111B** having an etch selectivity to the sacrificial layers **103** may function as an etch stop layer and thus protect the data storage layer **113**.

[0091] Referring to FIG. 3E, the densified buffer layer **111B** exposed through the first conductive areas **123A** is etched such that the data storage layer **113** is exposed. In this case, portions of the interlayer insulating layers **101** are etched, whereby each interlayer insulating layer **101** may remain with a second thickness **D2** less than the first thickness **D1**. In this case, second conductive areas **123B**, each of which has a vertical width greater than that of each first conductive area (**123A** of FIG. 3D), may be defined between the interlayer insulating layers **101**. The data storage layers **113** are exposed by second conductive areas **123B**. The densified buffer layer (**111B** of FIG. 3D) may be divided into buffer patterns **111BP** by the second conductive areas **123B**.

[0092] While the densified buffer layer (1118 of FIG. 3D) is etched, the data storage layer 113 having an etch selectivity to the densified buffer layer (111B of FIG. 3D) may remain without being removed.

[0093] Referring to FIG. 3F, blocking insulating patterns BI are formed by oxidizing partial areas of the data storage layer (113 of FIG. 3e) exposed through the second conductive areas 123B. As a result, a data storage layer 113DL having an uneven surface structure may be formed. The data storage layer 113DL having the uneven surface structure may include a first area and a second area. The first area refers to portions of the data storage layer 113DL that contact the buffer patterns 111BP and remain with a first thickness W1. The second area refers to the other portions of the data storage layer 113DL which contact the blocking insulating patterns BI and remain with a second thickness W2 less than the first thickness W1.

[0094] Referring to FIG. 3G, conductive patterns 131 may be formed on the blocking insulating patterns BI such that the second conductive areas 123B between the interlayer insulating layers 101 are filled with the conductive patterns 131. Each conductive pattern 131 may include a polysilicon layer, a metal layer, a metal silicide layer, or a combination thereof. Low-resistance metal such as tungsten may be used as the material of a metal layer for forming the conductive patterns 131. Thereafter, the slit 121 may be filled with an insulating layer 141.

[0095] According to the embodiment of the present disclosure, the first conductive areas are defined by etching the densified buffer layer which has uniform layer characteristics. Therefore, according to the embodiment of the present disclosure, there is almost no etching rate difference while the densified buffer layer is etched, and thus the edges of the first conductive areas may be formed at a right angle or a substantially right angle.

[0096] FIGS. 4A and 4B are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure. In more detail, FIGS. 4A and 4B are sectional views illustrating a method for manufacturing the semiconductor device shown in FIG. 1B.

[0097] Referring to FIG. 4A, interlayer insulating layers 201 and sacrificial layers 203 that are respectively formed of the same materials as those described with reference to FIG. 3A are alternately stacked.

[0098] Thereafter, the interlayer insulating layers 201 and the sacrificial layers 203 are etched so as to form a hole 205 passing through them. Thereafter, a buffer layer is formed on the sidewall of the hole 205 using the same material and method as those described with reference to FIG. 3A.

[0099] Thereafter, a partial area of the buffer layer that is adjacent to the sidewall of the hole 205 remains as a non-densified area NDA, and the other area of the buffer layer is densified through a curing process. In this case, a densified area DA is formed in the buffer layer. The densified area DA may be formed to have a predetermined thickness from an exposed surface of the buffer layer. Thereby, the densified buffer layer 211 may include the densified area DA and the non-densified area NDA. The sidewall of the hole 205 may be spaced apart from the densified area DA by the non-densified area NDA.

[0100] The curing process for the densification may be embodied by a radical oxidation method, a heat treatment process, furnace annealing or laser annealing, as described

with reference to FIG. 3B. The densified area DA may have a smaller amount of dangling bonds than that of the interlayer insulating layers 201 or the non-densified area NDA. During the curing process for the densification, the interlayer insulating layers 201 and the sacrificial layers 203 may be protected by the buffer layer. Thereby, in the present embodiment, the interlayer insulating layers 201 and the sacrificial layers 203 can be prevented from being oxidized, so that deformation of the sidewall of the hole 205 can be reduced.

[0101] Referring to FIG. 48, a data storage layer 213, a tunnel insulating layer 215 and a channel layer 217 may be formed on the densified buffer layer 211 through the same processes as those described with reference to FIG. 3C. When the channel layer 217 is formed in a hollow shape, a central region of the hollow channel layer 217 may be filled with a core insulating layer 219.

[0102] Thereafter, the interlayer insulating layers 201 and the sacrificial layers (203 of FIG. 4A) are etched to form a slit 221 passing through them. Subsequently, the sacrificial layers (203 of FIG. 4A) are removed through the same process as that described with reference to FIG. 3D. The densified buffer layer (211 of FIG. 4A) is thereafter etched through the same process as that described with reference to FIG. 3E. Thereby, conductive areas 223 are defined between the interlayer insulating layers 201. The conductive areas 223 may expose partial areas of the data storage layer 213 and divide the densified buffer layer (211 of FIG. 4A) into buffer patterns 2118P.

[0103] While the densified buffer layer (211 of FIG. 4A) is etched, the data storage layer 213 having an etch selectivity to the densified buffer layer (211 of FIG. 4A) may remain without being removed. The densified buffer layer (211 of FIG. 4A) includes the densified area DA and the non-densified area NDA that have different etching rates from each other. Therefore, while the densified buffer layer (211 of FIG. 4A) is etched, the densified area DA having a relatively high density is etched at an etching rate lower than that of the non-densified area NDA. As a result, an edge EG of each conductive area 223 that is adjacent to the data storage layer 213 may be formed in a round shape.

[0104] Subsequently, the same processes as those described with reference to FIGS. 3F and 3G are performed, whereby blocking insulating patterns and conductive patterns may be formed. In this way, memory cells having the structure shown in FIG. 1B may be formed.

[0105] According to the foregoing embodiment of the present disclosure, the buffer patterns with edges having a desired round shape may be formed by controlling the thickness of the densified area formed in the densified buffer layer. Thereby, the embodiment of the present disclosure can control the shape of the edges of the buffer patterns such that the memory cell has optimized performance.

[0106] FIGS. 5A and 5B are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure. In more detail, FIGS. 5A and 5B are sectional views illustrating a method for manufacturing the semiconductor device shown in FIG. 1C.

[0107] Referring to FIG. 5A, interlayer insulating layers 301 and sacrificial layers 303 that are respectively formed of the same materials as those described with reference to FIG. 3A are alternately stacked.

[0108] Thereafter, the interlayer insulating layers **301** and the sacrificial layers **303** are etched to form a hole **305** passing through them. Subsequently, a buffer layer is formed on the sidewall of the hole **305** using the same material and method as those described with reference to FIG. 3A.

[0109] A curing process for densification is thereafter performed. The curing process may be performed such that the entire area of the buffer layer, partial areas of the respective interlayer insulating layers **301** that are adjacent to the buffer layer, and sidewalls of the respective sacrificial layers **303** that are adjacent to the buffer layer are densified. Thereby, the densified area DA may be formed in the entire area of the buffer layer, sidewalls of the respective interlayer insulating layers **301** that are adjacent to the buffer layer, and sidewalls of the respective sacrificial layers **303** that are adjacent to the buffer layer.

[0110] A densified buffer layer **311B**, a first densified sidewall **301B** of each interlayer insulating layer **301**, and a second densified sidewall **303B** of each sacrificial layer **303** may be formed by a radical oxidization method.

[0111] Referring to FIG. 5B, a data storage layer **313**, a tunnel insulating layer **315** and a channel layer **317** may be formed on the densified buffer layer **311B** through the same processes as those described with reference to FIG. 3C. When the channel layer **317** is formed in a hollow shape, a central region of the hollow channel layer **317** may be filled with a core insulating layer **319**.

[0112] Thereafter, the interlayer insulating layers **301** and the sacrificial layers (**303** of FIG. 5A) are etched to form a slit **321** passing through them. The sacrificial layers (**303** of FIG. 5A) are thereafter removed through the same process described with reference to FIG. 3D. Subsequently, the second densified sidewall (**303B** of FIG. 5A) is etched. In this case, the edge of the first densified sidewall **301B** may be etched to have a round shape by a difference in etching rate due to a difference in material characteristics between the first densified sidewall **301B** and the second densified sidewall (**303B** of FIG. 5A). Thereafter, the densified buffer layer (**311B** of FIG. 5A) is etched. Thereby, conductive areas **323** are defined between the interlayer insulating layers **301**. The conductive areas **323** may expose partial areas of the data storage layer **313** and divide the densified buffer layer (**311B** of FIG. 5A) into buffer patterns **311BP**. The buffer patterns **311BP** and the first densified sidewall **301B** remain as the densified area DA.

[0113] Subsequently, the same processes as those described with reference to FIGS. 3F and 3G are performed, whereby blocking insulting patterns and conductive patterns are formed. In this way, memory cells having the structure shown in FIG. 1C may be formed.

[0114] According to the foregoing embodiment of the present disclosure, the conductive areas with edges having a desired round shape may be formed by controlling the thickness of the densified area formed in the sidewalls of the interlayer insulating layers. Thereby, the embodiment of the present disclosure can control the shape of the edges of the conductive areas such that the memory cell has optimized performance.

[0115] FIGS. 6A and 6B are sectional views illustrating a method for manufacturing a semiconductor device in accordance with an embodiment of the present disclosure. Moreover, FIGS. 6A and 6B are sectional views illustrating a method for manufacturing the semiconductor device shown in FIG. 1D.

[0116] Referring to FIG. 6A, interlayer insulating layers **401** and sacrificial layers **403**, that are respectively formed of the same materials as those described with reference to FIG. 3A, are alternately stacked.

[0117] Thereafter, the interlayer insulating layers **401** and the sacrificial layers **403** are etched to form a hole **405** passing through them. Subsequently, a buffer layer is formed on the sidewall of the hole **405** using the same material and method as those described with reference to FIG. 3A.

[0118] A curing process for densification is thereafter performed. The curing process may be performed such that the entire area of the buffer layer and partial areas of the respective interlayer insulating layers **401** that are adjacent to the buffer layer are densified. Thereby, the densified area DA may be distributed in the entire area of the buffer layer, and sidewalls of the respective interlayer insulating layers **401** that are adjacent to the buffer layer.

[0119] A densified buffer layer **411B** and densified sidewalls **401B** of the respective interlayer insulating layers **401** may be processed by a heat treatment process, furnace annealing or laser annealing. The heat treatment process, the furnace annealing or the laser annealing may be controlled such that the sacrificial layers **403** formed of nitride layers are prevented from being oxidized.

[0120] Referring to FIG. 6B, a data storage layer **413**, a tunnel insulating layer **415** and a channel layer **417** may be formed on the densified buffer layer **411B** through the same processes as those described with reference to FIG. 3C. When the channel layer **417** is formed in a hollow shape, a central region of the hollow channel layer **417** may be filled with a core insulating layer **419**.

[0121] Thereafter, the interlayer insulating layers **401** and the sacrificial layers (**403** of FIG. 6A) are etched to form a slit **421** passing through them. Subsequently, the sacrificial layers (**403** of FIG. 6A) are removed through the same process as that described with reference to FIG. 3D. The densified buffer layer (**411B** of FIG. 6A) is thereafter etched through the same process as that described with reference to FIG. 3E. Thereby, conductive areas **423** are defined between the interlayer insulating layers **401**. According to the embodiment of the present disclosure, since there is almost no etching rate difference in the densified buffer layer while the densified buffer layer (**411B** of FIG. 6A) is etched, the edges of the conductive areas **423** may be formed at a right angle or a substantially right angle.

[0122] The conductive areas **423** may expose partial areas of the data storage layer **413** and divide the densified buffer layer (**411B** of FIG. 6A) into buffer patterns **411BP**. The buffer patterns **411BP** and the densified sidewall **401B** remain as the densified area DA.

[0123] Subsequently, the same processes as those described with reference to FIGS. 3F and 3G are performed, whereby blocking insulting patterns and conductive patterns are formed. In this manner, memory cells having the structure shown in FIG. 1D may be formed.

[0124] According to the foregoing embodiment of the present disclosure, the conductive areas with the edges having a right-angled shape may be formed using the curing process through which the sacrificial layers are not oxidized.

[0125] In the above-mentioned embodiments of the present disclosure, a range within which a densified area is formed is quantitatively controlled, whereby conductive areas with edges having various shapes can be defined.

Therefore, the shape of the edges of the conductive areas can be controlled such that memory cells have optimized performance.

[0126] FIG. 7 is a block diagram illustrating a memory system according to an embodiment of the present disclosure. Referring FIG. 7, the memory system **1100** according to the embodiment includes a memory device **1120** and a memory controller **1110**.

[0127] The memory device **1120** may include at least one of the memory cells described with reference to FIGS. 1A to 1D. The memory device **1120** may include at least one of the memory strings described with reference to FIGS. 2A to 2C. Each memory string may include at least one of the memory cells having the structures described with reference to FIGS. 1A to 1D. The memory cells may be formed through the processes described with reference to FIGS. 3A to 3G, the processes described with reference to FIGS. 4A and 4B, the processes described with reference to FIGS. 5A and 5B, or the processes described with reference to FIGS. 6A and 6B. The memory device **1120** may be a multi-chip package including a plurality of memory chips.

[0128] The memory controller **1110** is configured to control the memory device **1120**, and may include a Static Random Access Memory (SRAM) **1111**, a CPU **1112**, a host interface **1113**, an Error Correction Code (ECC) **1114**, and a memory interface **1115**. The SRAM **1111** is used as an operation memory of the CPU **1112**. The CPU **1112** performs general control operations for data exchange of the memory controller **1110**. The host interface **1113** is provided with a data interchange protocol of a host and is coupled with the memory system **1100**. Furthermore, the ECC **1114** detects and corrects an error included in the data that is read from the memory device **1120**, and the memory interface **1115** interfaces with the memory device **1120**. In addition, the memory controller **1110** may further include a Read Only Memory (ROM) or the like that stores code data for interfacing with the host.

[0129] The above-described memory system **1100** may be a memory card or a Solid State Disk (SSD) equipped with the memory device **1120** and the controller **1110**. For example, when the memory system **1100** is an SSD, the memory controller **1110** may communicate with the outside for example, a host via one of various interface protocols, such as an Universal Serial Bus (USB), a MultiMedia Card (MMC), a Peripheral Component Interconnection-Express (PCI-E), a Serial Advanced Technology Attachment (SATA), a Parallel Advanced Technology Attachment (PATA), a Small Computer Small Interface (SCSI), an Enhanced Small Disk Interface (ESDI), or an Integrated Drive Electronics (IDE).

[0130] FIG. 8 is a block diagram illustrating a computing system in accordance with an embodiment of the present disclosure. Referring to FIG. 8, the computing system **1200** in accordance with the embodiment of the present disclosure may include a CPU **1220**, a Random Access Memory (RAM) **1230**, a user interface **1240**, a modem **1250**, and a memory system **1210** that are electrically coupled to a system bus **1260**. Furthermore, if the computing system **1200** is a mobile device, it may further include a battery for supplying operating voltage to the computing system **1200**. An application chip set, a camera image processor CIS, a mobile DRAM and the like may be further included.

[0131] As described above with reference to FIG. 7, the memory system **1210** may be configured with the memory device **1212** and the memory controller **1211**.

[0132] In the embodiments of the present disclosure, the thickness of the densified area may be quantitatively controlled by defining the densified area after the buffer layer has been formed. Thereby, in the embodiments of the present disclosure, the edge of the conductive area defined between the interlayer insulating layers may be formed in a desired shape. Since the profile of the conductive pattern is defined depending on the shape of the edge of the conductive area, the profile of the conductive pattern according to the embodiments of the present disclosure may be formed in a desired shape.

[0133] In the embodiments of the present disclosure, the thickness of the densified area can be quantitatively controlled such that the shape of the edge of the conductive pattern is formed in a shape capable of optimizing the operational reliability of the semiconductor device. Therefore, the operational reliability of the semiconductor device may be improved.

[0134] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and are not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

1. A manufacturing method for a semiconductor device, comprising:

- alternately stacking first layers and second layers;
- forming a hole passing through the first layers and the second layers;
- forming a buffer layer over a sidewall of the hole;
- forming a first densified area in the buffer layer;
- forming a second densified area in a partial area of each of the first layers;
- forming a third densified area in a partial area of each of the second layers;
- forming a data storage layer over the first densified area; and
- forming a channel layer over the data storage layer.

2. The manufacturing method according to claim 1, wherein the forming of the buffer layer comprises:

- forming an oxide layer using an Atomic Layer Deposition (ALD) method.

3. The manufacturing method according to claim 1, wherein the first densified area is formed by curing dangling bonds in the buffer layer, and

- wherein the curing is performed by a radical oxidation method, a heat treatment process, furnace annealing, laser annealing, or a combination thereof.

4. The manufacturing method according to claim 1, wherein the first densified area is formed by curing dangling bonds in the buffer layer, and

- wherein curing is performed such that an entire area of the buffer layer is formed of the first densified area.

5. The manufacturing method according to claim 1, wherein the first densified area is formed by curing dangling bonds in the buffer layer, and

wherein curing is controlled such that a non-densified area is defined in the buffer layer between the first densified area and the sidewall of the hole.

6. The manufacturing method according to claim 1, wherein an entire area of the buffer layer is formed of the first densified area in the buffer layer, and wherein the second densified area extends from the first densified area into the partial area of each of the first layers.

7. The manufacturing method according to claim 6, wherein the third densified area extends from the first densified area into the partial area of each of the second layers.

8. The manufacturing method according to claim 1, further comprising:

forming a tunnel insulating layer between the data storage layer and the channel layer.

9. The manufacturing method according to claim 8, further comprising:

etching the first layers and the second layers to form a slit; removing the second layers through the slit to expose the buffer layer;

removing the exposed buffer layer to form buffer patterns and conductive areas, wherein each of the conductive areas exposes the data storage layer, wherein each of

the conductive areas is defined by two neighboring first layers and the exposed data storage layer;

oxidizing the exposed data storage layer to form blocking insulating patterns in the conductive areas, respectively; and

forming conductive patterns over the blocking insulating patterns to fill the conductive areas, respectively.

10. The manufacturing method according to claim 9, wherein each of the conductive areas has a first edge, wherein the first edge is defined by each of the buffer pattern and the exposed data storage layer, and wherein the first edge is right-angled.

11. The manufacturing method according to claim 9, wherein each of the conductive areas has a first edge, wherein the first edge is defined by each of the buffer pattern and the exposed data storage layer, and wherein the first edge is rounded.

12. The manufacturing method according to claim 1, wherein the buffer layer has a different etch selectivity from the second layers.

13. The manufacturing method according to claim 1, wherein the buffer layer has a different etch selectivity from the data storage layer.

14. The manufacturing method according to claim 1, wherein the first densified area is formed by curing dangling bonds in the buffer layer.

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