Aemulus

# DM483e

## Specifications

*Version 1.0, 08-2014*

## Table of Contents

## Section 1: Specification Conditions

This document contains the specifications and supplemental information of DM483e high speed digital waveform generator and analyzer with integrated pin electronics (PE) and per pin parametric measurement unit (PPMU) functions.

Specifications are the standards against which the DM483e is tested. Upon leaving the factory the DM483e meets these specifications. Supplemental and typical values are non-warranted, apply at 23°C, and are provided solely as useful information. Specifications are subject to change without notice.

The source and measurement accuracies are specified at the terminals under the following conditions:

1. Ambient temperature 23°C ± 5°C
2. After 30 minutes warm-up
3. 1 PLC aperture time, unless otherwise stated
4. Remote sense operation
5. Calibration period: 6 months

## Section 2: Pin Specifications

### 2.1 General

| Specification | Value | Comments |
|---|---|---|
| Number of data pins | 12 pins of Pin Measurement unit (PMU) enabled | |
| Direction control of data pins | Per pin | |
| Number of remote sense pins | 12 | All PMU-enabled pins have remote sense capability |

### 2.2 Digital Generation/Output Pins

| Specification | Value | Comments |
|---|---|---|
| Generation Signal Type | Single-ended, ground reference | |
| Programmable generation voltage levels | Drive Voltage High Level (VIH)<br>Drive Voltage High Level (VIL)<br>Drive Termination Voltage (VT) | |
| Generation voltage range | -2V to 6V | |
| Accuracy | 0.25% of value + 20mV | |
| Generation voltage resolution | 100uV | |
| Generation voltage swing | 400mV to 8V | |
| Output Impedance | 50Ω | Nominal |
| Maximum allowed DC drive per pin | ±50mA | Nominal |
| Data pin tristate control | Per pin, per cycle | |
| Pin power-on state | Drivers disabled, high impedance (tri-state) | |
| Output protection | The device can sustain a short to any voltage between -2V and 6V provided that you observe the maximum drive strength limitations | |

## 2.3 Digital Acquisition/Input Pins

| Specification | Value | Comments |
|---|---|---|
| Acquisition Signal Type | Single-ended, ground reference | |
| Programmable acquisition voltage levels | Compare High Level (VOH)<br>Compare High Level (VOL)<br>Voltage Termination (VT) | |
| Acquisition voltage threshold | -2V to 7V | |
| Accuracy (VOH, VOL) | 0.25% of value + 20mV | |
| Accuracy (VT) | 0.25% of value + 20mV | |
| Termination voltage resolution | 600 uV | |
| Termination voltage range | 0V to 6.5V | |
| Minimum detectable voltage swing | 10mV | |
| Input impedance | High Impedance or 50Ω terminated into VT | |
| Input protection | The device can sustain a short to any voltage between -2V and 6V provided that you observe the maximum drive strength limitations | |

## 2.4 Active Load Pins

| Specification | Value | | Comments |
|---|---|---|---|
| Programmable levels | Current Source (IOH)<br>Current Sink (IOL) | | |
| Load | Range | Resolution | |
| | -12 mA to +12mA | 7 uA | |

## 2.5 High Voltage (HV) Pins

| Specification | Value | | Comments |
|---|---|---|---|
| Generation Signal Type | Single-ended, ground reference | | |
| Number of pins | 6 | | |
| Programmable levels | Force voltage | | HV = (VT + 1) x 2 |
| Force Voltage | Range | Accuracy | |
| | 0V to 15V | 1.5% of value + 450mV | |

## 2.6 Others

| Specification | Value | Comments |
|---|---|---|
| Clamp Voltage Range High Side (VCH) | -1.0V to 6.0V | |
| Clamp Voltage Range Low Side (VCL) | -1.5V to 5.0V | |
| Termination Voltage (VT) | -2.0V to 6.0V | |

## 2.7 PPMU Pins

| Specification | Value | | | Comments |
|---|---|---|---|---|
| Programmable levels | Force voltage (FV)<br>Force current (FI)<br>Voltage clamp high (VCH)<br>Voltage clamp low (VCL) | | | Voltage clamps are only active when forcing current |
| Force voltage (FV) | Range | Accuracy | Resolution | Maximum accuracy at the sense location with 1 50Hz PLC aperture |
| | -2V to 6V | 0.1% of value<br>+<br>0.1% of range | 800uV | |
| Force voltage rise time (no load) | Range | Settling time | | Typical rise time from 10% to 90% of the final value, 6V |
| | 2uA | 301us | | |
| | 20uA | 27us | | |
| | 200uA | 6.6us | | |
| | 2mA | 6.24us | | |
| | 25mA | 6.55us | | |
| Force voltage rise time (1nF load) | Range | Settling time | | Typical rise time from 10% to 90% of the final value, 6V |
| | 20uA | 264us | | |
| | 200uA | 24.4us | | |
| | 2mA | 6.6us | | |
| | 25mA | 6.46us | | |
| Load capacitance | Range | Capacitance | | These value represent the allowed load capacitance through a 1m SHC68-C68-D4 VHDCI cable to ensure a well-behaved transient response, <300us rise time. |
| | 20uA | 1nF | | |
| | 200uA | 10nF | | |
| | 2mA | 50nF | | |
| | 25mA | 50nF | | |
| Force current (FI) | Range | Accuracy | Resolution | Maximum accuracy at the sense location with 1 50Hz PLC |
| | ± 2uA | 0.25% of value<br>+<br>0.25% of range | 500pA | |
| | ± 20uA | | 6.3nA | |
| | ± 200uA | | 60nA | |

| | | | | |
|---|---|---|---|---|
| | ± 2mA | | 800nA | aperture |
| | ± 25mA | | 14uA | |
| Aperture time range | 1.25us to 200ms | | | |
| Aperture resolution | 1.25us | | | |
| Measure voltage | Range | Accuracy | Resolution | Maximum accuracy at the sense location with 1 50Hz PLC aperture |
| | -2V to 6V | 0.1% of value + 0.1% of range | 150uV | |
| Measure current | Range | Accuracy | Resolution | Maximum accuracy at the sense location with 1 50Hz PLC aperture |
| | ± 2uA | 0.25% of value + 0.25% of range | 8nA | |
| | ± 20uA | | 8nA | |
| | ± 200uA | | 30nA | |
| | ± 2mA | | 450nA | |
| | ± 25mA | | 9uA | |
| Voltage clamp high (VCH) | Range | 0V to 6V | | |
| Voltage clamp low (VCL) | Range | -2V to 4V | | |
| Maximum temperature at PPMU pin under Full Load | 85 °C | | | Fan set to HIGH speed. 240Ω/1W resistor is connected across each PMU channels FH and FL for all 12 pins. DVCI at 6V/25mA (12 hours duration). |

### 2.7.1 Typical Step Response


Figure 1: PMU Characteristic Step Response into a Capacitive Load 1nF in the 25mA

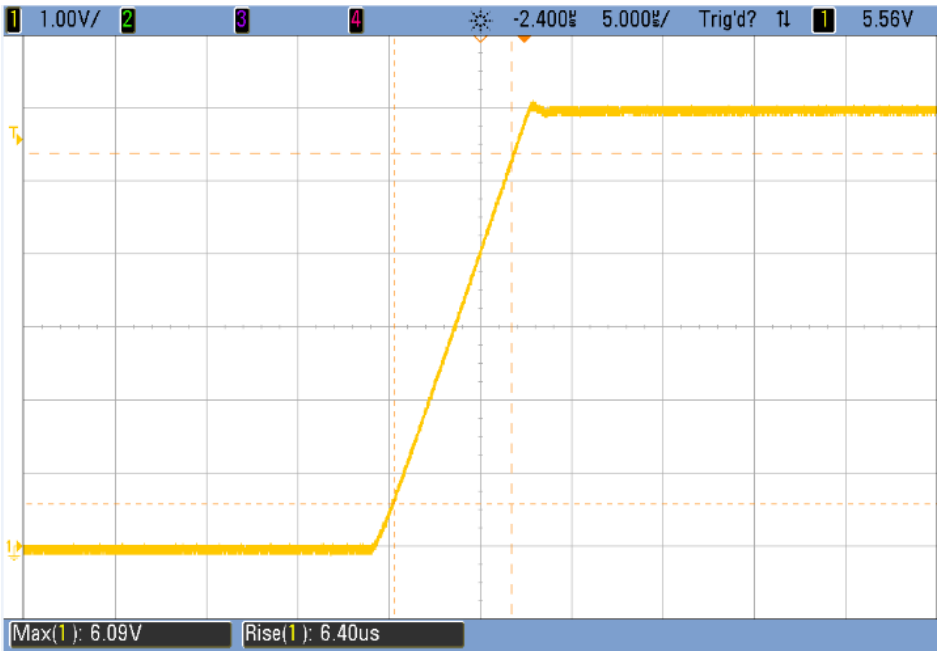


Figure 2: PMU Characteristic Step Response into a Capacitive Load 10nF in the 25mA


Figure 3: PMU Characteristic Step Response into a Capacitive Load 50nF in the 25mA

### 2.7.2 Noise and Resolution vs. Measurement Aperture

The following figure illustrates typical noise and resolution as a function of measurement aperture for the PMU.

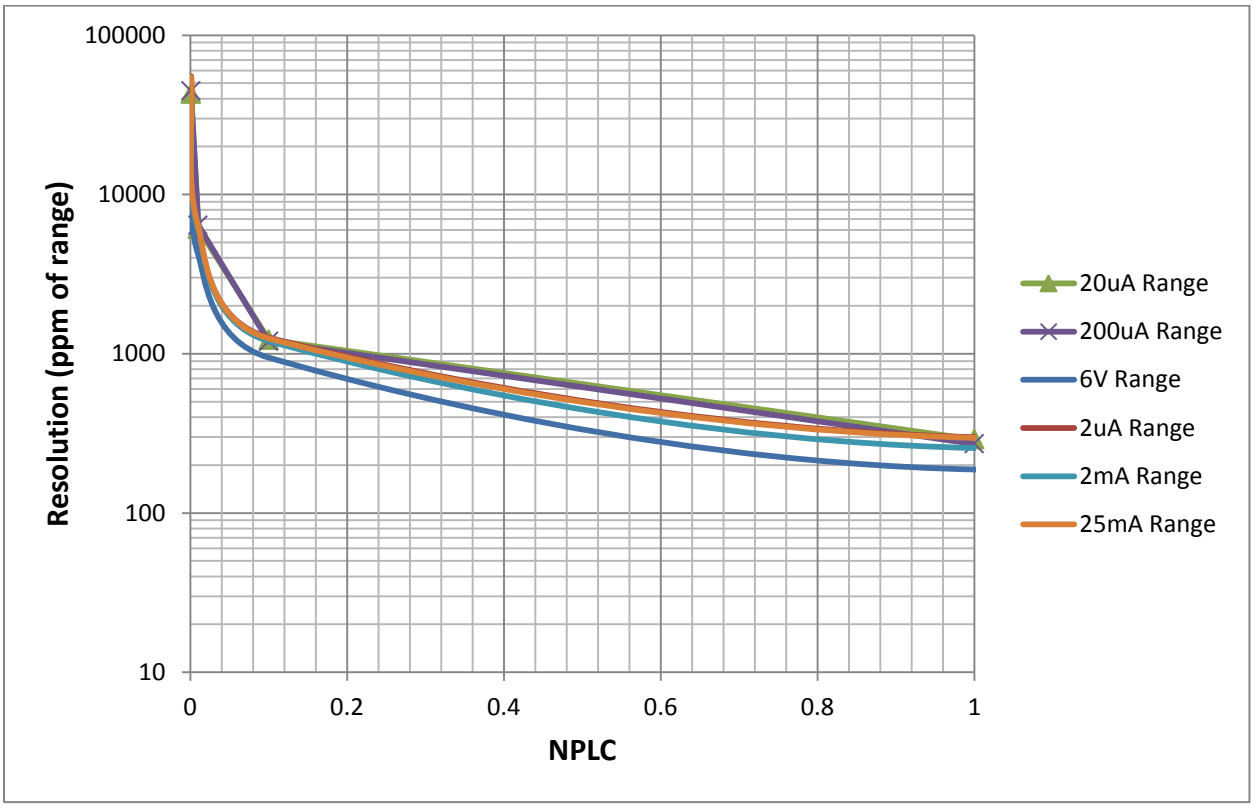


Figure 4: Resolution VS NPLC

To derive a resolution in absolute units, complete the following steps:

- Select a voltage or current range.
- For a given aperture time, find the corresponding resolution.
- To convert resolution from ppm of range to absolute units, multiply resolution in ppm of range by the selected range.

For example, the DM483e has a resolution of 200ppm when set to a 1 PLC. In the 6V range, resolution can be calculated by multiplying 6V by 200ppm, as shown in the following example:

6V * 200ppm = 6 * 200 * 1×10–6 = 1.2mV

Likewise, in the 2mA range, resolution can be calculated by multiplying 2mA by 300ppm, as shown in the following example:

2mA * 300ppm = 2mA * 300 * 1×10–6 = 600nA

## Section 3: Timing Specifications

### 3.1 Vector Rate

| Specification | Value | Comments |
|---|---|---|
| Vector clock source | Onboard Clock | |
| Frequency Range | 1kHz to 200MHz | |
| Frequency resolution | <0.1Hz | |
| Frequency accuracy | 0.015% of value | |

### 3.2 Generation/Output Timing

| Specification | Value | Comments |
|---|---|---|
| Maximum data rate per pin | 200Mbps | |
| Maximum data pin toggle rate | 100Mhz | |
| Data pin to pin skew | Maximum : ±500ps | |
| Output self-tune delay | NA | |

### 3.3 Acquisition/Input Timing

| Specification | Value | Comments |
|---|---|---|
| Maximum data rate per pin | 200Mbps | |
| Maximum data pin toggle rate | 100Mhz | |
| Data position mode | Delay from sample clock rising edge | |
| Input data delay frequency | All supported frequencies | |
| Input delay adjustment | ±25 Sample clock cycles expressed as a time in seconds. | |
| Input self-tune delay | 1ns | |
| Input data delay resolution | 11ps | |

## Section 4: Waveform Specifications

| Specification | Value | Comments |
|---|---|---|
| On-board memory size (generation) | 16 Mbit/pin | |
| On-board memory size (acquisition) | 16 Mbit/pin | History RAM |
| Generation mode | Clock mode | Generate continuous clock outputs |
| | Vector mode | Generate a sequence of waveforms.<br>Use vector file (*.vec) to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to output triggers. |
| Number of vector set per DM483e | 32 | |
| Number of timing set per DM483e | 32 | |
| Maximum data rate | 200Mbps | This applies to all pins |

## Section 5: Triggers

### 5.1 Trigger Inputs

| Specification | Value | Comments |
|---|---|---|
| Sources | PXI trigger lines | PXI_TRIG[0:7]<br>PXI_STAR<br>PXI_LBL6<br>PXI_LBR6<br>PXIE_DSTARA<br>PXIE_DSTARB |
| | Software trigger | |
| | External trigger 0-1 | Can be used to trigger vector engine to start driving vector |
| Polarity | High, Low, Rising, Falling | Configurable |
| Pulse Width | >=200ns | |

### 5.2 Trigger Outputs

| Specification | Value | Comments |
|---|---|---|
| Sources | PXI trigger lines | PXI_TRIG[0:7]<br>PXI_STAR<br>PXI_LBL6<br>PXI_LBR6 |
| | External trigger 0-1 | External trigger 0-1 (t0, t1) can be used in vector mode. When running in dual-site mode, trigger 0 is for site 0 whereas trigger 1 is for site 1. |
| Polarity | Active High | |
| Pulse Width | 1us to 10ms | Configurable |

## Section 6: MIPI RFFE

| Specification | Value | | Comments |
|---|---|---|---|
| Number of MIPI RFFE Controllers | 4 | | 2 MIPI RFFE controllers available for each pin group |
| Full-Speed Clock Frequency | Minimum | 32kHz | |
| | Maximum | 26MHz | |

## Section 7: Others

1. Output

   Front Panel Connectors: 68 position VHDCI receptacle

2. Dimension: 3U 1-slot space

## Section 8: Revision History

| | | |
|---|---|---|
| 1.0 | AUG 2014 | INITIAL RELEASE |

## Section 9: Contact Us

To obtain service, warranty or technical assistance, please contact Aemulus.

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Product specifications and descriptions in this document are subject to change without prior notice.