Aemulus

DM482e

Specifications

Version 1.5, 06-2014

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Section 1: Specification Conditions

This document contains the specifications and supplemental information of DM482e high speed digital waveform generator and analyzer with integrated pin electronics (PE) and per pin parametric measurement unit (PPMU) functions.

Specifications are the standards against which the DM482e is tested. Upon leaving the factory the DM482e meets these specifications. Supplemental and typical values are non-warranted, apply at 23°C, and are provided solely as useful information. Specifications are subject to change without notice.

The source and measurement accuracies are specified at the terminals under the following conditions:

1. Ambient temperature 23°C ± 5°C
2. After 30 minutes warm-up
3. 1 PLC aperture time, unless otherwise stated
4. Remote sense operation
5. Calibration period: 6 months

Section 2: Pin Specifications

2.1 General

Specification	Value	Comments
Number of data pins	12 pins of Pin Measurement unit (PMU) enabled	
Direction control of data pins	Per pin	
Number of remote sense pins	12	All PMU-enabled pins have remote sense capability

2.2 Digital Generation/Output Pins

Specification	Value	Comments
Generation Signal Type	Single-ended, ground reference	
Programmable generation voltage levels	Drive Voltage High Level (VIH) Drive Voltage High Level (VIL) Drive Termination Voltage (VT)	
Generation voltage range	-2V to 6V	
Generation voltage resolution	100uV	
Generation voltage swing	400mV to 8V	
Accuracy	0.25% of value + 20mV	
Output Impedance	50Ω	Nominal
Maximum allowed DC drive per pin	±50mA	Nominal
Data pin tristate control	Per pin, per cycle	
Pin power-on state	Drivers disabled, high impedance (tri-state)	
Output protection	The device can sustain a short to any voltage between -2V and 6V provided that you observe the maximum drive strength limitations	

2.3 Digital Acquisition/Input Pins

Specification	Value	Comments
Acquisition Signal Type	Single-ended, ground reference	
Programmable acquisition voltage levels	Compare High Level (VIH) Compare High Level (VIL) Voltage Termination (VT)	
Acquisition voltage threshold	-2V to 7V	
Accuracy (VOL, VOH)	0.25% of value + 20mV	
Termination voltage resolution	600 uV	
Termination voltage range	0V to 15V	
Accuracy (VT)	0.25% of value + 20mV	
Minimum detectable voltage swing	10mV	
Input impedance	High Impedance or 50Ω terminated into VT	
Input protection	The device can sustain a short to any voltage between -2V and 6V provided that you observe the maximum drive strength limitations	

2.4 Active Load Pins

Specification	Value		Comments
Programmable levels	Current Source (IOH) Current Sink (IOL)		
Load	Range	Resolution	
	-12 mA to +12mA	7 uA	

2.5 Others

Specification	Value	Comments
Clamp Voltage Range High Side (VCH)	-1.0V to 6.0V	
Clamp Voltage Range Low Side (VCL)	-1.5V to 5.0V	
Termination Voltage (VT)	-2.0V to 6.0V	

2.6 High Voltage Driver

Specification	Value	Comments
Voltage Range	0V to 13.5V	Only available at even-numbered pins (0, 2, 4, 6, 8, 10)
Accuracy	1.5% of value + 450mV	

2.7 PPMU Pins

<table>
<tr><td>Specification</td><td colspan="3">Value</td><td>Comments</td></tr>
<tr><td>Programmable levels</td><td colspan="3">Force voltage (FV)
Force current (FI)
Voltage clamp high (VCH)
Voltage clamp low (VCL)</td><td>Voltage clamps are only active when forcing current</td></tr>
<tr><td rowspan="2">Force voltage (FV)</td><td>Range</td><td>Accuracy</td><td>Resolution</td><td rowspan="2">Maximum accuracy at the sense location with 1 50Hz PLC aperture</td></tr>
<tr><td>-2V to 6V</td><td>0.1% of value
+
0.1% of range</td><td>800uV</td></tr>
<tr><td rowspan="6">Force voltage rise time (no load)</td><td>Range</td><td colspan="2">Settling time</td><td rowspan="6">Typical rise time from 10% to 90% of the final value, 6V</td></tr>
<tr><td>2uA</td><td colspan="2">301us</td></tr>
<tr><td>20uA</td><td colspan="2">27us</td></tr>
<tr><td>200uA</td><td colspan="2">6.6us</td></tr>
<tr><td>2mA</td><td colspan="2">6.24us</td></tr>
<tr><td>25mA</td><td colspan="2">6.55us</td></tr>
<tr><td rowspan="5">Force voltage rise time (1nF load)</td><td>Range</td><td colspan="2">Settling time</td><td rowspan="5">Typical rise time from 10% to 90% of the final value, 6V</td></tr>
<tr><td>20uA</td><td colspan="2">264us</td></tr>
<tr><td>200uA</td><td colspan="2">24.4us</td></tr>
<tr><td>2mA</td><td colspan="2">6.6us</td></tr>
<tr><td>25mA</td><td colspan="2">6.46us</td></tr>
<tr><td rowspan="5">Load capacitance</td><td>Range</td><td colspan="2">Capacitance</td><td rowspan="5">These value represent the allowed load capacitance through a 1m SHC68-C68-D4 VHDCI cable to ensure a well-behaved transient response, <300us rise time.</td></tr>
<tr><td>20uA</td><td colspan="2">1nF</td></tr>
<tr><td>200uA</td><td colspan="2">10nF</td></tr>
<tr><td>2mA</td><td colspan="2">50nF</td></tr>
<tr><td>25mA</td><td colspan="2">50nF</td></tr>
<tr><td rowspan="4">Force current (FI)</td><td>Range</td><td>Accuracy</td><td>Resolution</td><td rowspan="4">Maximum accuracy at the sense location with 1 50Hz PLC</td></tr>
<tr><td>± 2uA</td><td rowspan="3">0.25% of value
+
0.25% of range</td><td>500pA</td></tr>
<tr><td>± 20uA</td><td>6.3nA</td></tr>
<tr><td>± 200uA</td><td>60nA</td></tr>
</table>

	± 2mA		800nA	aperture
	± 25mA		14uA	
Aperture time range	1.25us to 200ms			
Aperture resolution	1.25us			
Measure voltage	Range	Accuracy	Resolution	Maximum accuracy at the sense location with 1 50Hz PLC aperture
	-2V to 6V	0.1% of value + 0.1% of range	150uV	
Measure current	Range	Accuracy	Resolution	Maximum accuracy at the sense location with 1 50Hz PLC aperture
	± 2uA	0.25% of value + 0.25% of range	8nA	
	± 20uA		8nA	
	± 200uA		30nA	
	± 2mA		450nA	
	± 25mA		9uA	
Voltage clamp high (VCH)	Range	0V to 6V		
Voltage clamp low (VCL)	Range	-2V to 4V		
Typical board temperature at Full Load	Initial: 45 °C Typical: 65 °C			Fan set to HIGH speed. FH and FL shorted for all 12 PMU channels. DICV at 25mA and 6V (12 hours duration). Board temperature will stabilize at 65°C

2.7.1 Typical Step Response

Figure 1: PMU Characteristic Step Response into a Capacitive Load 1nF in the 25mA

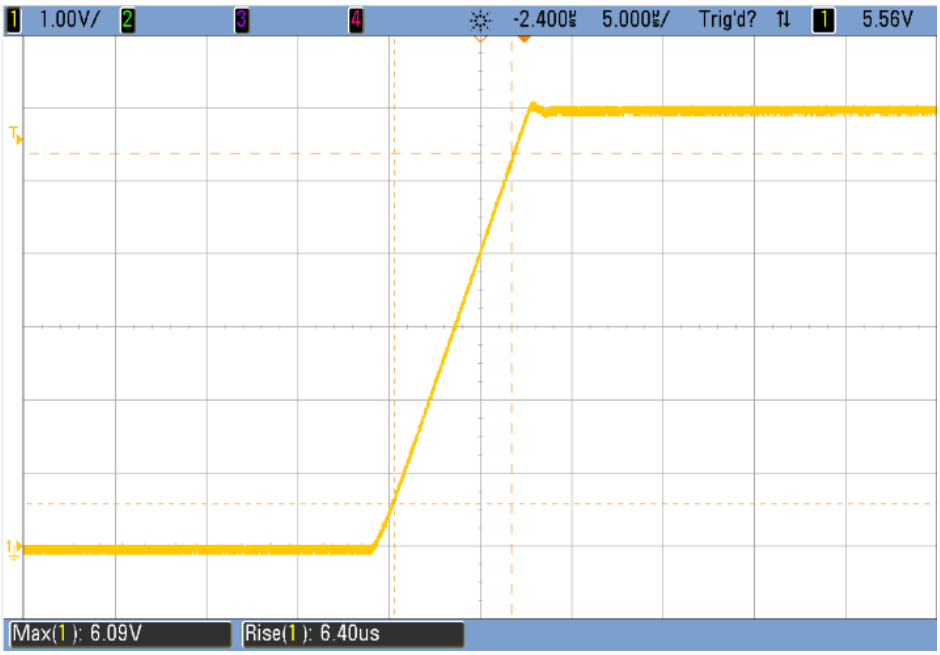

Figure 2: PMU Characteristic Step Response into a Capacitive Load 10nF in the 25mA

Figure 3: PMU Characteristic Step Response into a Capacitive Load 50nF in the 25mA

2.7.2 Noise and Resolution vs. Measurement Aperture

The following figure illustrates typical noise and resolution as a function of measurement aperture for the PMU.

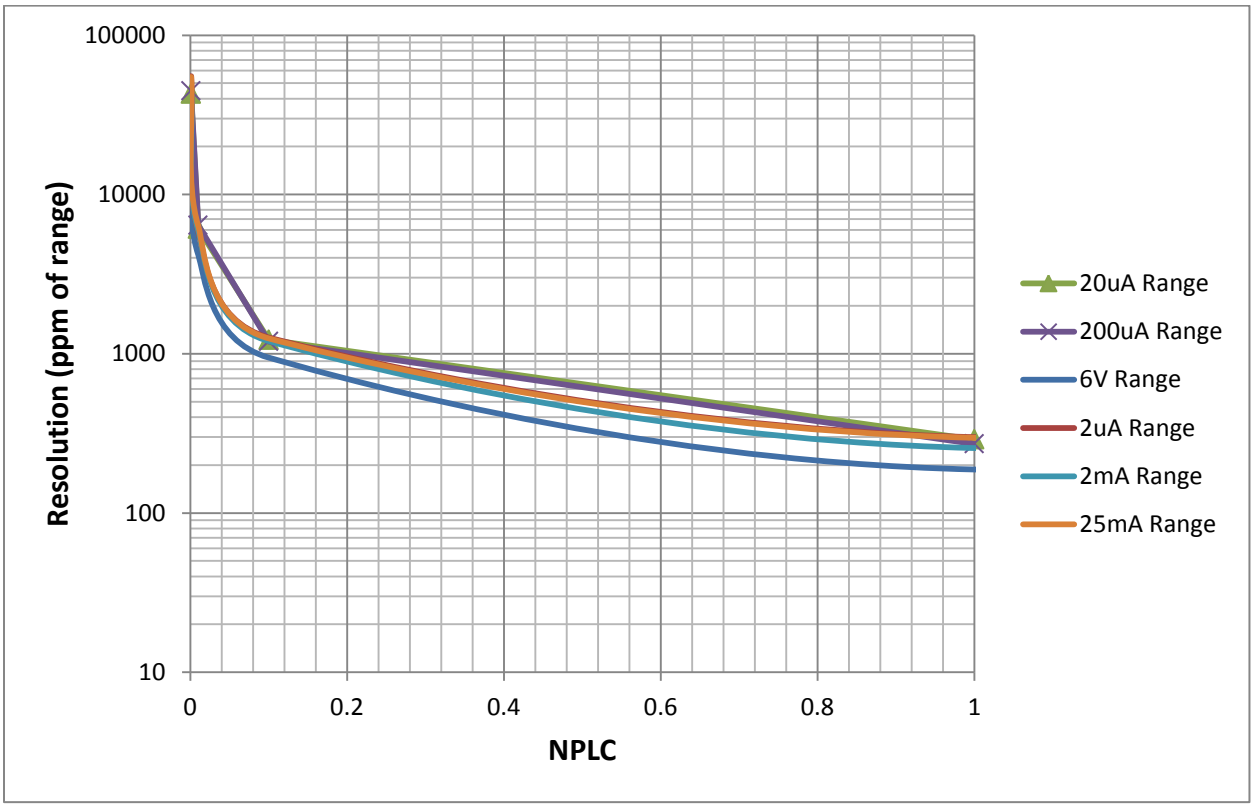

Figure 4: Resolution VS NPLC

To derive a resolution in absolute units, complete the following steps:

- Select a voltage or current range.
- For a given aperture time, find the corresponding resolution.
- To convert resolution from ppm of range to absolute units, multiply resolution in ppm of range by the selected range.

For example, the DM482e has a resolution of 200ppm when set to a 1 PLC. In the 6V range, resolution can be calculated by multiplying 6V by 200ppm, as shown in the following example:

6V * 200ppm = 6 * 200 * 1×10–6 = 1.2mV

Likewise, in the 2mA range, resolution can be calculated by multiplying 2mA by 300ppm, as shown in the following example:

2mA * 300ppm = 2mA * 300 * 1×10–6 = 600nA

Section 3: Timing Specifications

3.1 Vector Rate

Specification	Value	Comments
Vector clock source	Onboard Clock	
Frequency Range	1KHz to 300MHz	
Frequency resolution	<0.1Hz	
Frequency accuracy	0.015% of value	

3.2 Generation/Output Timing

Specification	Value	Comments
Maximum data rate per pin	300Mbps	
Maximum data pin toggle rate	150Mhz	
Data pin to pin skew	Maximum : ±500ps	
Output self-tune delay	NA	

3.3 Acquisition/Input Timing

Specification	Value	Comments
Maximum data rate per pin	300Mbps	
Maximum data pin toggle rate	150Mhz	
Data position mode	Delay from sample clock rising edge	
Input data delay frequency	All supported frequencies	
Input delay adjustment	±25 Sample clock cycles expressed as a time in seconds.	
Input data delay resolution	11ps for (ons to 4ns delay) Half clock cycle for other delay range.	

Section 4: Waveform Specifications

Specification	Value		Comments
On-board memory size (generation)	16 Mbit/pin		
On-board memory size (acquisition)	16 Mbit/pin		History RAM
Generation mode	Clock mode		Generate continuous clock outputs
	Vector mode		Generate a sequence of waveforms. Use vector file (*.vec) to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to output triggers.
Number of vector set per DM482e	32		
Number of timing set per DM482e	32		
Maximum data rate	Bidirectional	Dedicated Direction (Input-only/output only)	This applies to all pins
	200Mbps	300Mbps	

Section 5: Triggers

5.1 Trigger Inputs

Specification	Value	Comments
Sources	PXI trigger lines	PXI_TRIG[0:7] PXI_STAR PXI_LBL6 PXI_LBR6 PXIE_DSTARA PXIE_DSTARB
	Software trigger	
	External trigger 0-1	Can be used to trigger vector engine to start driving vector
Polarity	High, Low, Rising, Falling	Configurable
Pulse Width	>=200ns	

5.2 Trigger Outputs

Specification	Value	Comments
Sources	PXI trigger lines	PXI_TRIG[0:7] PXI_STAR PXI_LBL6 PXI_LBR6
	External trigger 0-1	External trigger 0-1 (t0, t1) can be used in vector mode. When running in dual-site mode, trigger 0 is for site 0 whereas trigger 1 is for site 1.
Polarity	Active High	
Pulse Width	1us to 10ms	Configurable

Section 6: MIPI RFFE

Specification	Value		Comments
Number of MIPI RFFE Controllers	4		2 MIPI RFFE controllers available for each pin group
Full-Speed Clock Frequency	Minimum	32kHz	
	Maximum	26MHz	

Section 7: SPI

Specification	Value		Comments
Number of SPI Controllers	2		1 SPI controllers available for each pin group
Bit-width for each Byte	Minimum	1	
	Maximum	24	
Clock Divider	Minimum	0	SPI Clock Frequency = 125MHz/((Clock Divider+2)*2)
	Maximum	4095	
Byte Length	Minimum	1	
	Maximum	256	
Delay after Each Byte	Minimum	0	
	Maximum	40us	

Section 8: I2C

Specification	Value		Comments
Number of I2C Controllers	2		1 I2C controllers available for each pin group
Clock Frequency	Minimum	600Hz	
	Maximum	52kHz	
Command Count	Minimum	1	
	Maximum	256	
Timeout	Minimum	0.01s	
	Maximum	5s	

Section 9: Others

1. Output

   Front Panel Connectors: 68 position VHDCI receptacle

2. Dimension: 3U 2-slot space

Section 10: Revision History

1.0	DEC 2012	INITIAL RELEASE
1.1	JUN 2013	CORRECTED PIN ELECTRONICS DRIVER CURRENT SPECS
1.2	JUN 2013	ADDED MIPI SPECIFICATION
1.3	JUL 2013	UPDATED PMU ACCURACY SPECIFICATIONS
1.4	JAN 2014	RENAMED "DRIVE TRISTATE" TO "DRIVE TERMINATION VOLTAGE" RENAMED "DRIVE VOLTAGE HIGH LEVEL (VIH)" TO "COMPARE HIGH LEVEL (VIH)" RENAMED "DRIVE VOLTAGE LOW LEVEL (VIH)" TO "COMPARE LOW LEVEL (VIH)" UPDATED TERMINATION VOLTAGE RESOLUTION REFINED TIMING SPECIFICATIONS
1.5	JUN 2014	UPDATED MAXIMUM ALLOWED DC DRIVE PER PIN SPECS UPDATED VIH, VIL, VOH, VOL, VT ACCURACY SPECS ADDED SPECIFICATIONS FOR HIGH VOLTAGE DRIVERS ADDED SPECIFICATIONS FOR SPI AND I2C CONTROLLERS

Section 11: Contact Us

To obtain service, warranty or technical assistance, please contact Aemulus.

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Product specifications and descriptions in this document are subject to change without prior notice.