

DM280e

Specifications

Table of Contents

TABLE OF CONTENTS	1
SECTION 1: SPECIFICATION CONDITIONS	2
SECTION 2: SPECIFICATIONS	3
SECTION 3: REVISION HISTORY	23
SECTION 4: CONTACT US.....	24

Section 1: Specification Conditions

This document contains the specifications and supplemental information of DM280e. Specifications are the standards against which the DM280e is tested. Upon leaving the factory the DM280e meets these specifications. Supplemental and typical values are non-warranted, apply at 23°C, and are provided solely as useful information.

Section 2: Specifications

Number of MIPI RFFE channels	2
MIPI RFFE terminals	SCLK0 and SDATA0 SCLK1 and SDATA1
Logic High of RFFE Channels	VIO
Impedance	75 Ohms
Communication Interface	PCIe
Half-speed read Access	Yes
Configurable Arbitrary Clock	32 KHz to 26 MHz
Configurable VIO Voltage Supply	1.5 - 3.8 volts \pm 10%
Slave Emulator	Yes

Table 1: Specifications of DM280e

Note:

1. Voltage levels are common to all channels.
2. The frequency is common to all channels.
3. The default delay for the DUT (Device-Under-Test) to send data during retrieve operation is double of the configured frequency.

Supplemental Specifications

Bus Active Data Transmission Timing Specification

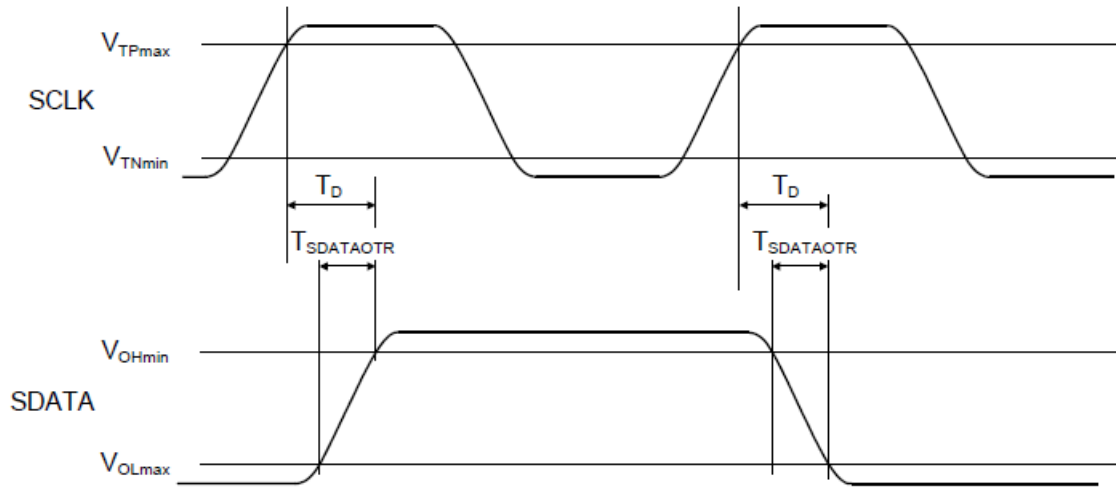


Figure 2: Bus Active Data Transmission Timing Specification

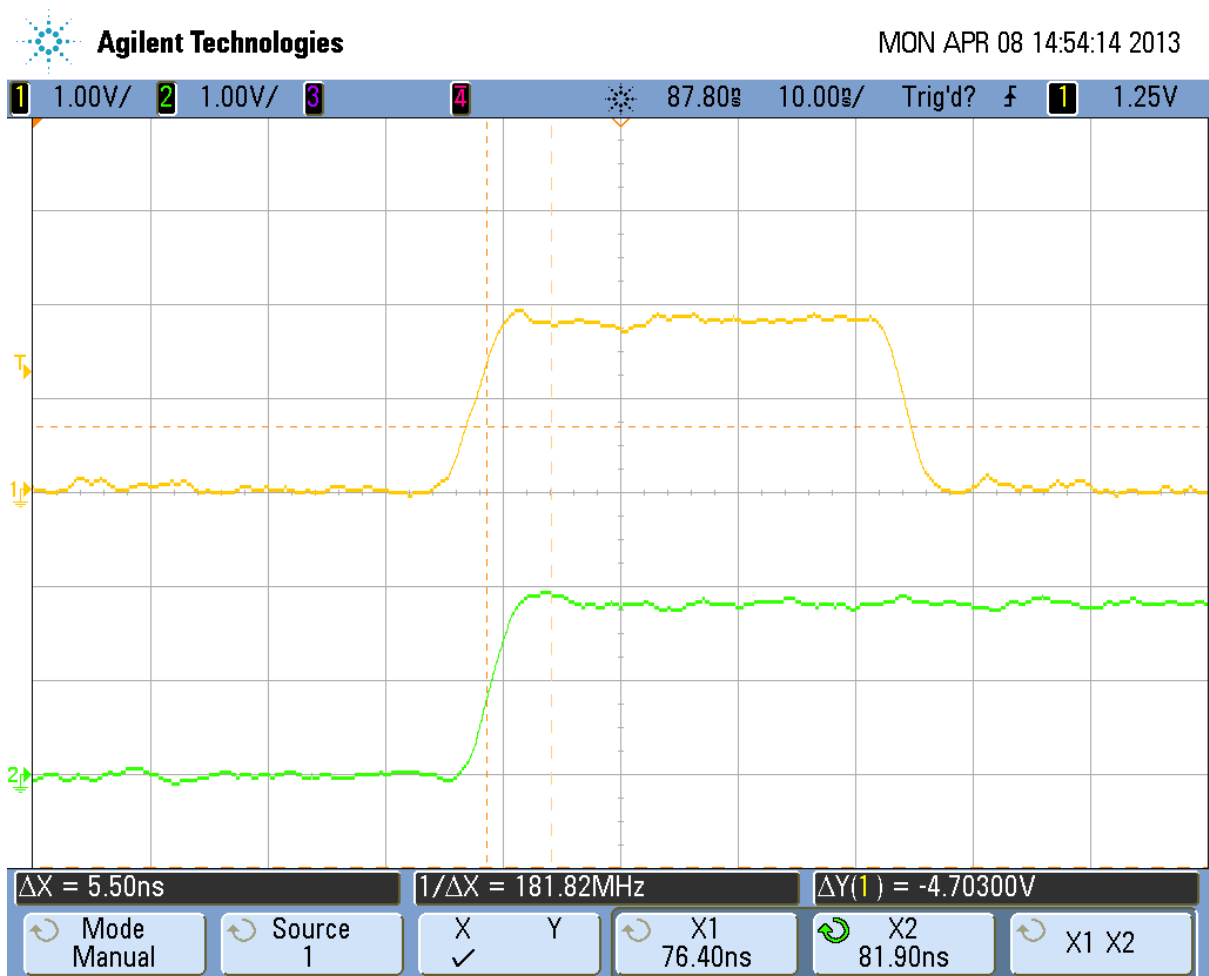
Symbol	Description	Half Speed Device		Full Speed Device		Units
		Min	Max	Min	Max	
T_D	Time for Data Output Valid from SCLK rising edge	0	22	0	10.25	ns
$T_{SDATAOTR}$	SDATA Output Transition (Rise/Fall) Time (Master only)	N/A	N/A	3.5	6.5	ns
	SDATA Output Transition (Rise/Fall) Time (Slave only)	2.1	10	2.1	6.5	ns

Table 2: SDATA Output Timing Characteristics

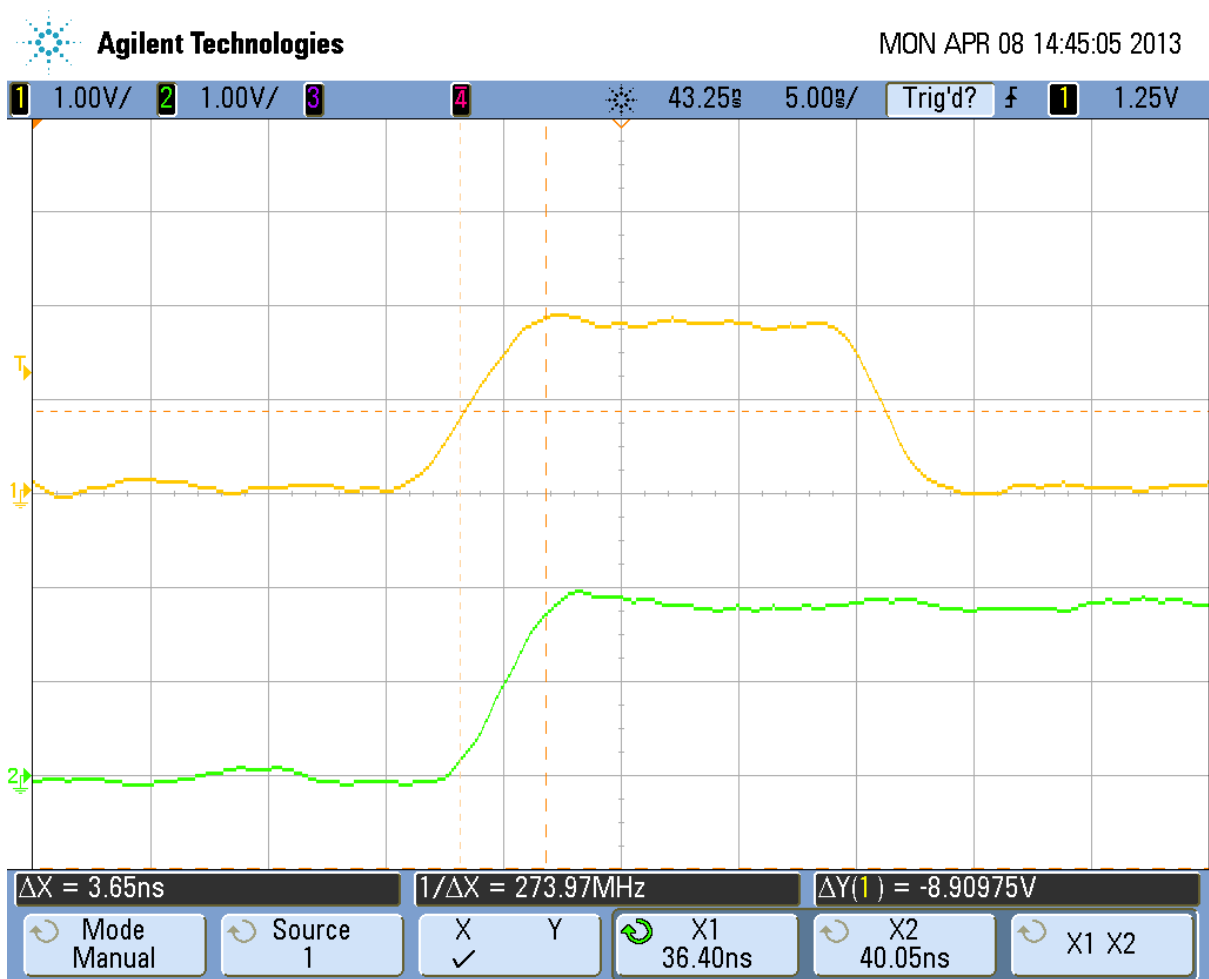
1. In full-speed operation, DM280e takes 2.65ns of T_D , which falls between the range of 0 and 10.25ns.



2. In half-speed operation, DM280e takes 5.50ns of T_D , which falls between 0 and 22ns.



3. Full-speed operation, T_{SDATAOTR} is 3.65ns, which falls between 3.5 and 6.5ns.



Clock Input Timing Requirements

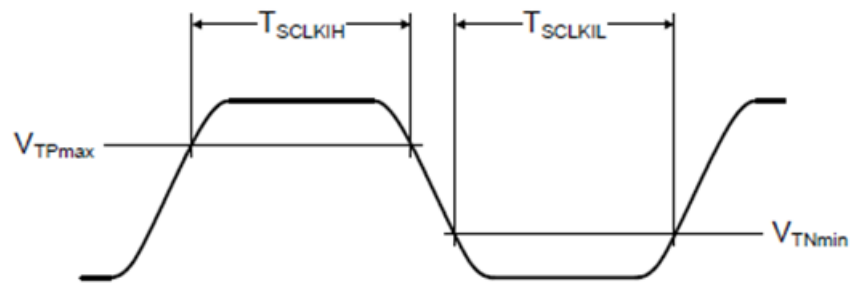
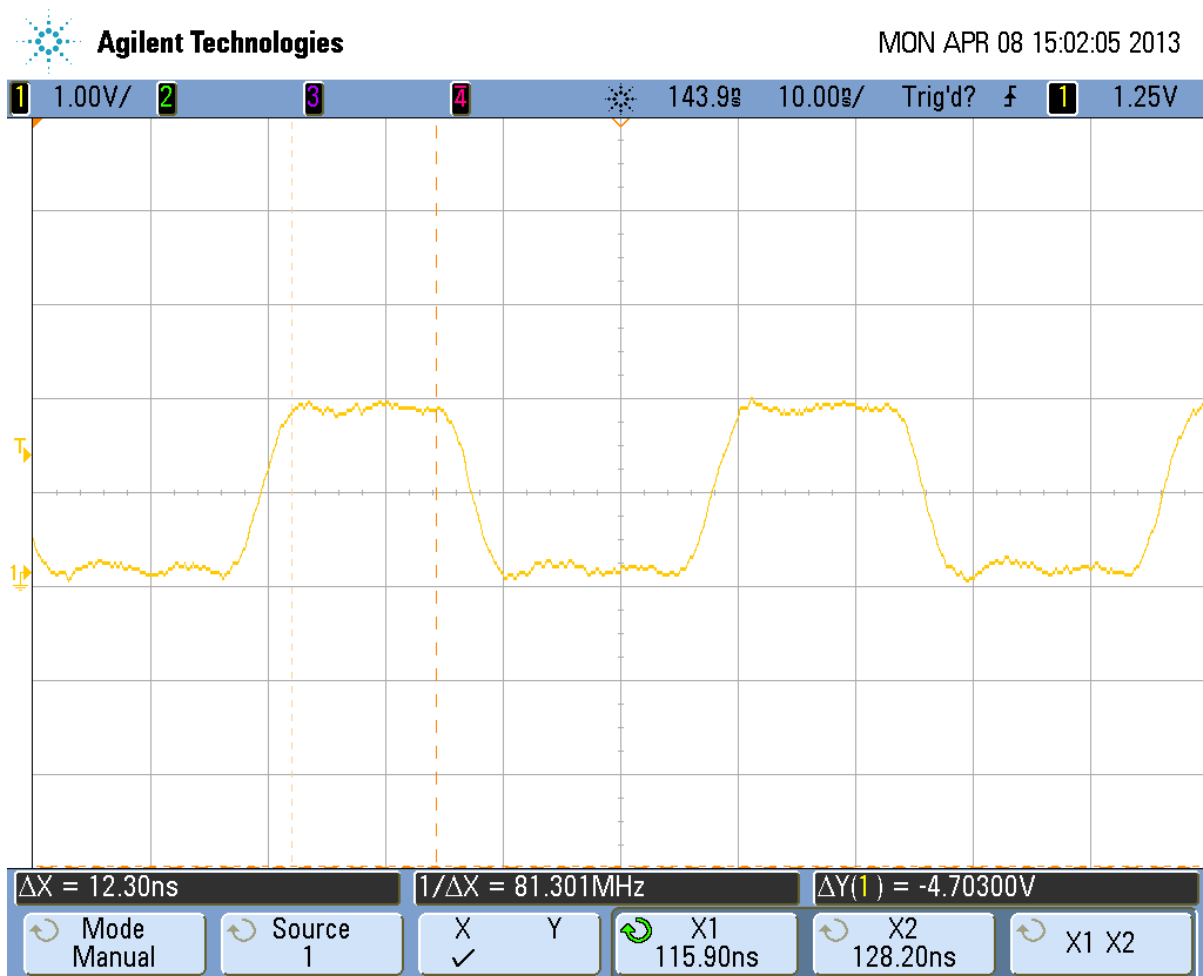


Figure 3: Received Signal Clock Constraint

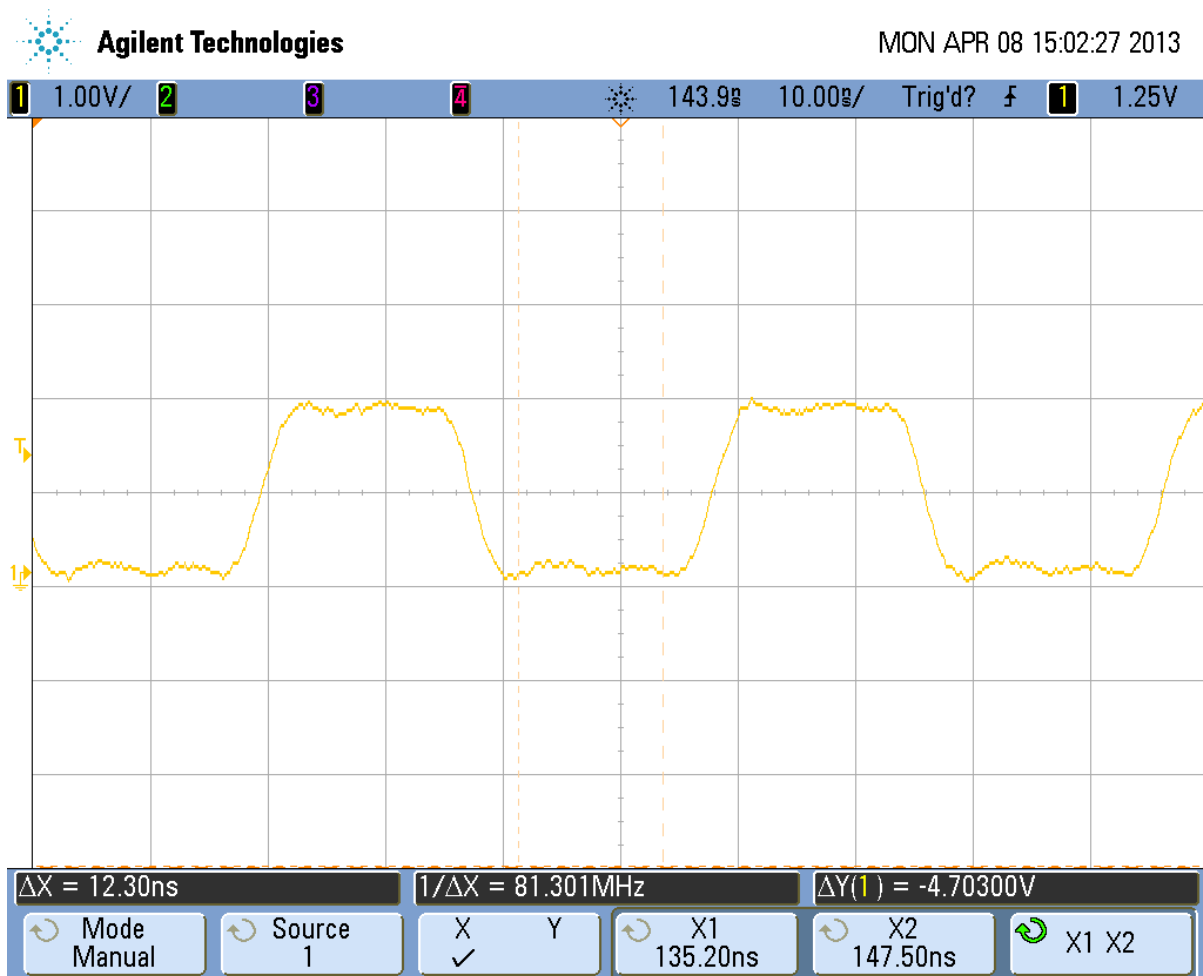
Symbol	Description	Half Speed Device		Full Speed Device		Units
		Min	Max	Min	Max	
T_{SCLKIH}	SCLK Input High Time	24		11.25		ns
T_{SCLKIL}	SCLK Input Low Time	24		11.25		ns

Table 3: Clock Input Timing Requirements

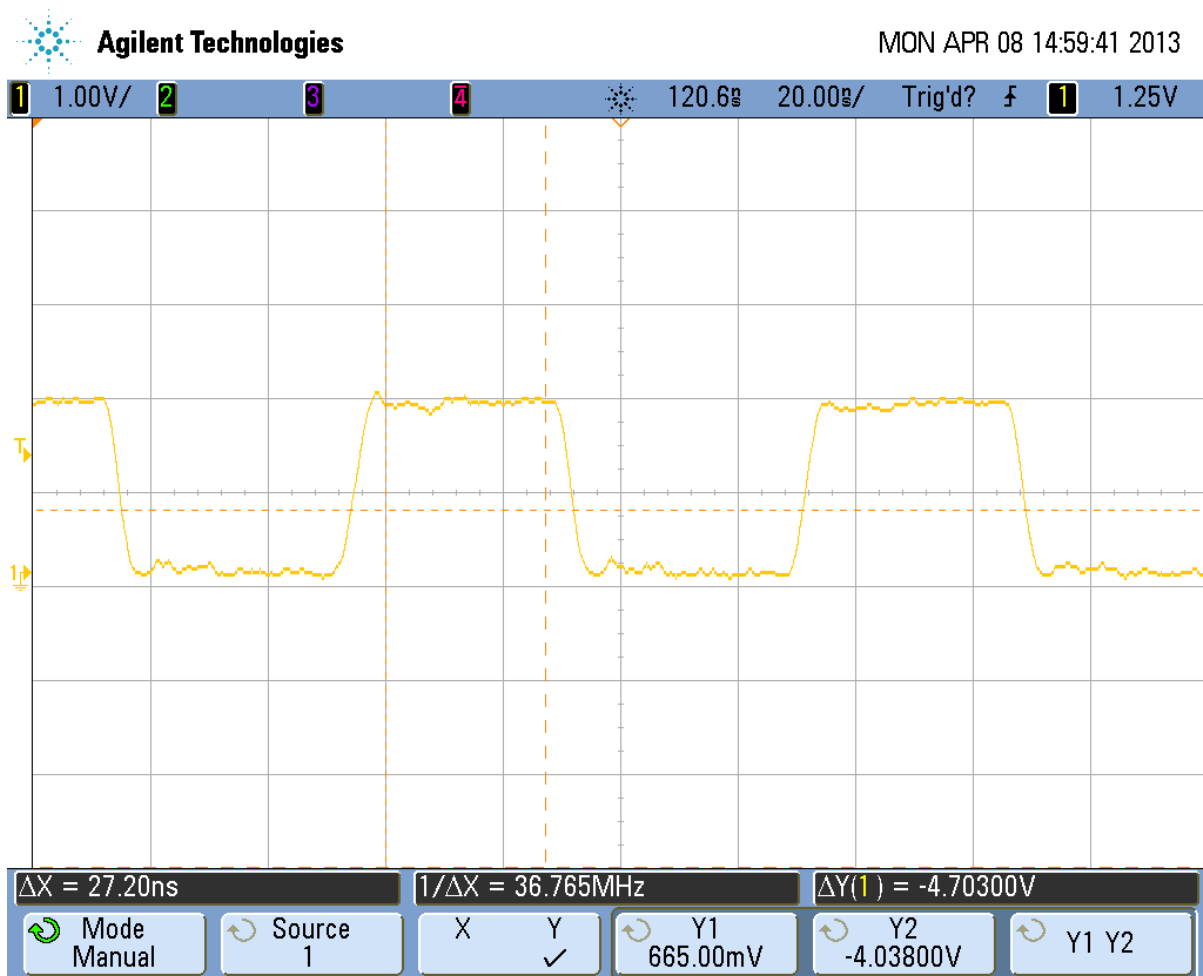
1. In full-speed operation, SCLK input high time is 12.30ns which is higher than 11.25ns.



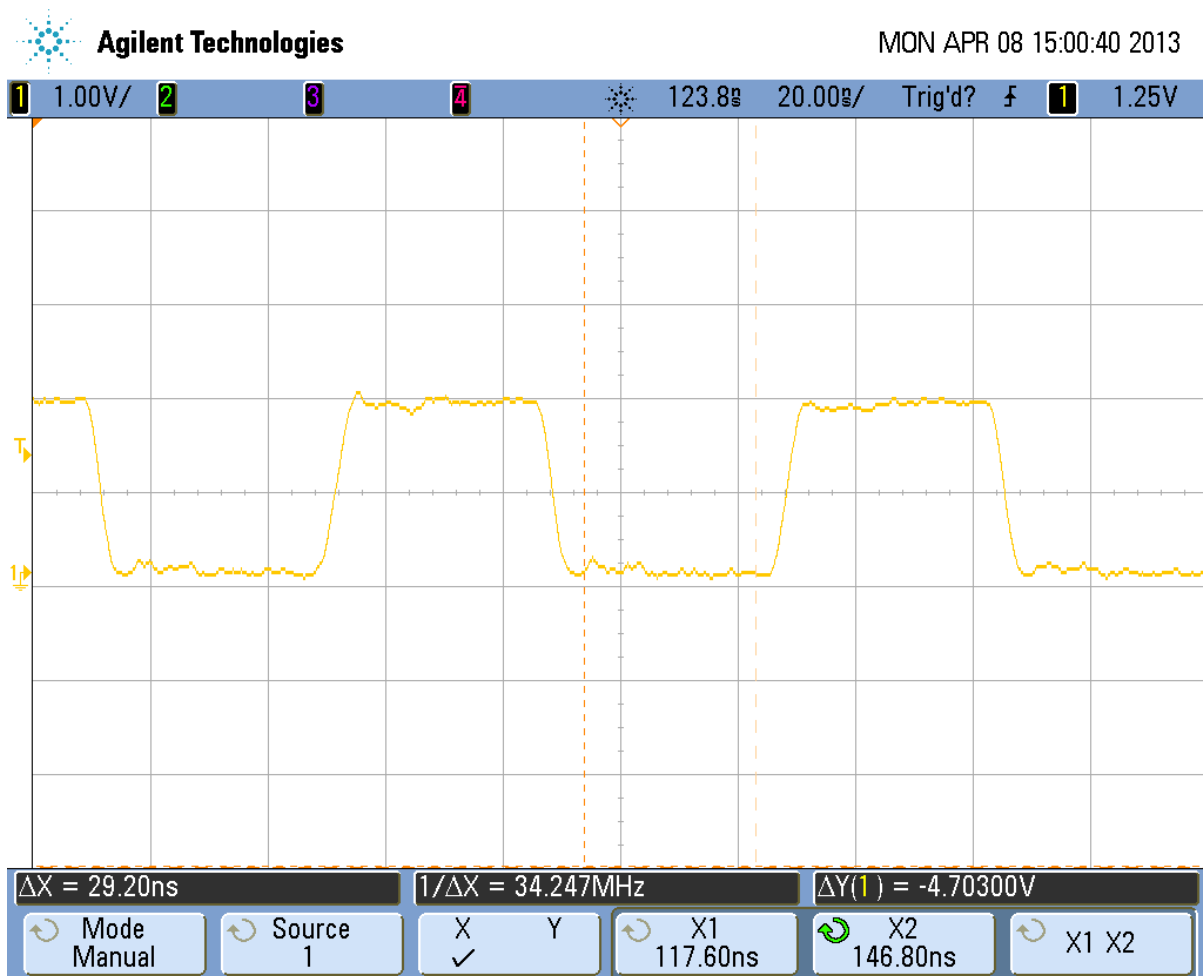
2. In full speed operation, SCLK input low time is 12.30ns, which is higher than 11.25ns.



3. During half speed operation, SCLK input high time is 27.20ns, which is higher than 24ns.



4. During half speed operation, SCLK input low time is 29.30ns, which is higher than 24ns.



Data Setup and Hold Time Requirements

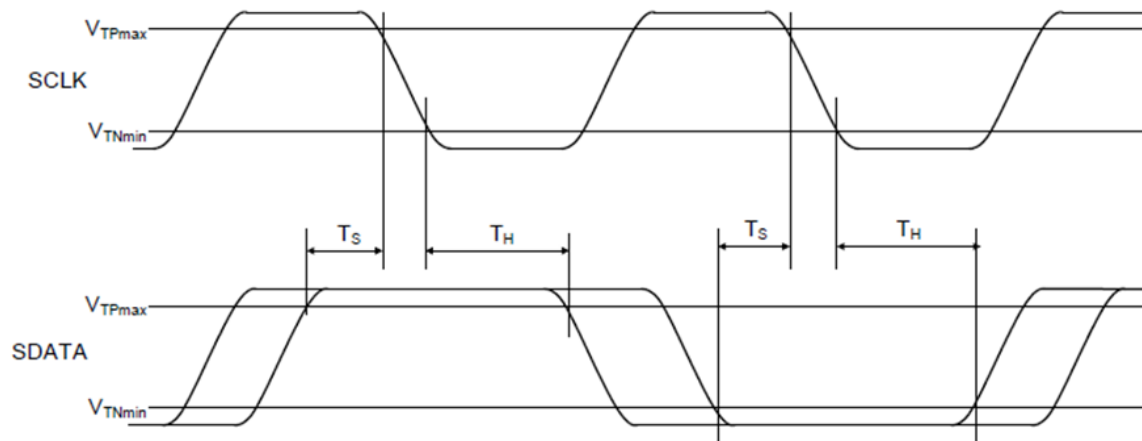


Figure 4: Bus Active Data Receiver Timing Requirements

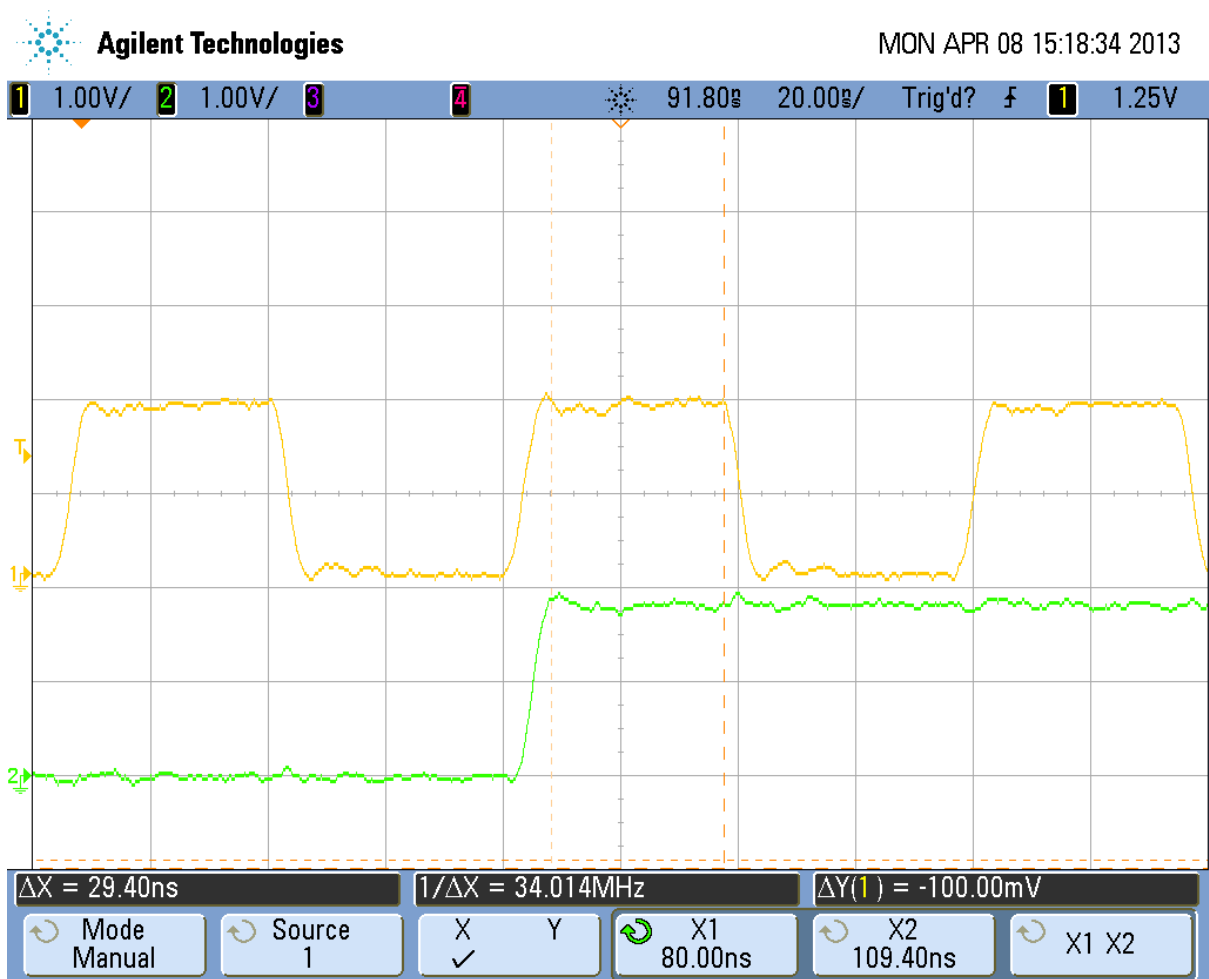
Symbol	Description	Half Speed Device		Full Speed Device		Units
		Min	Max	Min	Max	
T_S	Data setup time	2		1		ns
T_H	Data hold time	5		5		ns

Table 4: Data Setup and Hold Timing

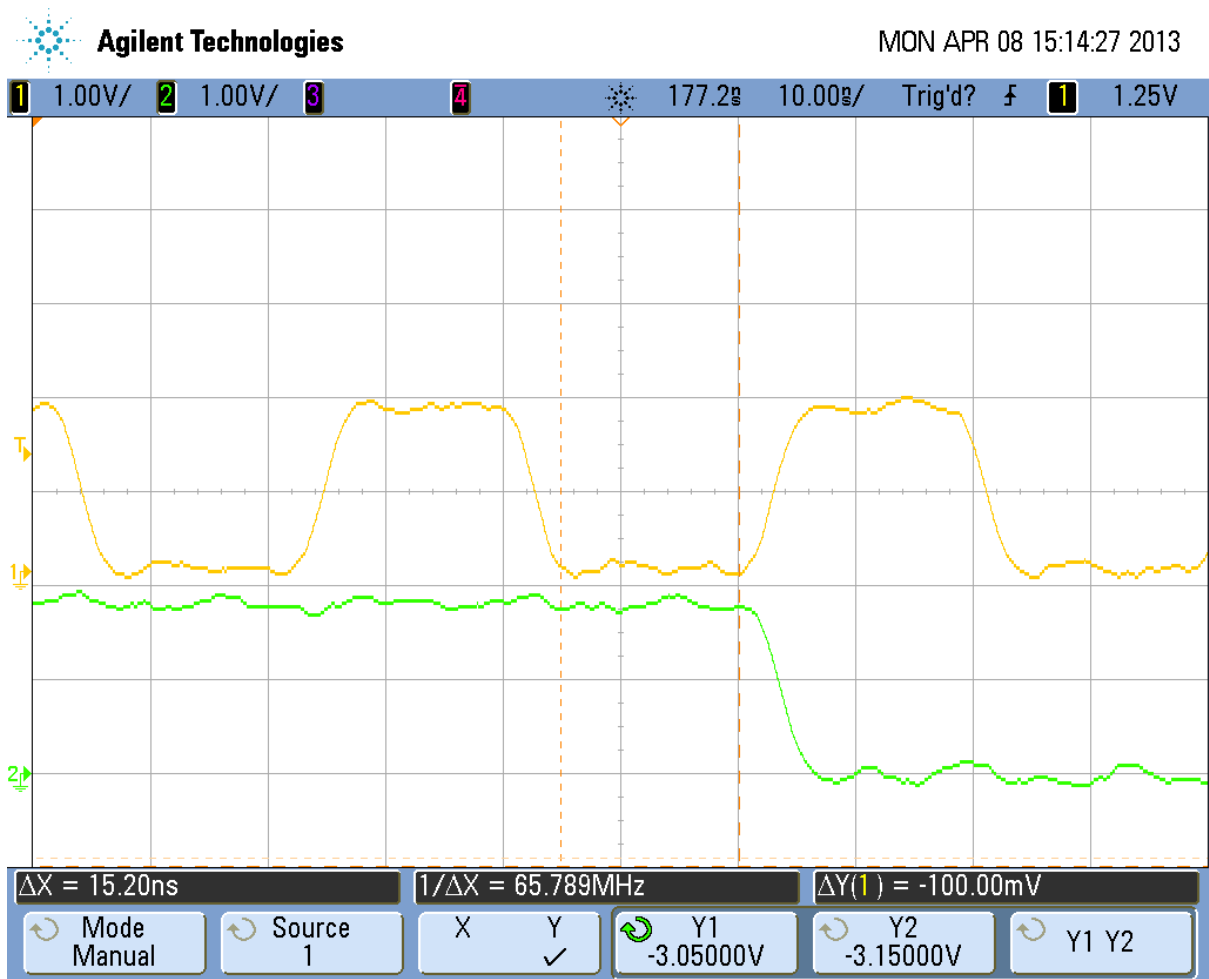
1. Full speed condition, T_S is 12.50ns, which is higher than 1ns.



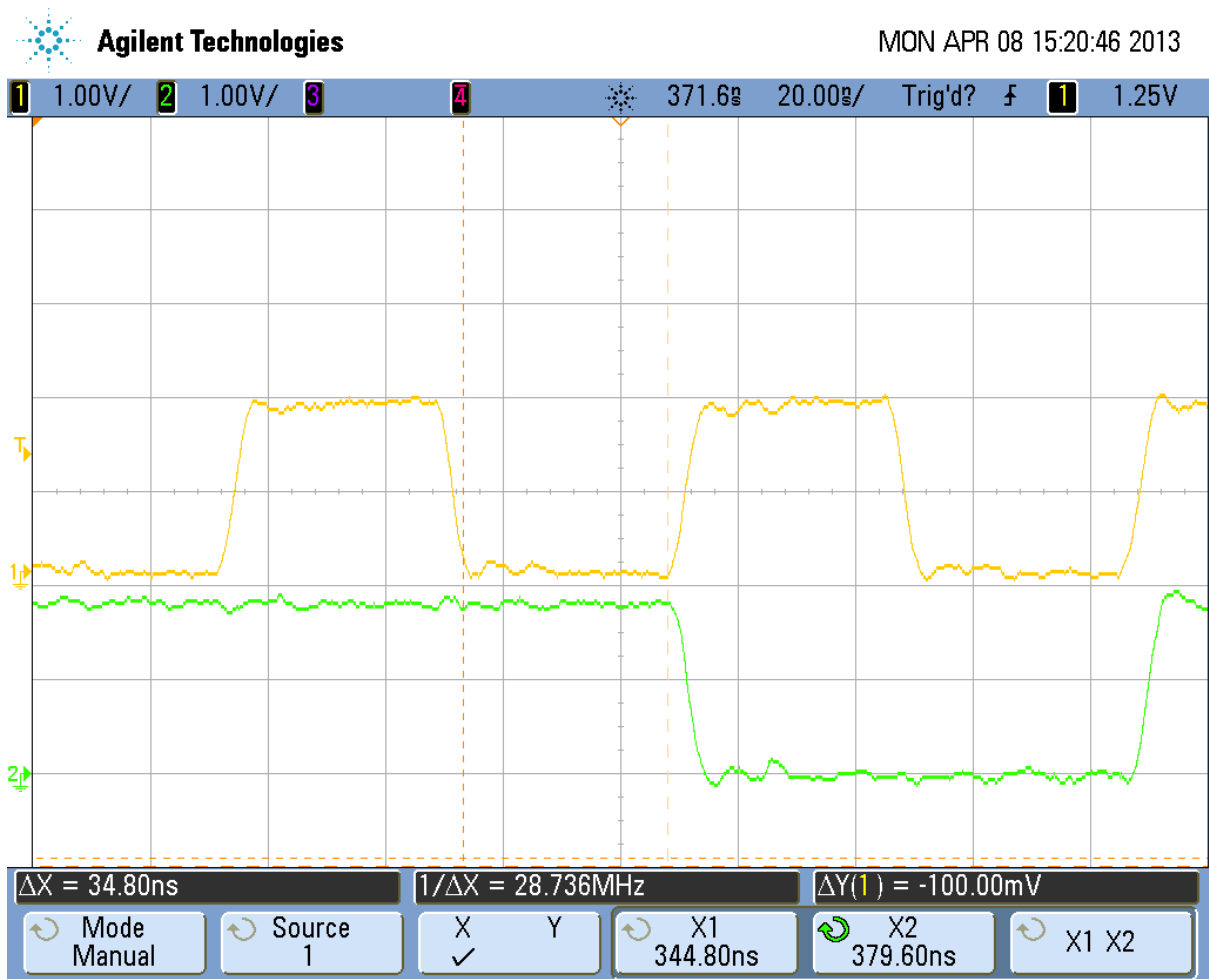
2. Half-speed condition, T_S is 29.40ns, which is higher than 2ns.



3. Full-speed condition, T_H is 15.20ns, which is higher than 5ns.



4. Half speed condition, T_H is 34.80ns, which is higher than 5ns.



Clock Driver Output Waveform Constraints

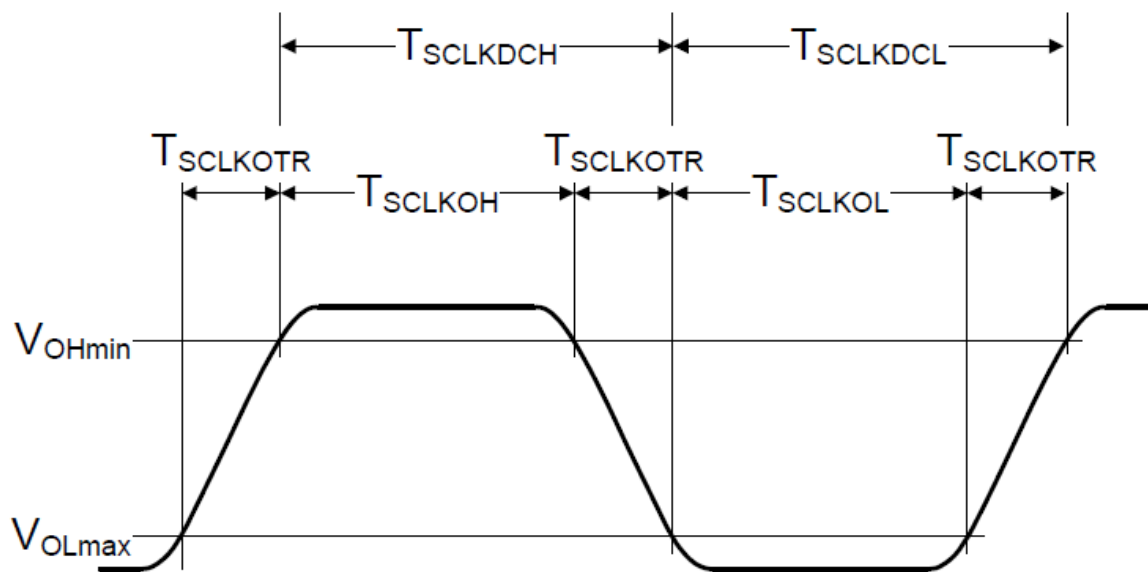


Figure 5: Clock Driver Waveform Constraints

Symbol	Description	Half Speed Device		Full Speed Device		Units
		Min	Max	Min	Max	
T_{SCLKOH}	Clock Output High Time	24		11.25		ns
T_{SCLKOL}	Clock Output Low Time	24		11.25		ns
$T_{SCLKOTR}$	Clock Output Transition (Rise/Fall) Time ¹	3.5	10	3.5	6.5	ns
$T_{SCLKDCH}$	Clock Output Duty Cycle, High Time ^{2,3}	45	55	45	55	%
$T_{SCLKDCL}$	Clock Output Duty Cycle, Low Time ^{2,3}	45	55	45	55	%

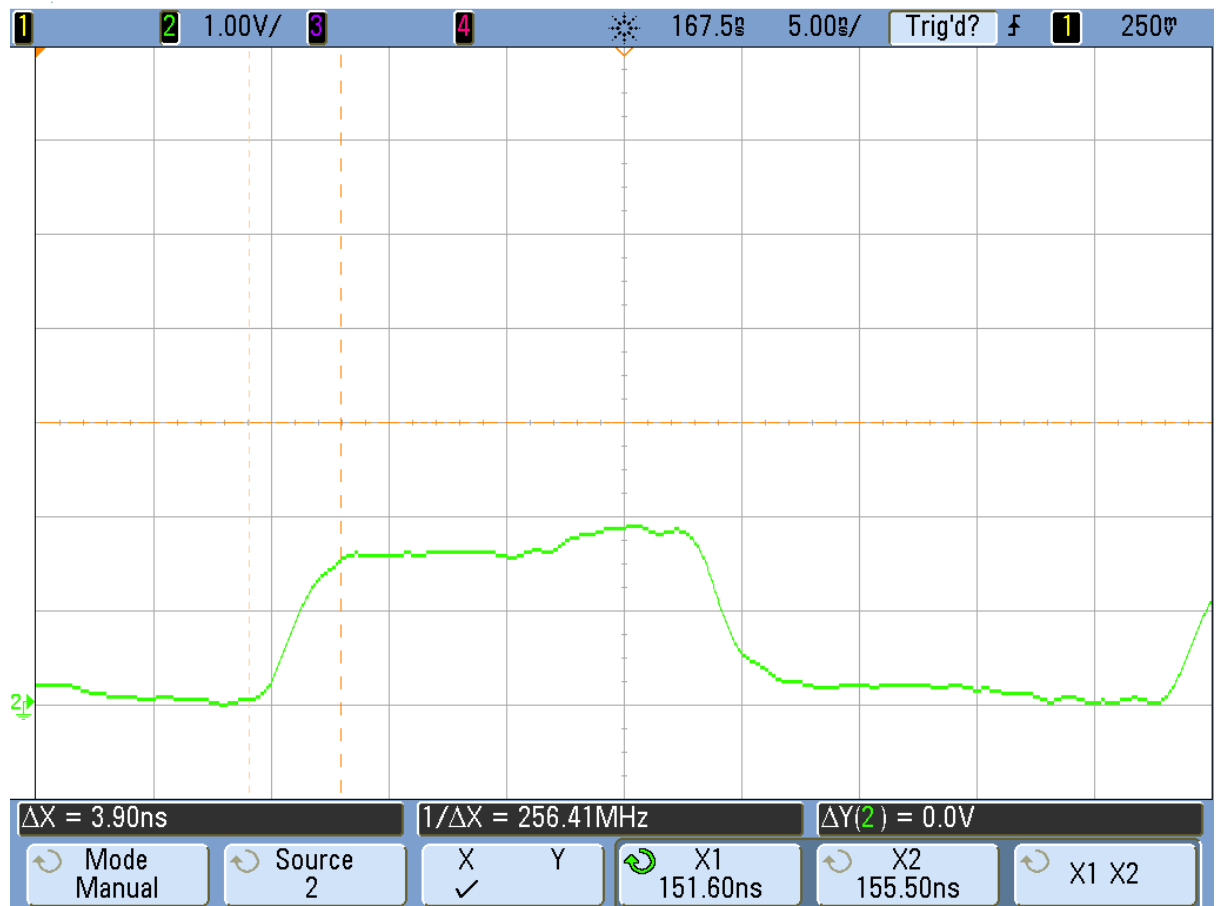
Table 5: Output Timing Characteristics

1. Rise time for half speed device is 3.90ns, which is between 3.50ns and 10.00ns.

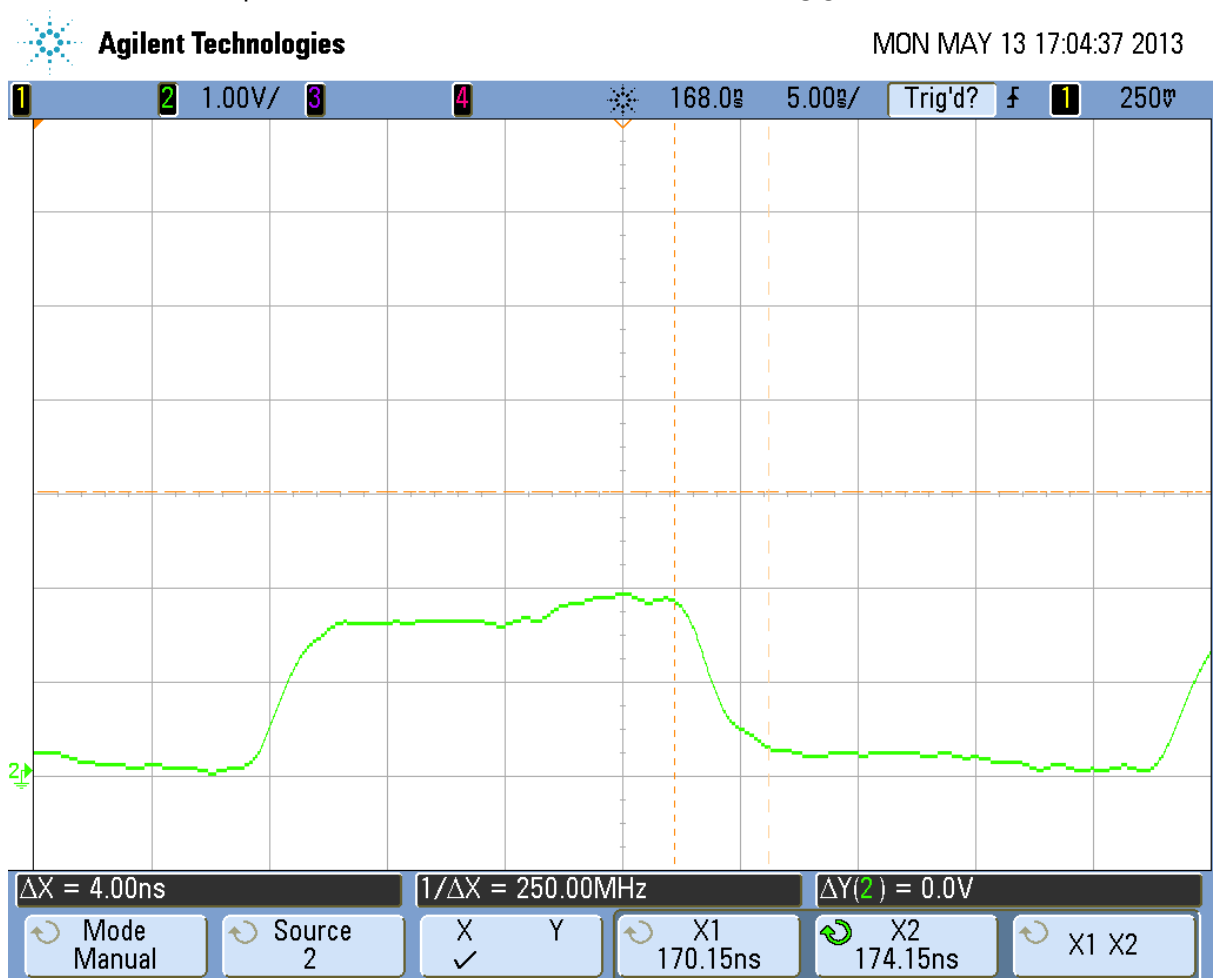


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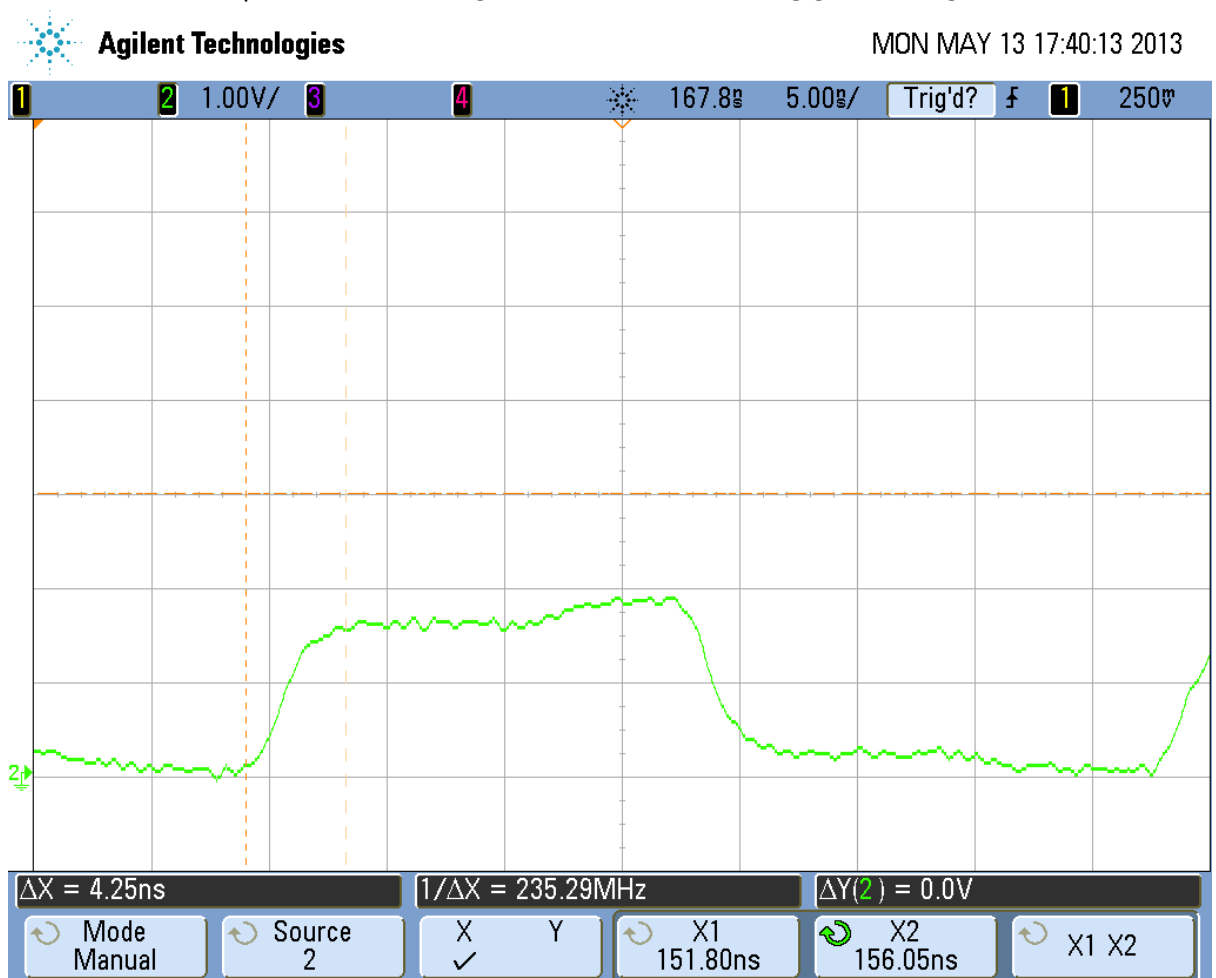
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2. Fall time for half speed device is 4.00ns, which is in between 3.50ns and 10.00ns.



3. Rise time for full speed device is 4.25ns which is in between 3.5ns and 6.5ns.



4. Fall time for full speed device is 4.15ns, which is in between 3.5ns and 6.5ns.



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Section 3: Revision History

1.0	APR 2013	INITIAL RELEASE
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Section 4: Contact Us

To obtain service, warranty or technical assistance, please contact Aemulus.



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Product specifications and descriptions in this document are subject to change without prior notice.