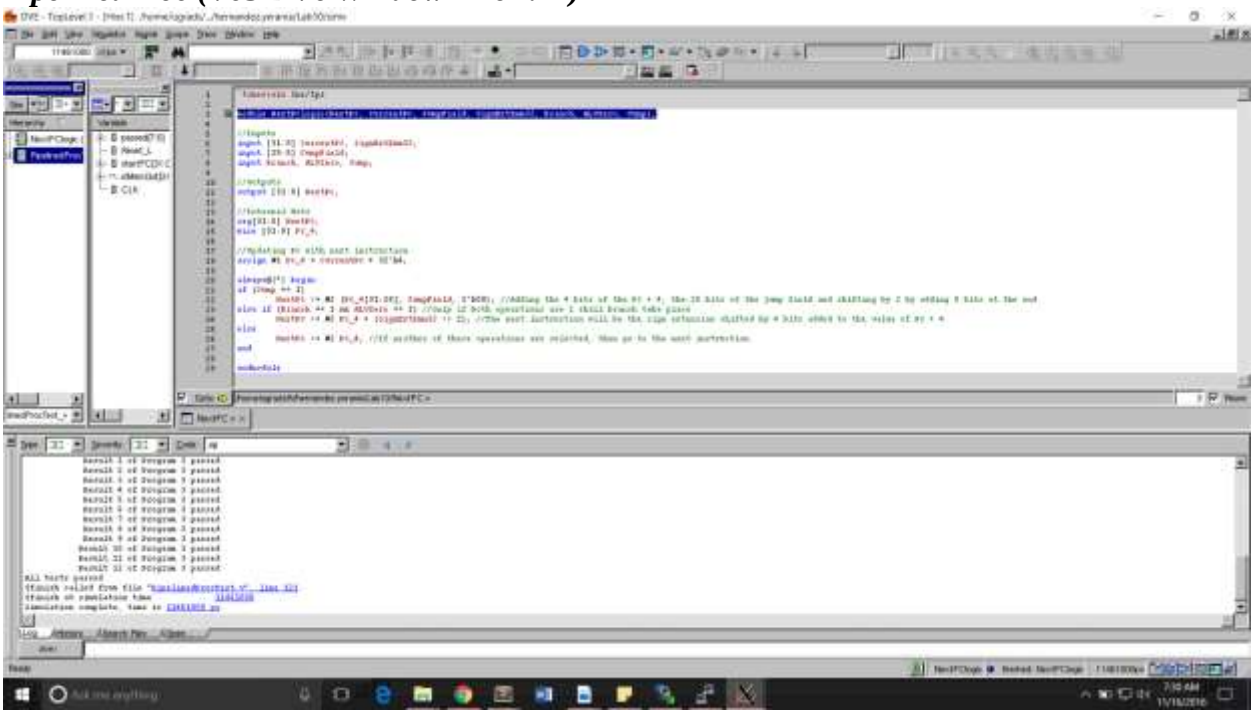
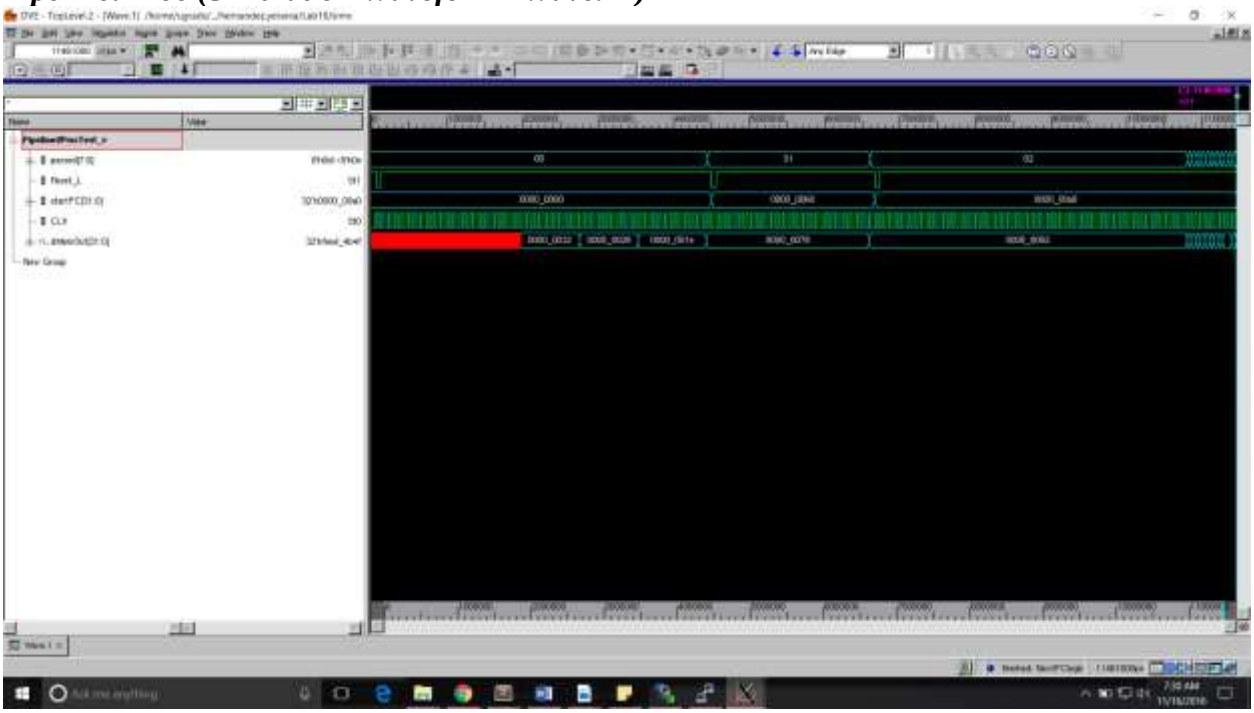
Lab 10

PipelinedProc (VcS DVe Window “Heir.1”)



PipelinedProc (Simulation Waveform “Wave.1”)



PipelinedProc Explanation

The PipelinedProc works properly based on the test bench. Analyzing the simulation, there are three different programs being used to test the different operations that need to be taken into account for this pipeline to function. The PipelinedProc allows us to compile and synthesize all the components of a processor together, with PipelineCycle using the same values as the SingleCycle. In addition, however, we have a hazard file that allows us to handle the different hazards possible with the different operations, such as branching and jumping. These are divided in stages, meaning that when an operation in either one of the three programs is tested, and it causes a need for this operation in the next pipeline cycle, then the operation is being checked with the past results in order to see if it will be needed and what course of action will be needed. It is simply checking for dependencies and taking care of them through different stage scenarios. As a result, the PipelinedProc simulation shows the results of each of the components of the processor and the final result, including the different states of hazards that are necessary during operations.