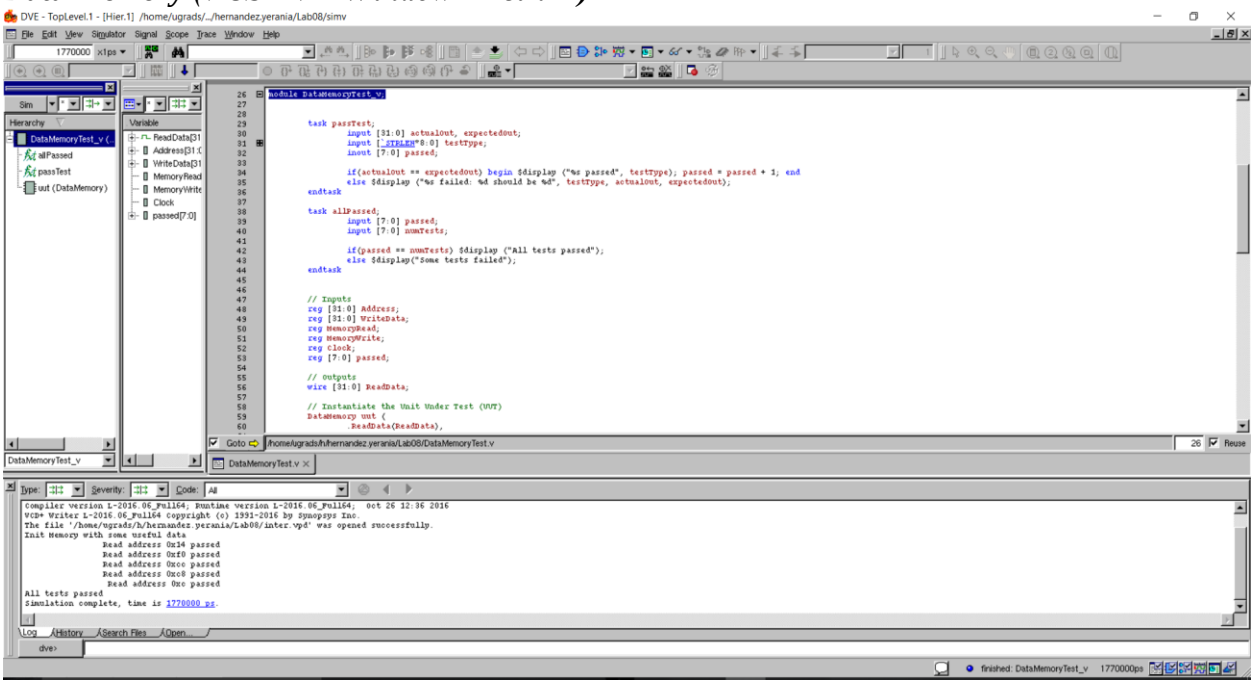
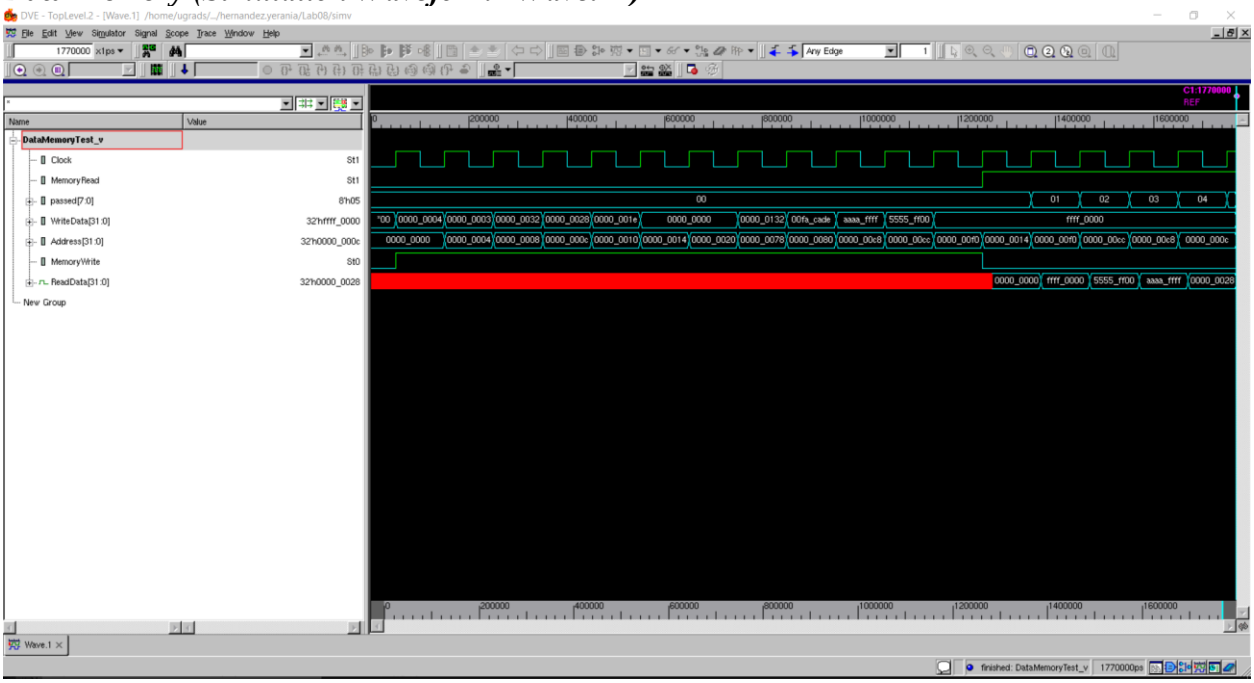
Lab 8

Data Memory (VCS DVE Window "Heir.1")



Data Memory (Simulation Waveform "Wave.1")

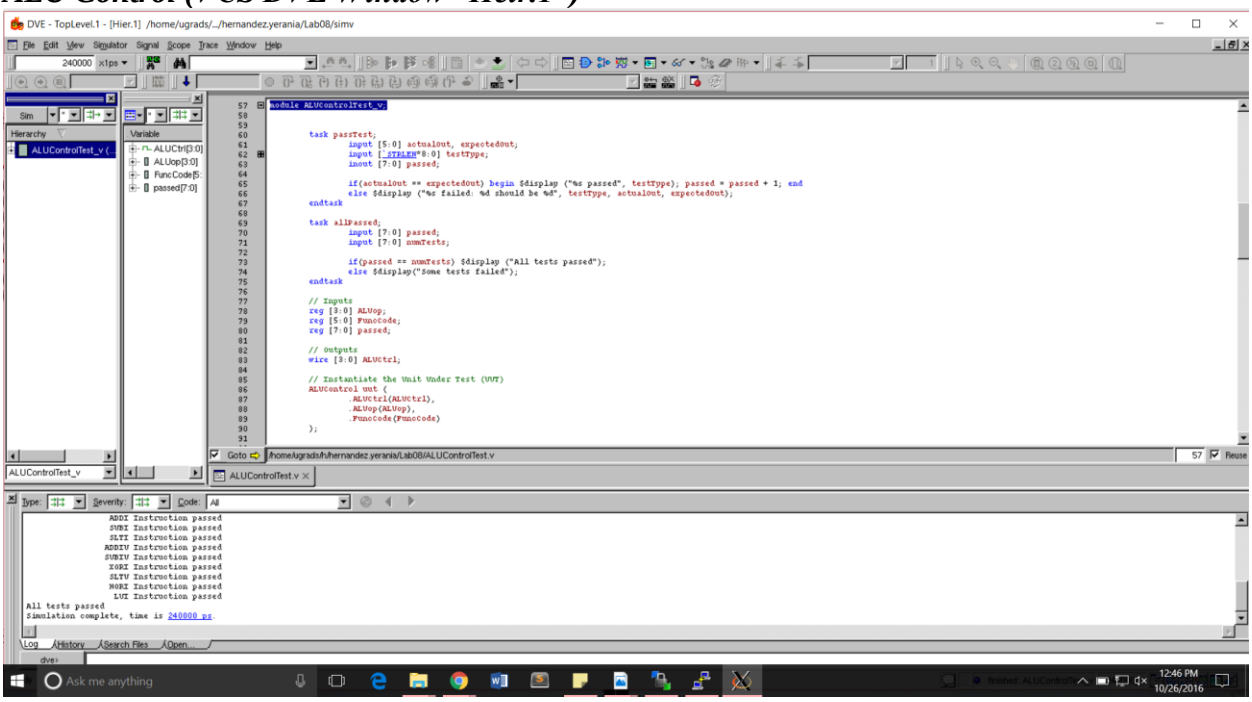


Data Memory Explanation

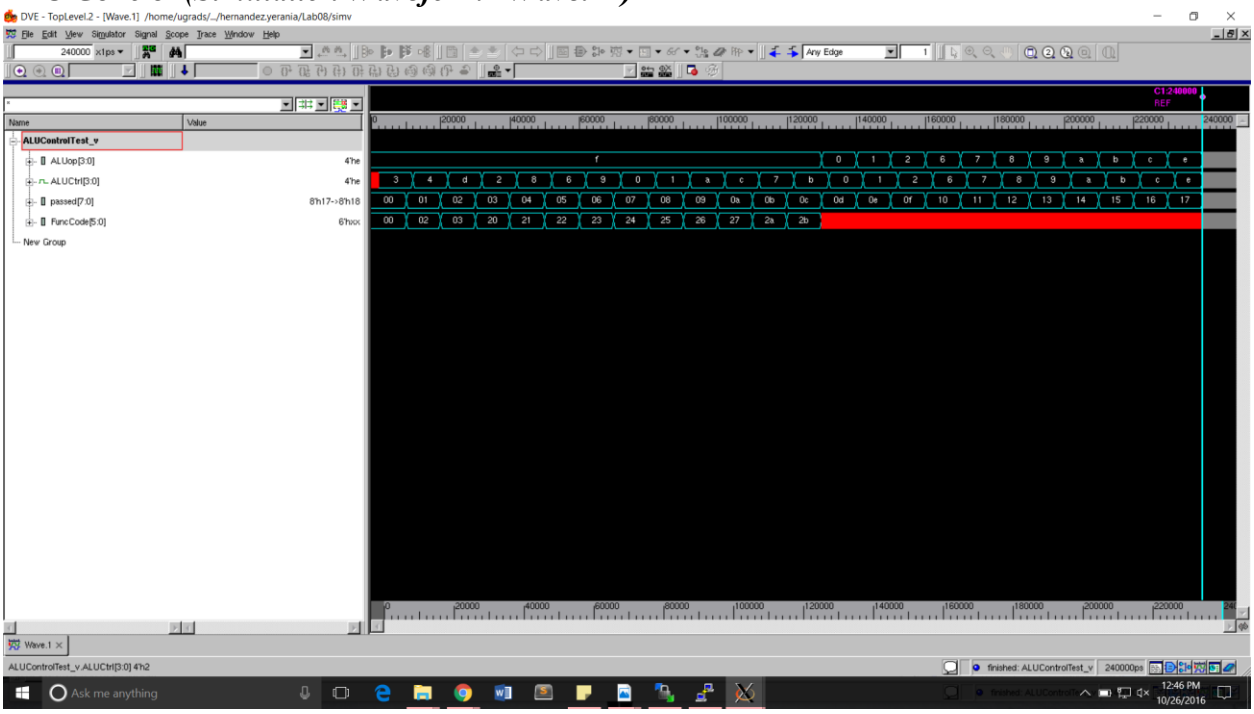
Data memory works properly based on the test bench. Analyzing the simulation, the first part consists of the program writing into memory various values in specific addresses, which is why there is a red bar sine this is the reading input. The last part of the simulation (after the red bar),

the program is reading in the specific values based on the memory location indicated, such as when it reads in 5555_ff00 from the address 0000_00cc, and the same procedure goes for the rest of values.

ALU Control (VCS DVE Window “Heir.1”)



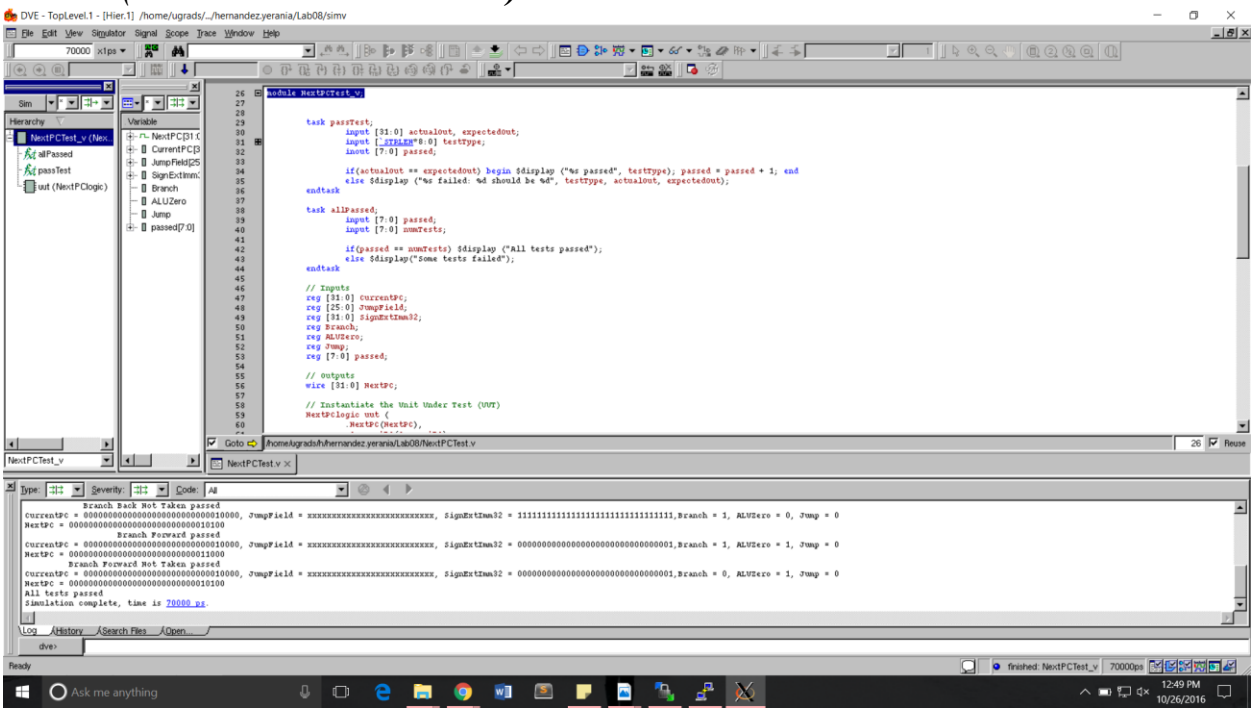
ALU Control (Simulation Waveform “Wave.1”)



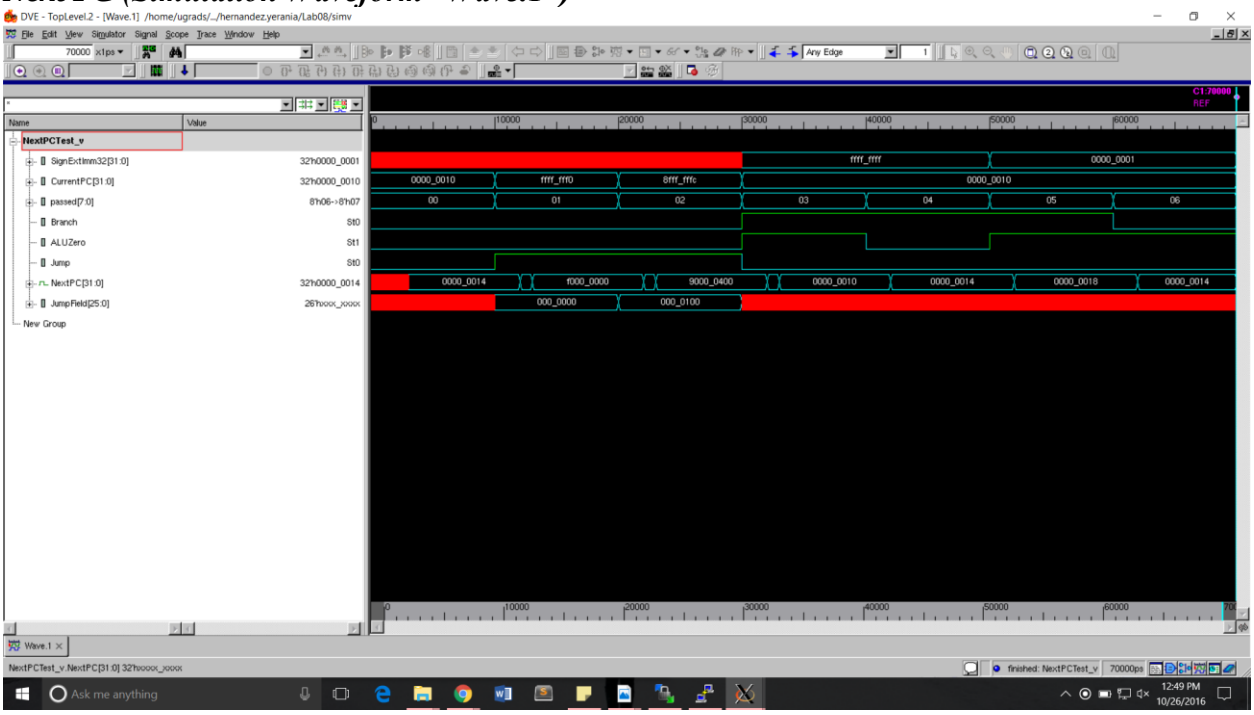
ALU Control Explanation

ALU control works properly based on the test bench and the modified test bench based on prelab specifications. Analyzing the simulation, the part in which the FuncCode has a red bar means that the FuncCode does not matter and therefore the values of the ALUCtrl are the same as those of the ALUop. The rest of the simulation is an R-type which is why the ALUop is f (1111 in binary) and the value of the ALUCtrl depends on the FuncCode. As shown, each of the indicated operations is assigned to the proper ALUCtrl.

Next PC (VCS DVE Window "Heir.1")



Next PC (Simulation Waveform "Wave.1")



Next PC Explanation

The program Next PC works properly based on the test bench and displays the outputs of the values. Analyzing the simulation, there are two operations that is occurring, jump and branch. When jump is turned on, the value of NextPC will consist of the first 4 bits of the value in CurrentPC, with the values of JumpField, and 2 bits of 0 added in order to implement the shift. When jump is turned off but branch is still not turned on, then NextPC will be the value of the next instruction, which is adding 4 to the CurrentPC. When branch is turned on, but ALUZero is not 1, then no operation of branching should occur and therefore NextPC should only be the CurrentPC plus 4 as usual to get to the next instruction. However, when both values are 1, then the branch operation should be executed by shifting SignExtImm32 by 4 bits and adding the value of the next instruction, which is the CurrentPC plus 4, which is shown through the simulation such as when the value of CurrentPC is 0000_0010 and then branching causes it to be 0000_0018. The same procedure occurs for the rest of the values.