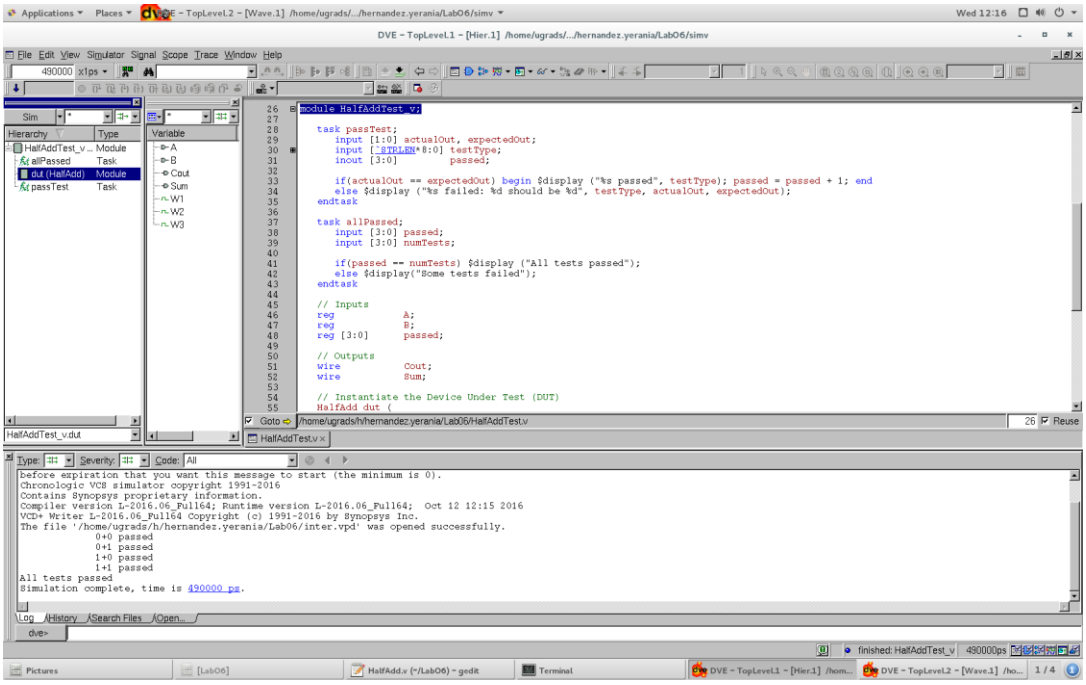
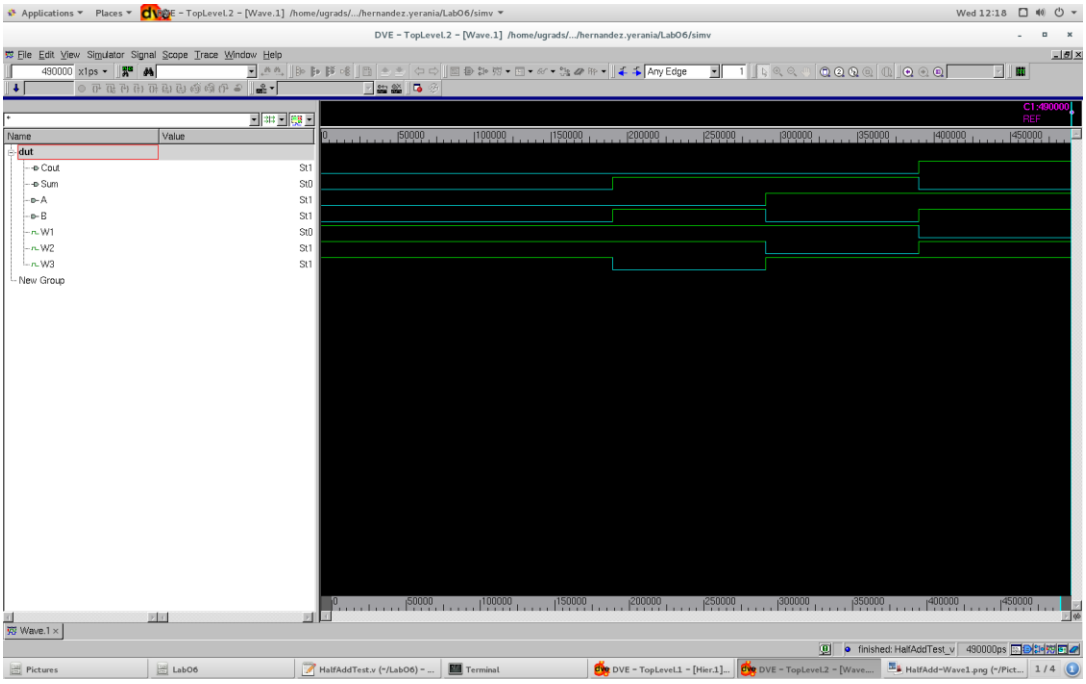
Lab 6

Half Adder (VCS DVE Window "Hier.1")



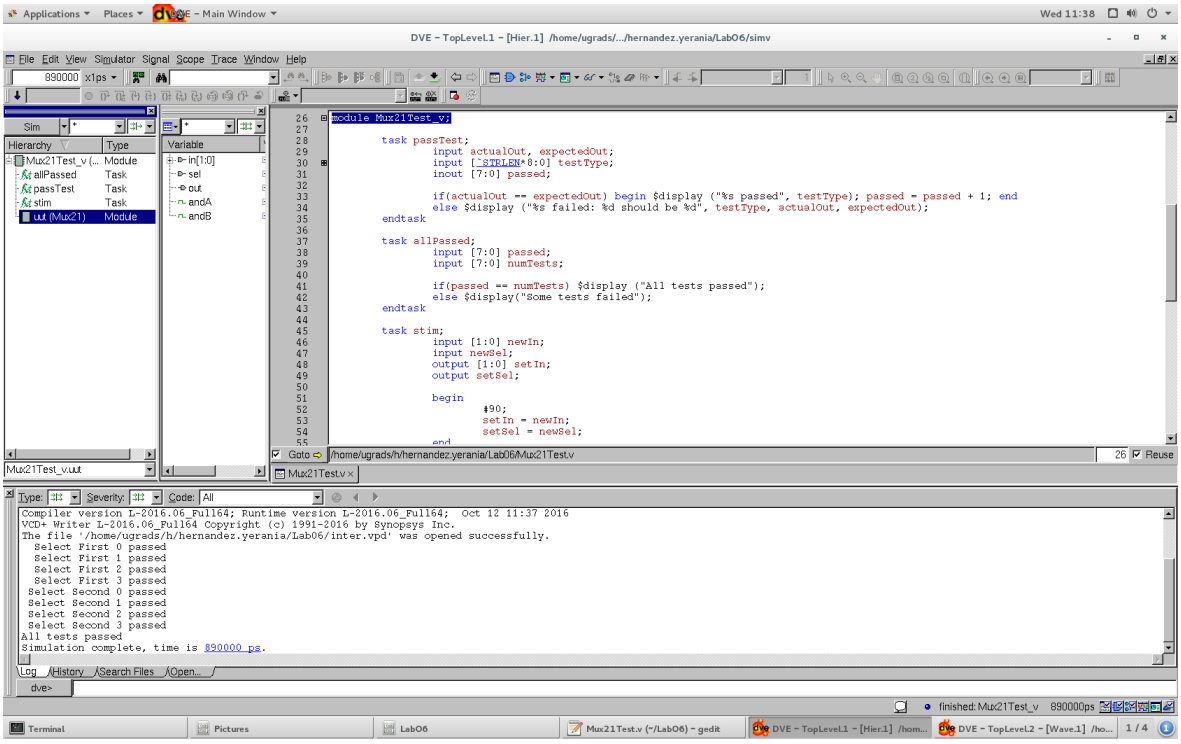
Half Adder (Simulation Waveform "Wave.1")



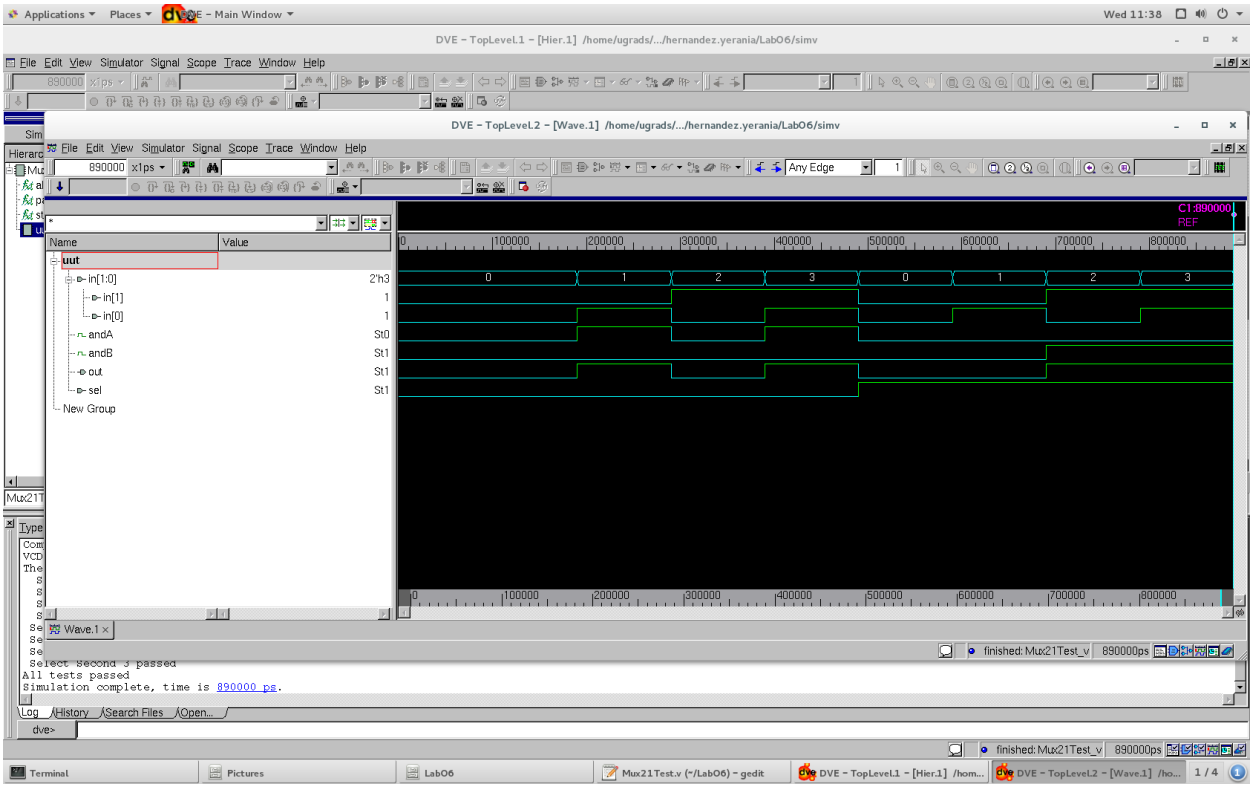
Half-Adder Explanation

According to the test bench, all the cases have passed. Analyzing the simulation based on the truth table, we can verify that the half-adder is functioning properly. When the output of A is 0, and B is 0, the result of sum and cout are both 0, which is shown by a flat line on the simulation. When the output of B is changed to 1, the Sum changes to 1. As soon as the value of A is changed to 1, B being 0, sum continues to stay at 1. However, when both inputs of A and B are 1, the sum changes to the value 0 and cout finally changes to 1. W1, W2, and W3 are all the wires with the results of the intermediate steps in order to reach the final result of sum and carry, which are properly achieved.

2-to-1 MUX (VCS DVE Window "Hier.1")



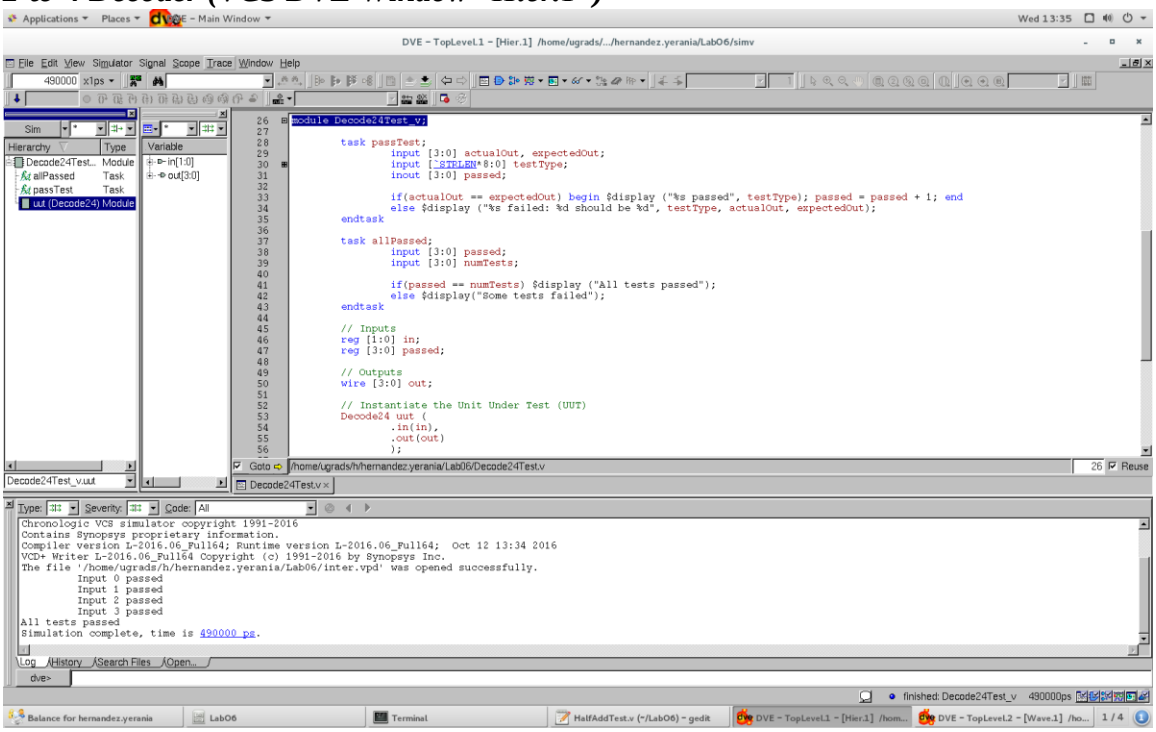
2-to-1 MUX (Simulation Waveform "Wave.1")



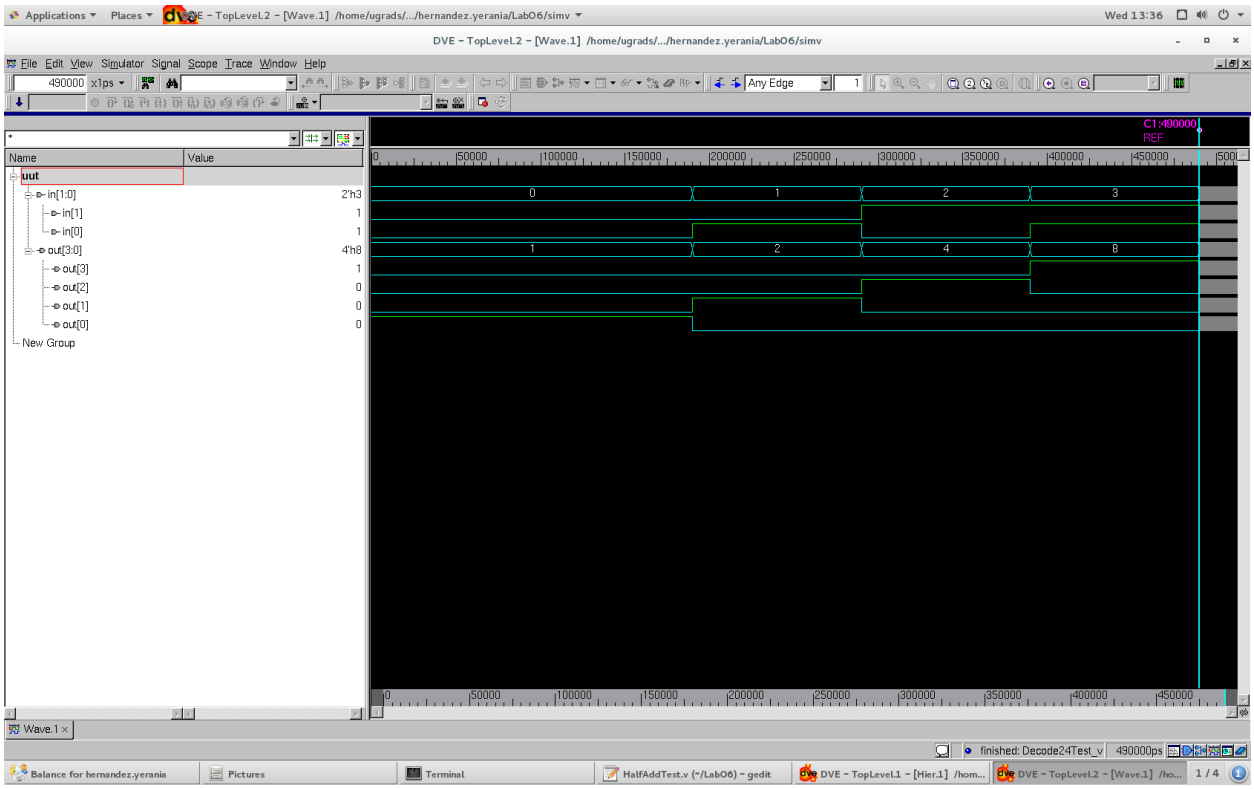
2-to-1 Mux Explanation

According to the test bench, all the cases have passed. Analyzing the simulation based on the truth table, we can verify that the 2-to-1 mux is functioning properly. When sel is 0, there are 4 different combinations that can occur, two of which cause the output to be 1. When the input is both 0, the output is 0, and when in[0] is 0 and in[1] is 0, the output is 0 based on the simulation. When the input of in[0] is 1 though, the output is 1 regardless of in[1]. When sel is 1, there are also 4 different combinations that can occur, two of which cause the output to be 1 as well. As long as in[1] is 0, the output is 0 regardless of the value for in[0] and as long as in[1] is 1 the output is 1 regardless of the value for in[0]. All these combinations match the truth table for circuit, while andA and andB demonstrate the intermediate steps to achieve these results.

2-to-4 Decoder (VCS DVE Window "Hier.1")



2-to-4 Decoder (Simulation Waveform "Wave.1")



2-to-4 Decoder Explanation

According to the test bench, all the cases have passed. Analyzing the simulation based on the truth table, we can verify that the 2-to-4 deocder is functioning properly. When the in[0] and in[1] are both 0, the value of out[0] should be 1 and the other output values should be 0, which is shown in the simulation. When in[0] turns into 1 but in[1] still is 0, the value of out[1] should be 1, while the rest of the values of out hold 0. The value of out[2] is 1 when in[1] is 1 and in[0] is 0, while out[3] is 1 when in[1] and in[0] are both 1. These results from the simulation coincide with the truth table of the decoder.