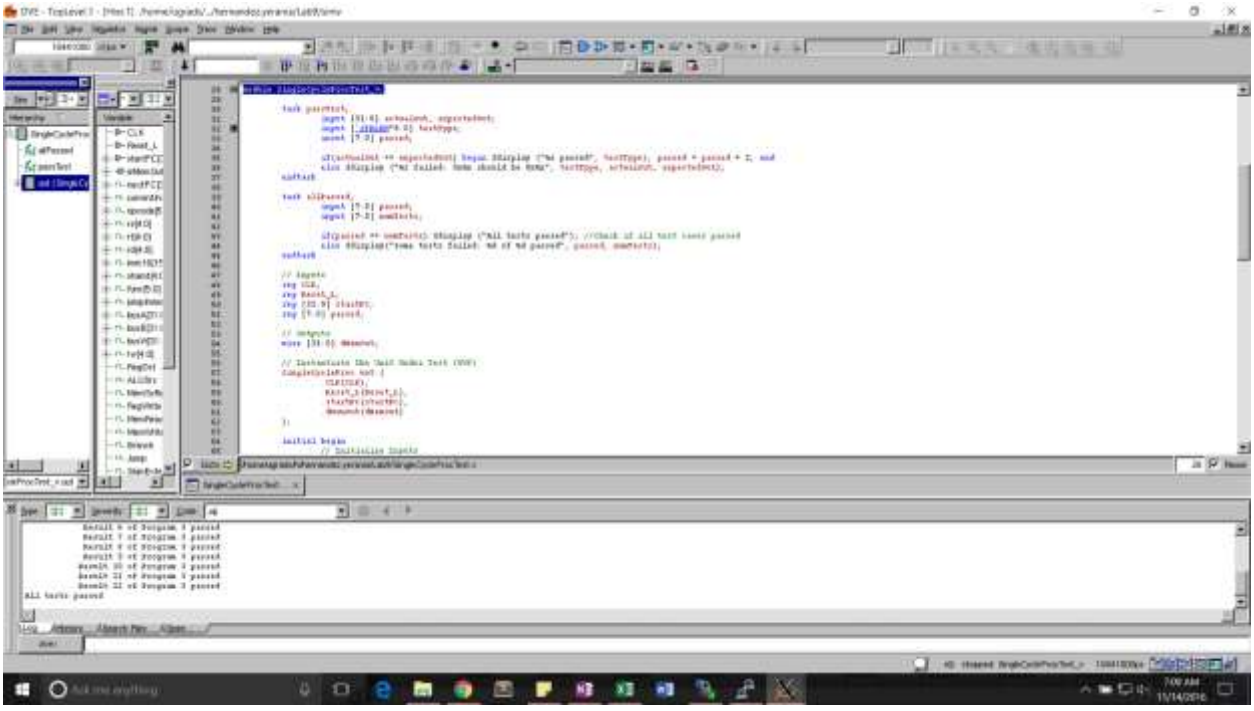
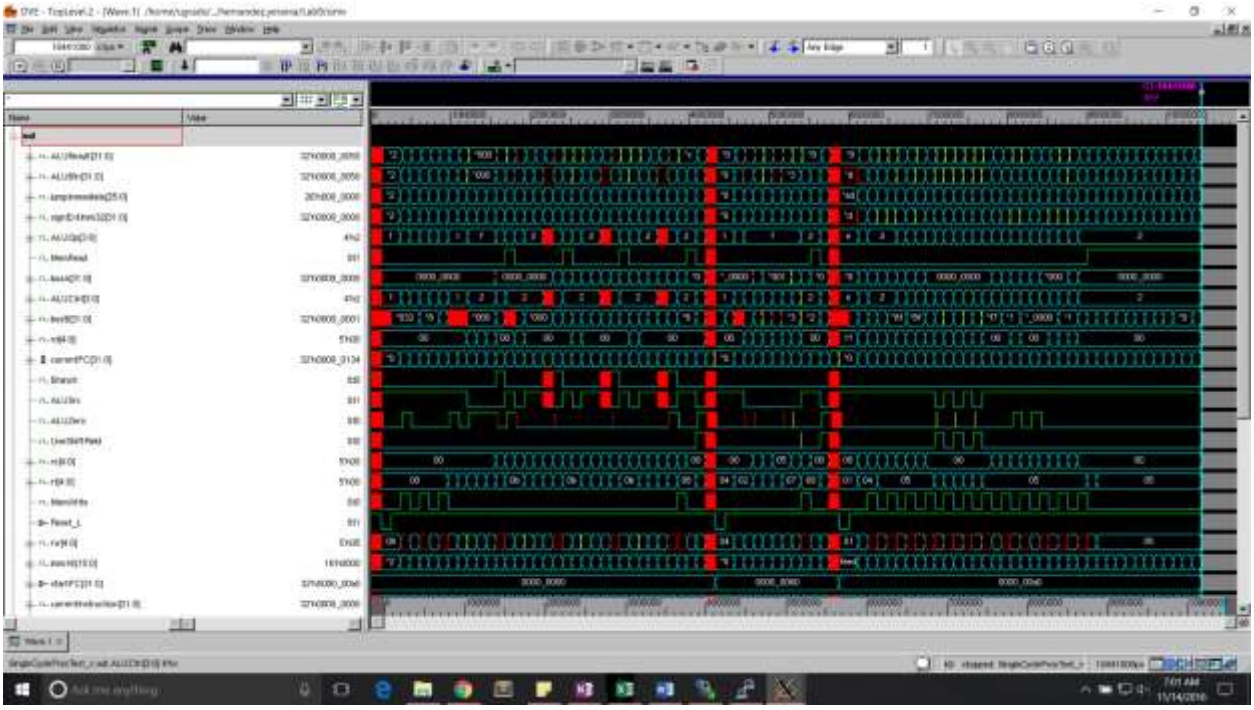
Lab 9

SingleCycleProc (VcS DVe Window “Heir.1”)



SingleCycleProc (Simulation Waveform “Wave.1”)



SingleCycleProc Explanation

The SingleCycleProc works properly based on the test bench. Analyzing the simulation, there are three different programs that are being run in order to test the different operations of the single cycle processor. The SingleCycleProc basically compiles and synthesizes all the components that have been made up from the previous labs and also includes the control bits necessary for the control unit. As a result, the simulation shows the results of each of the components and the final result after the control unit is implemented. For example, the first program is adding values of numbers and testing the operations of add, addi, lw, and so forth. However, program 2 is more focused on arithmetic logic and logical operations, and therefore, in the simulation you can see the results of these operations being stored in data memory. As a result, we know that it is testing add, sub, and, and so forth and that these operations are functioning properly. Program 3 tests the immediate instructions based on the logical and arithmetic operations, storing and loading the values from memory, which is shown in the results of the values while it tests for addi, addiu, andi, sliti, sltiu, xori, and so forth.